BOOK # 19

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THE VOLKER-CRAIG SERIES OF VIDEO DATA TERMINALS ARE DESIGNED IN A MODULAR FASHION TO PROVIDE FLEXIBILITY IN OPTIONS, UPGRADING, AND SERVICING.

IN THE STANDARD TERMINAL,THE BULK OF THE CIRCUITRY IS LOCATED ON SIX PRINTED CIRCUIT CARDS. FIVE OF THESE CARDS CONTAIN TTL AND MOS INTEGRATED CIRCUIT LOGIC. THE SIXTH COMPRISES A PORTION OF THE TERMINAL POWER SUPPLY.

FOUR OF THE LOGIC CARDS PLUG INTO A BANK OF EDGE CONNECTORS MOUNTED ON AN ASSEMBLY TO FORM THE LOGIC MODULE. WHEN VIEWED FROM THE FRONT OF THE TERMINAL THE CARDS ARE (IN ORDER):MEMORY (MEM),TIMING (TIM), CURSOR (CUR), KEYBOARD SEND/RECEIVE (KSR).

THE KEYBOARD CARD ASSEMBLY (ON MODELS VC203,VC303) IS MOUNTED AT THE FRONT OF THE CHASSIS. THE STANDARD TERMINAL IS EQUIPPED WITH ONE OF THE KB35 SERIES KEYBOARDS. THESE GENERATE THE 96 ASCII CODES. THE KEYS ARE ARRANGED SIMILARLY TO A TELETYPE 33 TERMINAL.

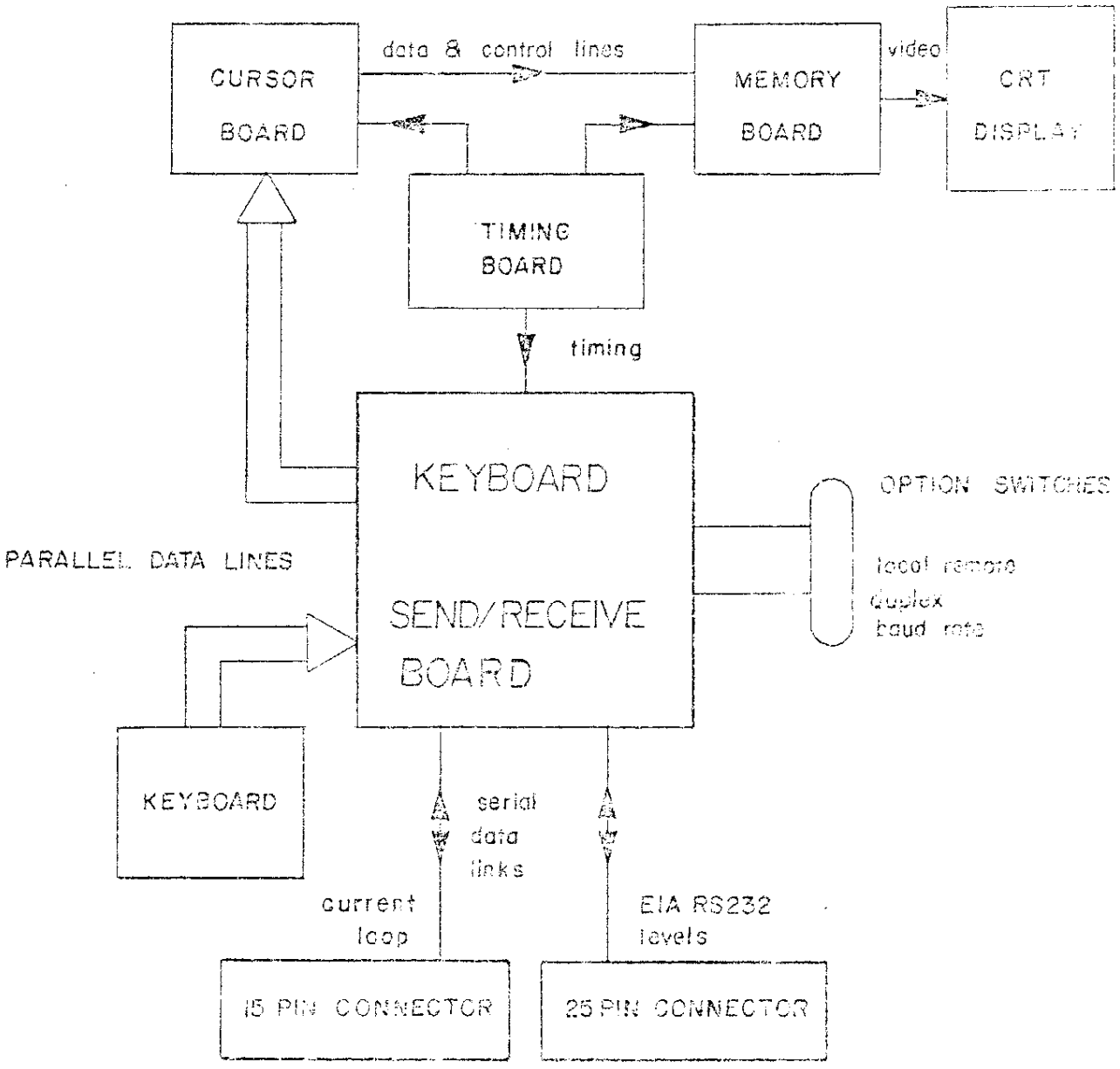
TERMINALS PROVIDED WITH OPTION "LOW" CONTAIN ONE OF THE KB44 SERIES KEYBOARDS WHICH GENERATE THE FULL 128 CHARACTER ASCII-7 CODE SET.

IN THIS MANUAL, EACH CIRCUIT CARD IS DESCRIBED, FOLLOWED BY A DESCRIPTION OF THE UNIT OPERATION.

THE BLOCK DIAGRAMS ARE ARRANGED IN SUCH A WAY AS TO LEAD THE READER TO THE APPROXIMATE LOCATION OF THE COMPONENTS ON THE SCHEMATIC RELATING TO THAT PARTICULAR BLOCK DIAGRAM.

NON-DISCLOSURE

BLOCK DIAGRAM OF TERMINAL



SERIAL NUMBERS

ALL PRODUCTS AND COMPONENTS (E.G.TERMINALS, CIRCUIT CARDS, KEYBOARDS,ETC.) CONTAIN MODEL (AND/OR PART) NUMBERS AND A UNIQUE SERIAL NUMBER. THIS ALLOWS THE COMPANY TO KEEP RECORDS FOR SERVICE PURPOSES. FOR EACH TERMINAL SHIPPED, THE PLANT MAINTAINS A RECORD WHICH SHOWS THE LEVEL OF UPGRADING ASSOCIATED WITH THAT TERMINAL. SIMILARLY, SERVICE DOCUMENTATION IS ITSELF SERIALISED IN ORDER TO FACILITATE BETTER COMPANY-FIELD SERVICE COMMUNICATIONS. THIS SERIAL NUMBER SHOULD BE REFERENCED WHEN CORRESPONDING WITH THE COMPANY. THE SERVICE DOCUMENTATION ALSO IDENTIFIES TERMINAL AND COMPONENT SERIAL NUMBERS FOR WHICH IT IS APPLICABLE.

PAGE HEADINGS

THERE ARE UP TO FIVE IDENTIFIERS AT THE HEADING OF EACH PAGE OF SERVICE DOCUMENTATION. THE FORMAT IS AS FOLLOWS:

SUB-SECTION & PAGE NO. TITLE PART NOS.(DATE CODES)
DATE OF ISSUE (D/M/YR) SERIAL NOS.

NOMENCLATURE

SINCE THIS MANUAL IS EDITED AND UP-DATED ON A COMPUTER-FACILITY, CERTAIN REPRESENTATIONS ARE AWKWARD AND COMPUTER-ORIENTED SYMBOLS MUST BE USED. AS OF THIS WRITING, THESE ARE:

DESCRIPTION	USE	SYMBOL
**********	***	******
BAR LINE	BARRED SIGNALS (COMPLEMENTS)	/ OR ' (QUOTE)

POWER SUPPLY

THE DESIGNATION OF THE POWER SUPPLY IN THE VC103,VC203, AND VC303 TERMINALS IS PS2100 AND IS IDENTIFIED BY NOTING THAT IT IS COMPRISED OF A SINGLE POWER TRANSFORMER (VC PART NO.0336), A PS100 CIRCUIT CARD, AND ASSOCIATED FILTER CAPACITORS, REGULATOR, AND RECTIFIER (CF.DWG).

ONE OF THE TRANSFORMER SECONDARY WINDINGS SUPPLIES A BRIDGE RECTIFIER AND FIXED VOLTAGE REGULATOR (LM323K) TO PRODUCE THE TTL VOLTAGE SOURCE OF 5V AT 3A.

THE SECOND SECONDARY WINDING FEEDS THE CIRCUIT CARD (PS100) ON WHICH THE VOLTAGE IS RECTIFIED AND REGULATED BY FIXED VOLTAGE REGULATORS TO PRODUCE VOLTAGES OF -5.0V AT 1A, -12.0V AT .5A, AND A DUAL 15V SUPPLY AT 100MA (PER SIDE). THE RELEVANT TEST POINTS FOR THESE VOLTAGES ARE IDENTIFIED ON THE CIRCUIT CARD.

TESTING FOR THE CORRECT VOLTAGES SHOULD ALWAYS BE CONSIDERED A PRELIMINARY STEP IN ANY TERMINAL FAULT ANALYSIS.

AN INCORRECT OR ABSENT VOLTAGE SHOULD BE TRACED BACK TO THE SECONDARY IN ORDER TO ISOLATE THE FAULT.

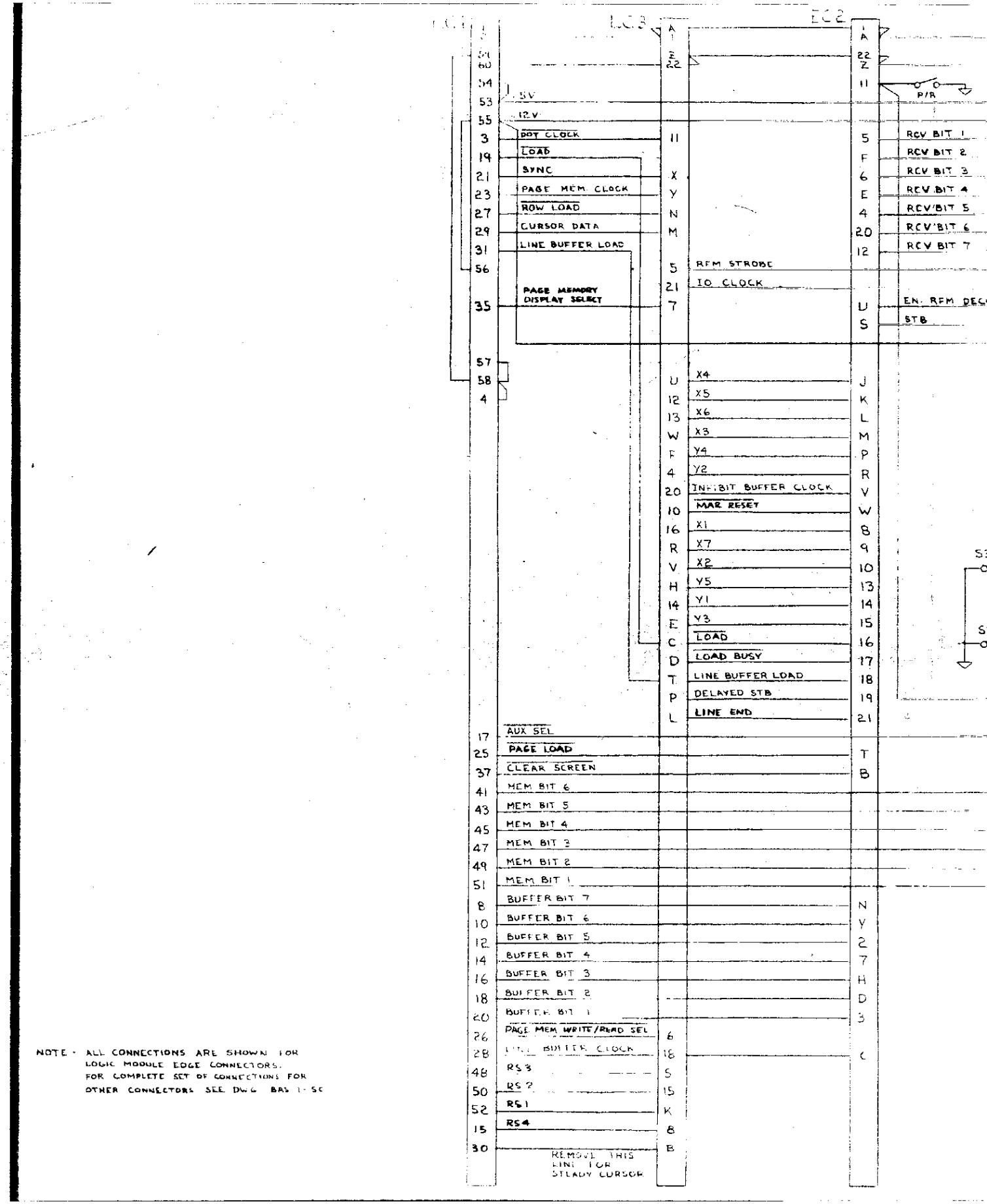
ALL PS2100 COMPONENTS ARE STANDARD INDUSTRY-SOURCED COMPONENTS, EXCEPT FOR THE TRANSFORMER WHICH MAY BE ORDERED DIRECTLY FROM VOLKER-CRAIG LTD. IN EMERGENCY CASES, THE TRANSFORMER MAY BE REPLACED BY ONE OR MORE STANDARD OFF-THE-SHELF TRANSFORMERS WHICH PRODUCE APPROXIMATELY (WITHIN 10%) THE SAME SECONDARY VOLTAGES AND CURRENTS.

KEYBOARD

THERE ARE NUMEROUS DIFFERENT TYPES (ESPECIALLY AS REGARDS LAYOUT AND ENCODING) OF KEYBOARDS EMPLOYED IN THE VC103,VC203, AND VC303 TERMINALS.

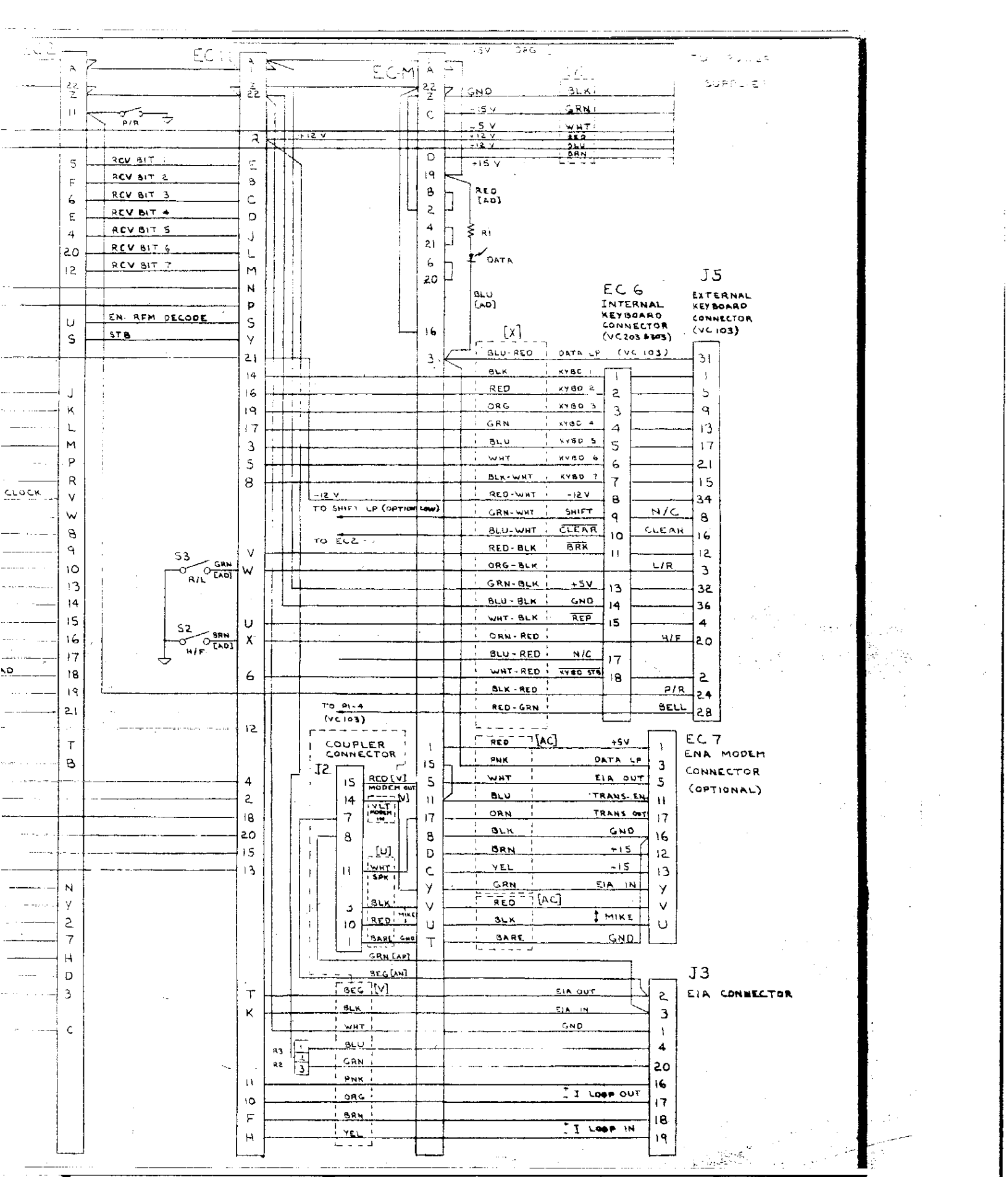
IN GENERAL, ALL KEYBOARDS ARE ASCII-ENCODED AND PRODUCE THE BIT-PATTERNS DOCUMENTED IN THE "VOLKER-CRAIG LIMITED OPERATING MANUAL". IF KEYBOARD PROBLEMS ARISE (E.G.FAILURE OF SOME KEYSWITCHES TO PRODUCE CHARACTERS, COMPLETE FAILURE, BOUNCE PROBLEMS-I.E. MULTIPLE CHARACTERS APPEARING) IT IS SUGGESTED THAT THE SUSPECT KEYBOARD RETURNED TO THE FACTORY FOR SERVICE.

CUSTOMERS MAY OBTAIN A COPY OF THE SCHEMATIC DIAGRAM PERTAINING TO THE KEYBOARD IN THEIR TERMINAL BY WRITING TO THE "VICE-PRESIDENT OF MARKETING, VOLKER-CRAIG LIMITED" AND BY STATING THE MODEL AND SERIAL NUMBER OF SAID KEYBOARD.



NOTE - ALL CONNECTIONS ARE SHOWN FOR LOGIC MODULE EDGE CONNECTORS. FOR COMPLETE SET OF CONNECTIONS FOR OTHER CONNECTORS SEE DWG BAS 1-SC

2	LAST REVISION DAY 25/02/75	SHEET 1 OF 2 ORIGINAL 21 FEB 1975	LOG-1-SC



LOG
LOGIC MODULE

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THE KEYBOARD SEND/RECEIVE CARD (KSR), ALSO KNOWN AS THE SERIAL/PARALLEL INTERFACE, RECEIVES SERIAL DATA FROM AN EXTERNAL DEVICE OR FACILITY AND CONVERTS THIS DATA INTO A PARALLEL FORMAT. SIMILARLY, THE PARALLEL WORD FROM THE KEYBOARD IS CONVERTED TO A SERIAL FORMAT FOR DATA TRANSMISSION.

THE UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART) IS THE HEART OF THIS CIRCUIT, PERFORMING THE RECEIVE AND TRANSMIT FUNCTIONS AS WELL AS CHECKING PARITY AND GENERATING THE NECESSARY START AND STOP BITS. ON RECEIVE, VALIDITY OF THE START BIT IS ALSO DETERMINED BY THE UART.

THE KSR CARD IS NOT REQUIRED UNLESS THE TERMINAL IS TO COMMUNICATE IN A SERIAL MODE.

BLOCK DIAGRAM DESCRIPTION

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

THE UART RECEIVER SECTION RECEIVES SERIAL DATA AND OUTPUTS PARALLEL DATA. IN SO DOING, IT CHECKS FOR LEGITIMATE START BITS. A RECEIVED PARITY BIT IS IGNORED. THE UART TRANSMITTER SECTION TRANSMITS SERIAL DATA FROM A PARALLEL INPUT. IN SO DOING, IT GENERATES A START BIT, 7 DATA BITS, A PARITY BIT (ODD OR EVEN-SELECTABLE), AND TWO STOP BITS.

INPUT SELECTOR

THE INPUT SELECTOR IS A MULTIPLEXER WHICH ALLOWS EITHER PARALLEL KEYBOARD OR PARALLEL AUXILIARY DATA TO PASS TO THE UART TRANSMITTER. AUXILIARY DATA MAY, FOR EXAMPLE, BE SUPPLIED BY THE MEMORY SECTION TO FACILITATE BLOCK DATA TRANSMISSION. THE AUXILIARY SELECT IS NORMALLY HIGH TO PERMIT KEYBOARD OPERATION.

CONTROL CODE DECODE AND BELL TIMER/DRIVER

THIS BLOCK DETECTS A CONTROL 'G' (ASCII:C000111) CODE AND PULSES A ONE-SHOT TO PROVIDE A TIMED SIGNAL FOR PURPOSES OF ACTIVATING AN AUDIBLE ALARM.

BAUD RATE COUNTER

THIS IS A TIMING CHAIN DRIVEN BY AN EXTERNAL 154KHZ CLOCK (PROVIDED BY THE TIMING SUBSYSTEM) OR AN ON-BOARD CLOCK (OPTIONAL). THE COUNTER HAS BCD PROGRAMMABLE INPUTS FOR SELECTING ONE OF 8 DIVISORS. THE OUTPUT FROM THE COUNTER IS A CLOCK SIGNAL WHICH IS 16 TIMES THE FREQUENCY OF THE DESIRED BAUD RATE.

REPEAT STROBE

THE OUTPUT FROM THE BAUD RATE COUNTER IS GATED TO THE UART STROBE INPUT TO ALLOW STROBING AT THE MAXIMUM CHARACTER TRANSMISSION SPEED. VIZ. IF A BAUD RATE OF 600 IS SELECTED, 60 CHARS/SEC WILL BE THE REPEAT RATE.

SERIAL RECEIVE

THIS BLOCK CONVERTS EITHER EIA VOLTAGE LEVELS OR 20 MA CURRENT LOOP SIGNALS TO TTL LEVELS. IT ALSO CONTAINS GATING TO BLOCK RECEPTION IN THE LOCAL MODE.

SERIAL TRANSMIT

THIS BLOCK CONVERTS TTL LEVELS TO EIA VOLTAGE LEVELS AND 20 MA CURRENT LOOP SWITCHING. IT ALSO CONTAINS GATING TO DISABLE TRANSMISSION IN THE LOCAL MODE.

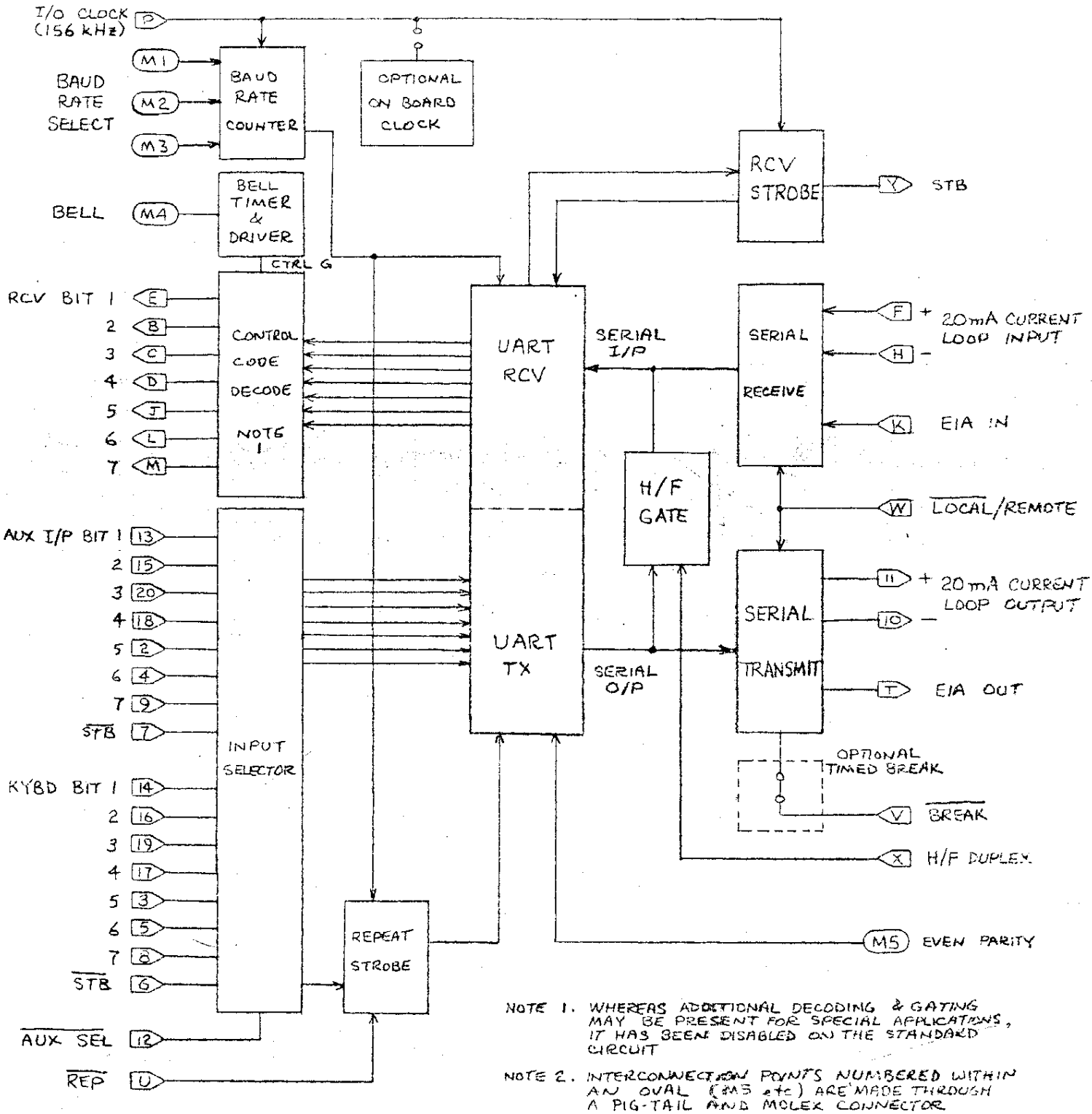
HALF/FULL GATE

IN THE HALF DUPLEX MODE, THE H/F GATE ROUTES THE UART SERIAL OUTPUT TO THE UART SERIAL INPUT THEREBY CAUSING DATA WHICH HAS BEEN CONVERTED TO SERIAL FORM, TO BE RECEIVED BY THE UART.

TIMED BREAK (OPTION)

THIS BLOCK PROVIDES A TIMED (VARIABLE-TRIMMER ADJUSTABLE) BREAK SIGNAL WHICH IS INITIATED BY DEPRESSING THE 'BREAK' KEY. THIS TIMED PERIOD DOES NOT A) ALL DEPEND ON THE DURATION OF THE KEYSWITCH CLOSURE. IF THIS OPTION IS NOT PROVIDED, THE BREAK KEY FORCES THE DATA OUTPUTS INTO A SPACE CONDITION (LOGIC ZERO) FOR AS LONG AS THE KEY IS DEPRESSED.

KSR BOARD



NOTE 1. WHEREAS ADDITIONAL DECODING & GATING MAY BE PRESENT FOR SPECIAL APPLICATIONS, IT HAS BEEN DISABLED ON THE STANDARD CIRCUIT

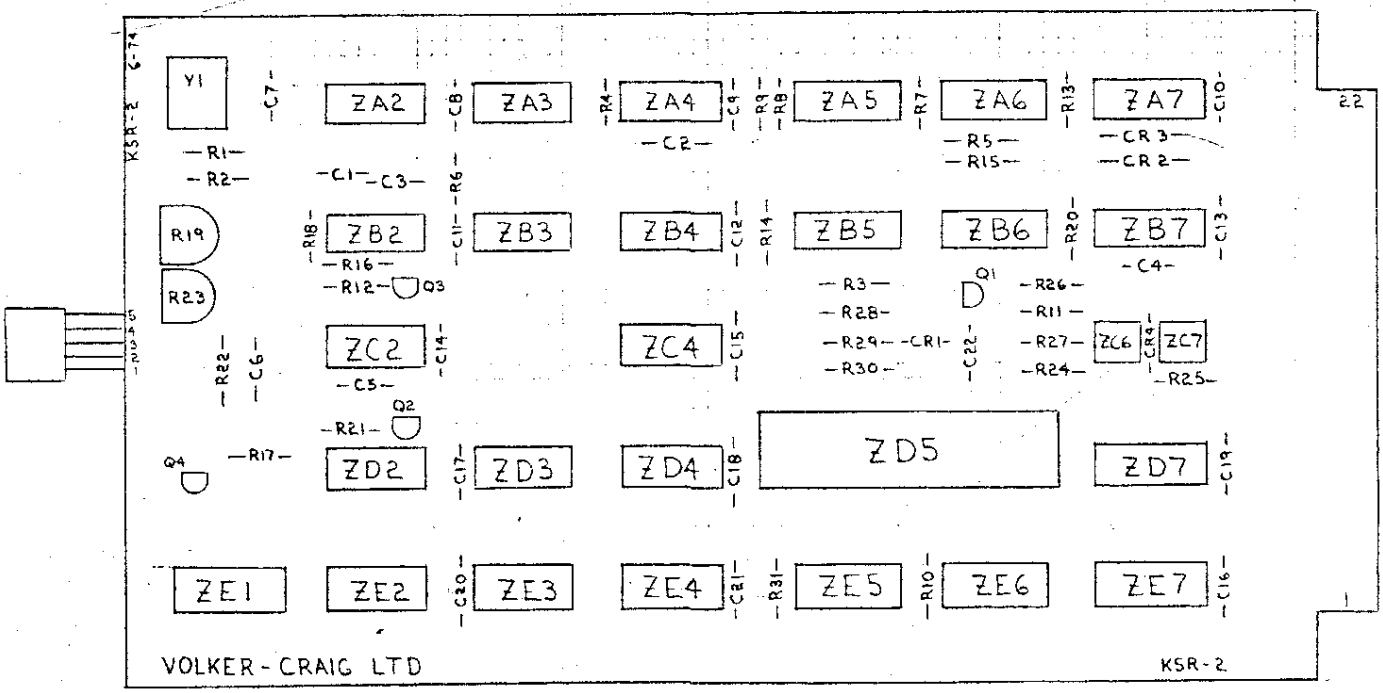
NOTE 2. INTERCONNECTION POINTS NUMBERED WITHIN AN OVAL (M5 etc) ARE MADE THROUGH A PIG-TAIL AND MOLEX CONNECTOR

KEYBOARD SEND/RECEIVE BOARD KSR-2

PIN FUNCTIONS

PIN NUMBER	DESCRIPTION	TO(<)/FROM(>)
1 +5VDC	VCC FOR ALL TTL	>PWR SUPPLY
2 AUX 5	AUXILIARY INPUT BIT 5	>MEM-43
3 KEYBD 5	KEYBOARD BIT 5	>KEYBD-5
4 AUX 6	AUX INPUT BIT 6	>MEM-41
5 KYBD 6	KEYBOARD BIT 6	>KYBD-6
6 KYBD STB	KEYBOARD STROBE	>KYBD-18
7 AUX STB	AUX STROBE	>
8 KYBD 7	KEYBOARD BIT 7	>KYBD-7
9 AUX 7	AUX BIT 7	>MEM-39
10 -	CURRENT LOOP TRANSMIT NEGATIVE	<J3-17
11 +	CURRENT LOOP TRANSMIT POSITIVE	<J3-16
12 AUX SELECT	SELECTS AUX INPUT	<MEM-17
13 AUX 1	AUX INPUT BIT 1	>MEM-51
14 KYBD 1	KYBD BIT 1	>KYBD-1
15 AUX 2	AUX BIT 2	>MEM-49
16 KYBD 2	KYBD BIT 2	>KYBD-2
17 KYBD 4	KYBD BIT 4	>KYBD-4
18 AUX 4	AUX BIT 4	>MEM-45
19 KYBD 3	KYBD BIT 3	>KYBD-3
20 AUX 3	AUX BIT 3	>MEM-47
21 -12VDC	VSS SUPPLY (FOR UART)	>PS100
22 GND	SYSTEM GROUND	>PWR SUPPLY
A +5VDC	VCC FOR ALL TTL	>PWR SUPPLY
B RCV BIT 2	ASCII DATA FROM UART BIT 2	<CUR-F
C RCV BIT 3	ASCII DATA FROM UART BIT 3	<CUR-6
D RCV BIT 4	ASCII DATA FROM UART BIT 4	<CUR-E
E RCV BIT 1	ASCII DATA FROM UART BIT 1	<CUR-5
F +	CURRENT LOOP RECEIVE POSITIVE	>J3-18
H -	CURRENT LOOP RECEIVE NEGATIVE	>J3-19
J RCV BIT 5	ASCII DATA FROM UART BIT 5	<CUR-4
K EIA IN	EIA LEVEL INPUT	>J3-3
L RCV BIT 6	ASCII DATA FROM UART BIT 6	<CUR-20
M RCV BIT 7	ASCII DATA FROM UART BIT 7	<CUR-12
N RFM STB	NOT ACTIVE ON STANDARD BOARD	>TIM-5
P I/O CLOCK	EXTERNAL CLOCK INPUT	>TIM-21
R +12VDC		>PS100
S ENABLE RFM STB	NOT ACTIVE ON STANDARD BOARD	>CUR-2
T EIA OUT	EIA LEVEL OUTPUT	<J3-2
U REP'	LOW FOR REPEATED STROBE	>KYBD-15
V BRK'	LOW FOR BREAK (FOR SPACE COND.)	>KYBD-11
W LOCAL'	LOW FOR LOCAL MODE OPERATION	>S3
X FULL DUPLEX'	LOW FOR FULL DUPLEX OPERATION	>S2
Y STB	?	<TIM-S
Z GND	SYSTEM GROUND	>POWER SUPPLY

COMPONENTS LAYOUT - KSR-2



COMPONENTS LIST - KSR-2

All resistors, unless otherwise noted, are ¼W, 5%.
All capacitors, unless otherwise noted, are 25V or greater.

C1	1n0 (CRYS. OSC.)	R1	2K2 (CRYS. OSC.)	ZA1	NOT USED
C2	10uF	R2	2K2 (CRYS. OSC.)	ZA2	7404 (CRYS. OSC.)
C3	50uF (BELL)	R3	3K3	ZA3	7474 (CRYS. OSC.&CNTL P)
C4	10n	R4	4K7	ZA4	7402
C5	.1uF (TIMED BRK)	R5	3K3	ZA5	7405
C6	47uF (TIMED BRK)	R6	3K3	ZA6	7401
C7	2n2	R7	3K3	ZA7	ML1488
C8	2n2	R8	3K3	ZB1	NOT USED
C9	2n2	R9	3K3	ZB2	74121 (BELL)
C10	2n2	R10	3K3	ZB3	7410 (BELL&CNTL P)
C11	2n2	R11	NOT USED	ZB4	7427 (BELL&CNTL P)
C12	2n2	R12	1K5	ZB5	7408
C13	2n2	R13	3K3	ZB6	7408
C14	2n2	R14	3K3	ZB7	ML1489
C15	2n2	R15	3K3	ZC1	NOT USED
C16	2n2	R16	2K2 (BELL)	ZC2	74121 (TIMED BRK)
C17	2n2	R17	4K7 (BELL)	ZC3	NOT USED
C18	2n2	R18	2K2 (BELL)	ZC4	7474
C19	2n2	R19	47K POT. (BELL)	ZC5	NOT USED
C20	2n2	R20	4K7	ZC6	IL-1
C21	2n2	R21	1K (TIMED BRK)	ZC7	IL-1
C22	2n2	R22	2K2 (TIMED BRK)	ZD1	NOT USED
		R23	470 POT. (TIMED BRK)	ZD2	NOT USED
CR1	1N4148	R24	47	ZD3	74 .21
CR2	1N4001	R25	220	ZD4	74151
CR3	1N4001	R26	1K5	ZD5	AY-5-1012
CR4	1N4148	R27	1K5	ZD6	NOT USED
		R28	2K2	ZD7	74157
Q1	2N4401	R29	2K2	ZE1	NOT USED
Q2	2N4401 (TIMED BRK)	R30	2K2	ZE2	NOT USED
Q3	2N4401 (BELL)	R31	1K5	ZE3	7493
Q4	2N4403 (BELL)			ZE4	7493
		Y1	QUARTZ CRYSTAL	ZE5	7474 (CRYS. OSC.)
			1.2288 MHz	ZE6	7400
				ZE7	74157

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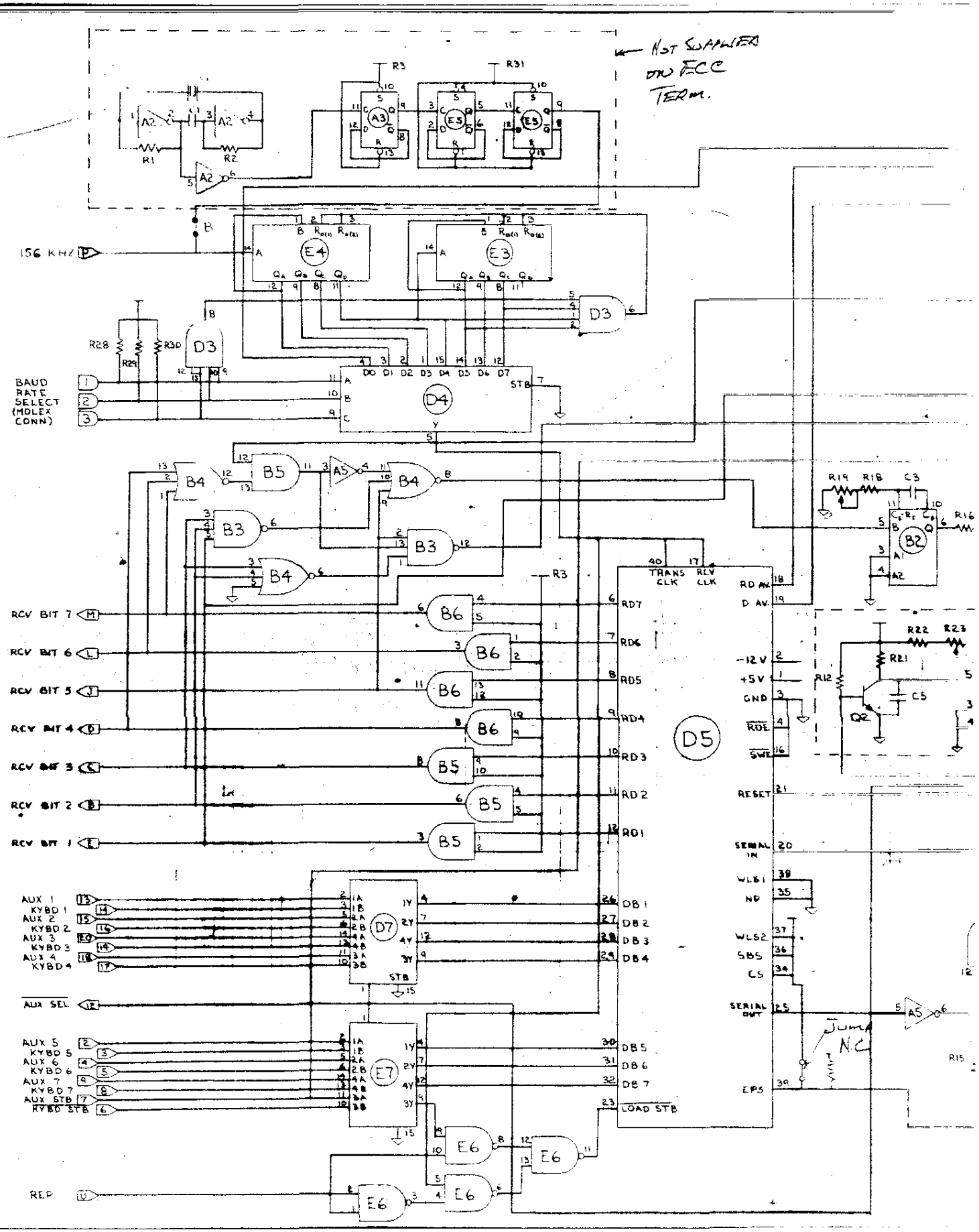
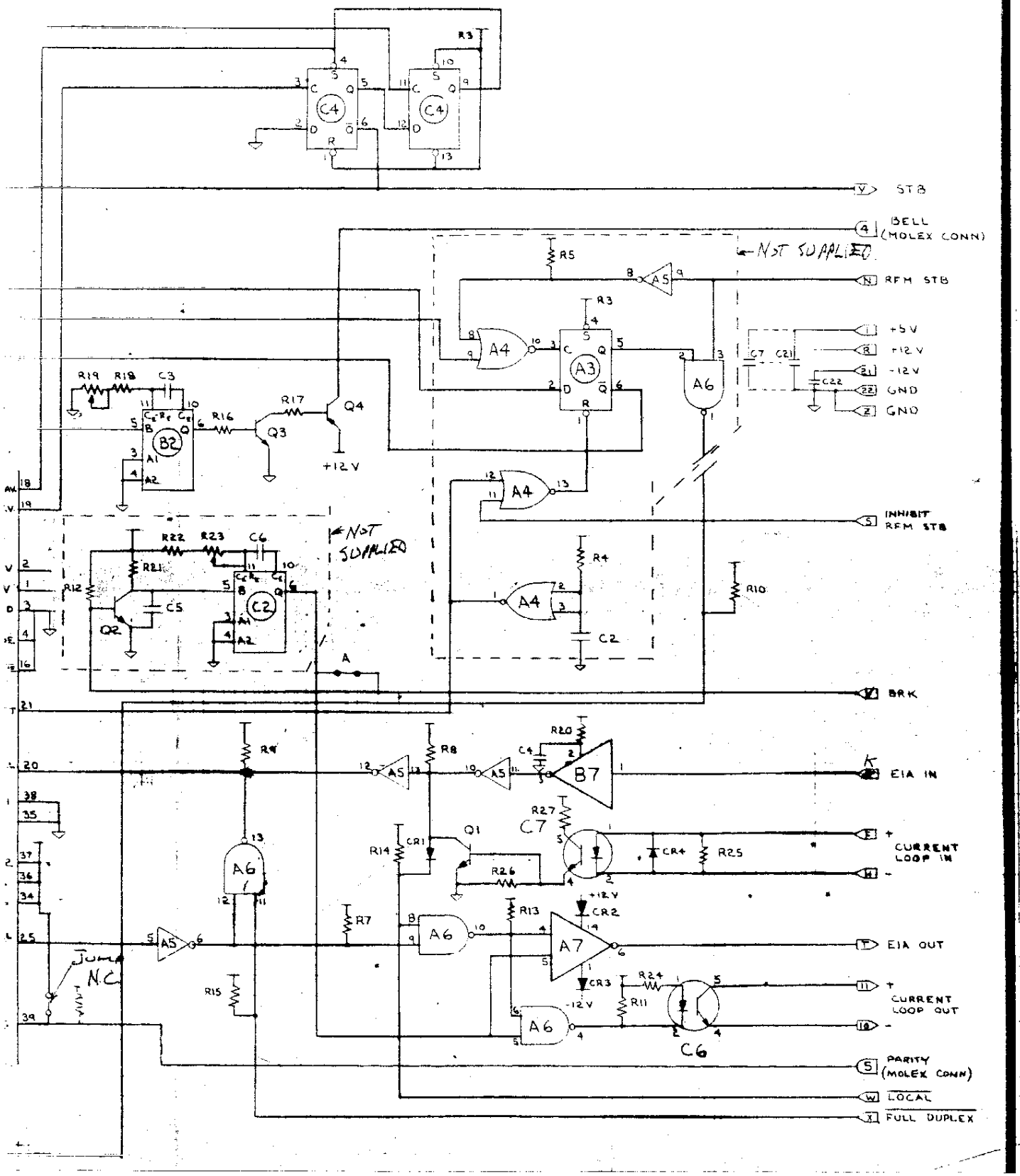


1	BOARD DATE 6.74	SHEET 1 OF 2	KSR-2-SC	KEYBOARD
	LAST REVISION DAY 25/02/75	ORIGINAL CT 17/10/74		



KSR
KEYBOARD SEND/RECEIVE PCB

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THE CURSOR BOARD CONTAINS THE TWO REGISTERS WHICH DETERMINE THE POSITION OF THE CURSOR, OPERATES ON THE CONTROL CODES WHICH AFFECT THE POSITION OF THE CURSOR, AND LATCHES DATA ARRIVING FROM THE KSR BOARD UNTIL IT HAS BEEN PROCESSED. OTHER PORTIONS OF THE CIRCUIT INTERACT WITH THE TIMING BOARD TO ENSURE THAT CHARACTERS ARE INSERTED INTO THE CORRECT PLACES IN THE PAGE MEMORY AND TO IMPLEMENT THE SCROLL FUNCTION IN THE ROLL MODE.

BLOCK DIAGRAM DESCRIPTION

DATA INPUT LATCH THIS BLOCK STORES DATA BITS RECEIVED FROM THE UART ON THE KSR BOARD UNTIL LOADED INTO PAGE MEMORY UNLESS THE RECEIEVD DATA IS A CONTROL CODE. CONTROL CODES ARE STORED UNTIL A CONTROL FUNCTION HAS BEEN PERFORMED.

CONTROL CODE DECODER

THE RECODER DETECTS CONTROL CODES (THE TWO MOST SIGNIFICANT BITS OF THE ASCII WORD ARE '00' IF THE CHARACTER IS A CONTROL CODE) AND IMPLEMENTS THE REQUIRED OPERATION. CONTROL CODES ARE NOT DISPLAYED. THE CONTROL CODES DECODED BY CUR-1 ARE:

CODE	NAME	FUNCTION	ASCII BIT-PATTERN
****	****	********	**********
CTRL H	BKSP	BACKSPACE	0001000
CTRL I	FWD	ADVANCE CURSOR	0001001
CTRL J	LF	LINE FEED	0001010
CTRL K	HOME	MOVE CURSOR TO TOP LEFT	0001011
CTRL L	CLEAR	CLEAR SCREEN & HOME CURSOR	0001100
CTRL M	CR	CARRIAGE RETURN	0001101
CTRL N	RLF	MOVE CURSOR UP	0001110
CTRL O	CAD	ENABLE CURSOR ADDRESSING	0001111

UC/LC CONVERTER

ON STANDARD UPPER-CASE ONLY TERMINALS, INCOMING LOWER-CASE CHARACTERS ARE CONVERTED TO UPPER-CASE CHARACTERS. FOR TERMINALS EQUIPPED WITH OPTION "LOW", A TRACE IS CUT AND A JUMPER IS ADDED TO ALLOW THE LOWER-CASE CHARACTERS TO PASS THROUGH UNALTERED.

CURSOR ADDRESS REGISTER

THIS REGISTER STORES 7-BIT X AND 5-BIT Y COMPONENTS OF CURSOR ADDRESS. THE X-ADDRESS IS INCREMENTED EACH TIME A CHARACTER IS ADDED TO A LINE

AND DECREMENTED WHEN A BKSP CONTROL CODE (BKSP OR CTRL H) IS RECEIEVED. THE Y-ADDRESS IS INCREMENTED BY A LINE FEED CONTROL CODE (LF OR CTRL J), OR BY OVERRUNNING THE END OF THE CHARACTER LINE. IT IS DECREMENTED BY A RERSE LINE FEED CONTROL CODE (CTRL N) OR BY THE SCROLL CIRCUITRY.

LOAD CONTROL

THIS CIRCUIT GENERATES A DELAYED STROBE AFTER CHARACTERS ARE RECEIEVED FROM THE UART. A LOAD' SIGNAL FROM THE TIMING BOARD CAUSES THE GENERATION OF BUFFER LOAD' FOR A DISPLAYABLE CHARACTER. FOR A CONTROL CHARACTER, THE LOAD' PULSE ENABLES THE CONTROL CODE DECODER.

CLEAR CONTROL

THIS CONTROLS THE INSERTION OF SPACES INTO THE BOTTOM TWO LINES OF THE DISPLAY FOR SCROLL OPERATION OR INTO THE ENTIRE PAGE FOR CLEAR SCREEN OPERATION.

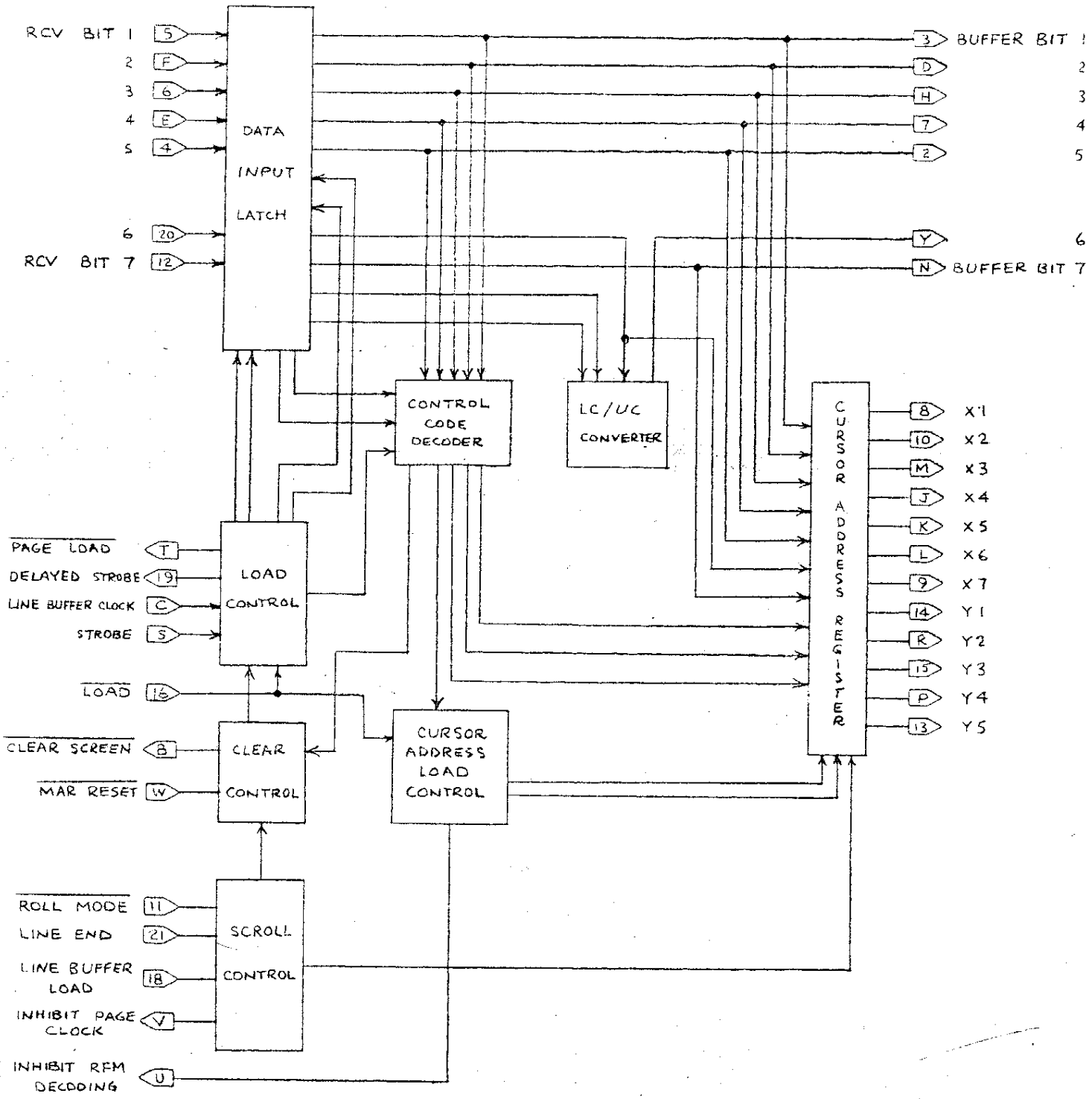
CURSOR ADDRESS LOAD CONTROL

AFTER BEING LATCHED BY A CTRL O CHARACTER, THE NEXT TWO ASCII CHARACTERS ARE ROUTED TO PRESET THE X AND Y CURSOR ADDRESS REGISTERS, RESPECTIVELY.

SCROLL CONTROL

WITH THE TERMINAL IN THE ROLL MODE, A CHARACTER INSERTED IN THE LAST POSITION OF THE BOTTOM LINE (OR A LINE FEED ANYWHERE ON THE LAST LINE) INITIATES THE SCROLL OPERATION. THE NEXT MAR RESET PULSE AFTER INITIATION CAUSES A SPACE CODE TO BE SENT TO THE PAGE MEMORY WHERE IT IS LOADED INTO THE TOP TWO LINES OF THE MEMORY (ODD AND EVEN LINES IN PARALLEL). THE LOADING STOPS WHEN THE LINE END SIGNAL GOES HIGH. AT THIS TIME, THE Y-POSITION COUNTER IN THE CURSOR ADDRESS REGISTER IS DECREMENTED ONE COUNT. DURING THE NEXT LINE BUFFER LOAD SIGNAL, THE INHIBIT PAGE CLOCK' SIGNAL IS ENABLED FOR 80 CHARACTER TIMES WHICH CAUSES THE MEMORY ADDRESS REGISTER ON THE TIMING BOARD TO HALT COUNTING FOR THIS PERIOD. THIS RESULTS IN THE TW BLANK LINES BEING POSITIONED AT THE BOTTOM OF THE SCREEN. WHEN A SECOND LINE BUFFER LOAD SIGNAL ARRIVES, THE SCROLL CIRCUIT IS RESET AND THE Y-POSITION COUNTER IS DECREMENTED ONCE MORE CAUSING THE CURSOR TO APPEAR ON THE SECOND LINE FROM THE BOTTOM.

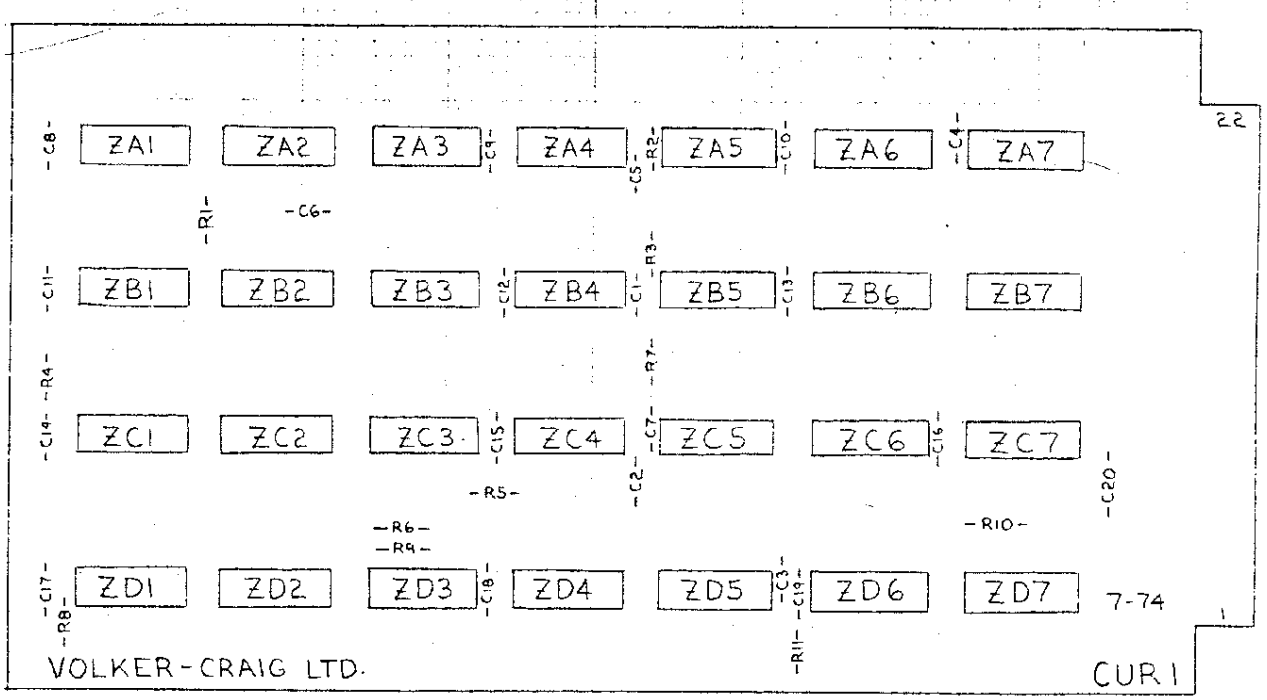
CURSOR BOARD



PIN FUNCTIONS

PIN NUMBER	DESCRIPTION	TO(<),FROM(>)
1 +5VDC	VCC FOR ALL TTL	>REG
2 BUFFER BIT 5	ASCII DATA TO PAGE MEMORY	<MEM-12
3 BUFFER BIT 1	ASCII DATA TO PAGE MEMORY	<MEM-20
4 RCV BIT 5	ASCII DATA FROM UART	>KSR-J
5 RCV BIT 1	ASCII DATA FROM UART	>KSR-E
6 RCV BIT 3	ASCII DATA FROM UART	>KSR-C
7 BUFFER BIT 4	ASCII DATA TO PAGE MEMORY	<MEM-14
8 X1	CUR ADDR CHAR POSN BCD 1	<TIM-16
9 X7	CUR ADDR CHAR POSN BCD 40	<TIM-R
10 X2	CUR ADDR CHAR POSN BCD 2	<TIM-V
11 ROLL MODE'	LOW TO ENABLE SCROLLING OPERATION	>P/R SW.
12 RCV BIT 7	ASCII DATA FROM UART	>KSR-M
13 Y5	CUR ADDR LINE POSN BIN 16	<TIM-H
14 Y1	CUR ADDR LINE POSN BIN 1	<TIM-14
15 Y3	CUR ADDR LINE POSN BIN 4	<TIM-E
16 LOAD'	LOW TO ENABLE GENERATION OF BUFFER LOAD' ON CTRL CODES OR CURSOR ADDRESSING	>TIM-C
17 LOAD BUSY'	NOT USED ON CUR-1	>TIM-D
18 LINE BUFFER LOAD	TRIGGERS SCROLLING AT PAGE BOTTOM	>TIM-T
19 DELAYED STROBE	LOW FOR 641NS WHILE CHAR IS BEING LOADED.GOES HIGH WHEN READY	<TIM-P
20 RCV BIT 6	ASCII DATA FROM UART	>KSR-L
21 LINE END	POSITIVE ADGES RESET SCROLL LATCH	>TIM-L
22 GND	SYSTEM GROUND	>PWR SUPPLY
A +5VDC	VCC SUPPLY	>PWR SUPPLY
B CLEAR SCREEN'	LOW FOR ONE COMPLETE MEMORY CYCLE TO CLEAR SCREEN;FOR 1 LINE TO SCROLL	<MEM-37
C LINE BUFFER CLOCK	POSITIVE EDGES START & STOP DELAYED STROBE AFTER DATA RECEIVED	>TIM-18
D BUFFER BIT 2	ASCII DATA TO PAGE MEMORY	<MEM-18
E RCV BIT 4	ASCII DATA FROM UART	>KSR-D
F RCV BIT 2	ASCII DATA FROM UART	>KSR-B
H BUFFER BIT 3	ASCII DATA TO PAGE MEMORY	<MEM-16
J X4	CUR ADDR CHAR POSN BCD 8	<TIM-U
K X5	CUR ADDR CHAR POSN BCD 10	<TIM-12
L X6	CUR ADDR CHAR POSN BCD 20	<TIM-13
M X3	CUR ADDR CHAR POSN BCD 4	<TIM-W
N BUFFER BIT 7	ASCII DATA TO PAGE MEMORY	<MEM-8
P Y4	CUR ADDR LINE POSN BIN 8	<TIM-F
R Y2	CUR ADDR LINE POSN BIN 2	<TIM-4
S STROBE	POS.EDGE TRIGGERS LOAD SEQUENCE	>KSR-W
T PAGE LOAD'	LOW WHEN CHARACTERS OR SPACES ARE TO BE LOADED INTO PAGE MEMORY	<MEM-25
U INHIBIT RFM DECODING	HIGH DURING CURSOR ADDRESSING	<KSR-S
V INHIBIT PAGE CLOCK'	LOW FOR ONE LINE BUFFER LOAD TIME DURING SCROLL SEQUENCE	<TIM-20
W MAR RESET'	NEG.EDGE TRIGGERS SCROLL LATCH	>TIM-10
X CLEAR'	OPTIONALLY WIRED TO C4-3 VIA 100-OHM RES.FOR CLEAR PAGE SWITCH	>KYBD-10
Y BUFFER BIT 6	ASCII DATA TO PAGE MEMORY	<MEM-10
Z GND	SYSTEM GROUND	>PWR SUPPLY

COMPONENTS LAYOUT -CUR-1



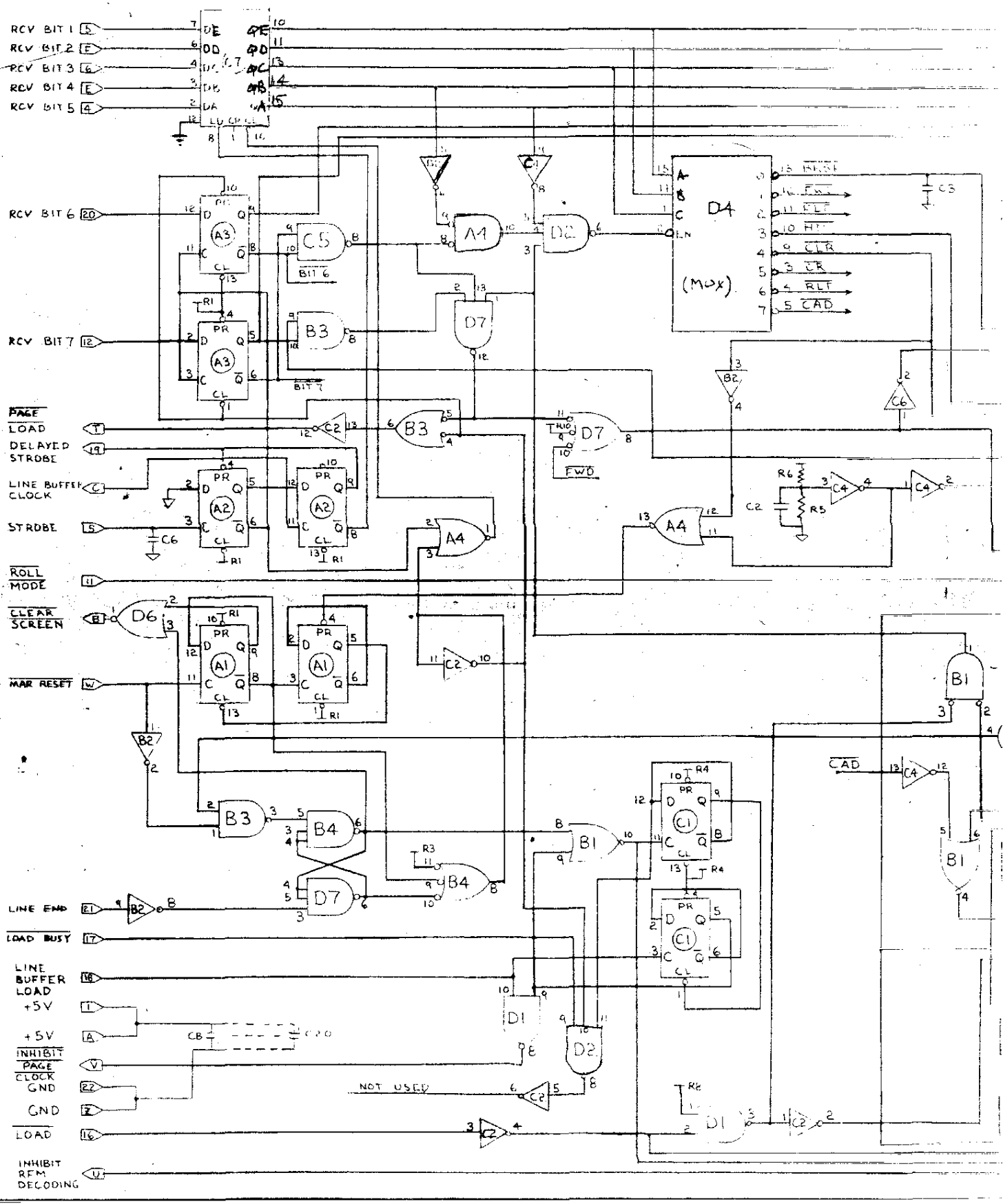
COMPONENTS LIST -CUR-1

All resistors, unless otherwise noted, are ¼W, 5%.
All capacitors, unless otherwise noted, are 25V or greater.

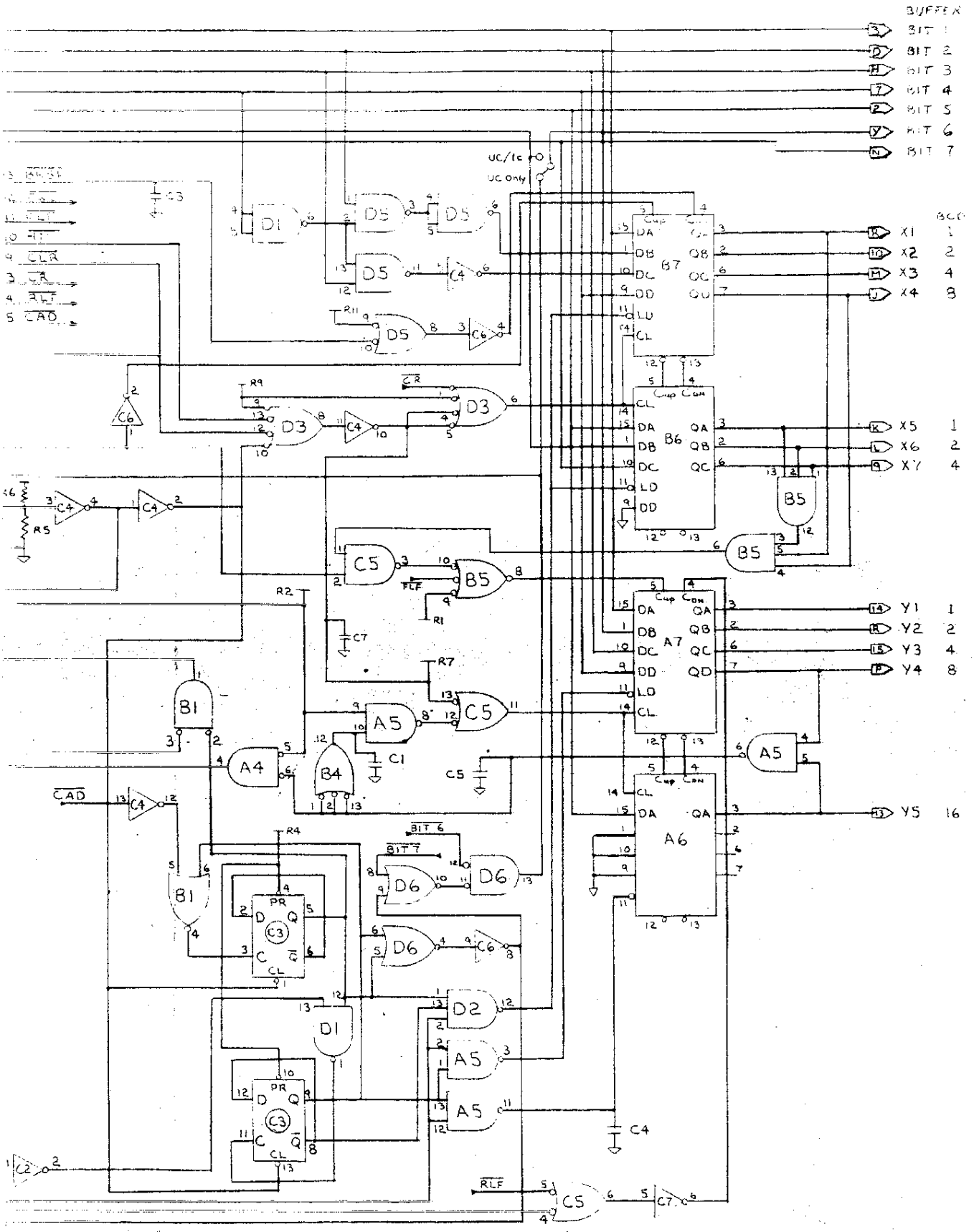
C1	4n7
C2	15uF
C3	n47
C4	n47
C5	1n0
C6	4n7
C7	1n0
C8	4n7
C9	4n7
C10	4n7
C11	4n7
C12	4n7
C13	4n7
C14	4n7
C15	4n7
C16	4n7
C17	4n7
C18	4n7
C19	4n7
C20	15uF

R1	1K5
R2	1K5
R3	1K5
R4	1K5
R5	3K3
R6	2K2
R7	470
R8	1K5
R9	1K5
R10	1K5
R11	1K5

ZA1	7474
ZA2	7474
ZA3	7474
ZA4	7402
ZA5	7400
ZA6	74193
ZA7	74193
ZB1	7402
ZB2	7404
ZB3	7400
ZB4	7410
ZB5	7411
ZB6	74193
ZB7	74192
ZC1	7474
ZC2	7404
ZC3	7474
ZC4	7404
ZC5	7400
ZC6	7404
ZC7	7496
ZD1	7400
ZD2	7410
ZD3	7420
ZD4	8251
ZD5	7400
ZD6	7402
ZD7	7410



1	BOARD DATE 7-74		CURSC
	LAST REVISION DAY	ORIGINA	



CUR
CURSOR BOARD

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TIMING CIRCUIT CARD (TIM) SERVICE INFORMATION

THE TIMING CARD (TIM) GENERATES ALL OF THE TIMING SIGNALS REQUIRED FOR THE OPERATION OF THE TERMINAL. THESE INCLUDE MEMORY CIRCULATION CLOCKS, DOT DISPLAY CLOCK, AND VIDEO SYNCHRONIZING SIGNALS. THE TIMING CARD ALSO INCLUDES THE CIRCUITRY TO DERIVE PULSES AT THE APPROPRIATE TIMES FOR LOADING CHARACTERS INTO THE PAGE MEMORY AND TO GENERATE THE VISIBLE CURSOR.

IT SHOULD BE NOTED THAT THE STATE OF THE CHARACTER COUNTER INDICATES THE POSITION OF THE NEXT CHARACTER TO BE DISPLAYED. THIS COMPENSATES FOR THE VARIOUS PROPAGATION DELAYS, PARTICULARLY THAT OF THE CHARACTER GENERATOR ROM (ON THE MEMORY CARD).

BLOCK DIAGRAM DESCRIPTION

MASTER CLOCK

THIS BLOCK GENERATES A CRYSTAL-CONTROLLED 12.4800 MHZ SQUAREWAVE.

COLUMN COUNTER

THIS BLOCK GENERATES THE 8 VERTICAL COLUMNS OF THE 8 X 10 DOT MATRIX FORMING THE CHARACTERS. 5 OF THE COLUMNS CONTAIN THE DOT MATRIX PATTERN AND THE REMAINING 3 COLUMNS SERVE TO SPACE THE CHARACTERS.

DOT CLOCK AND ROW LOAD

THIS BLOCK GATES OFF THE DOT CLOCK FOR THE VIDEO OUTPUT SHIFT REGISTERS (ON MEM CARD) DURING "ROW LOAD", WHEN THE OUTPUT OF THE CHARACTER GENERATOR IS LOADED INTO THE VIDEO SHIFT REGISTERS. ROW LOAD IS INHIBITED DURING VERTICAL RETRACE AND DURING BLANKED SCANS BETWEEN CHARACTER LINES (SCAN BLANKING PROVISION IS DELETED ON UC/LC AND GRAPHICS TERMINALS).

CHARACTER COUNTER

THIS BLOCK DEFINES 100 CHARACTER POSITIONS PER LINE, OF WHICH 80 ARE DISPLAYED. ALSO DERIVED ARE THE HORIZONTAL SYNC, I/O CLOCK, AND LINE BUFFER LOAD SIGNALS.

SCAN LINE COUNTER

THIS BLOCK GENERATES BCD ROW SELECT SIGNALS TO CONTROL THE ROW OUTPUT OF THE CHARACTER GENERATOR ROM (ON MEM).

LINE COUNTER

THE LINE COUNTER DEFINES 26 CHARACTER LINES PER PAGE, OF WHICH 24 ARE DISPLAYED. IT ALSO PRODUCES THE VERTICAL SYNC AND PAGE MEMORY DISPLAY SELECT SIGNALS.

SYNC GENERATOR

THE SYNC GENERATOR, USING AS INPUTS THE SIGNALS FROM THE ABOVE-MENTIONED COUNTERS, PRODUCES THE HORIZONTAL AND VERTICAL SYNC PULSES WHICH ARE MIXED INTO THE COMPOSITE VIDEO OUTPUT LINE.

PAGE CLOCK SELECT/CONTROL

THIS CIRCUIT SELECTS THE 2.08MHZ CLOCK SIGNAL DURING THE RECIRCULATION CYCLE OF PAGE MEMORY. THE 1.56MHZ CLOCK SIGNAL IS SELECTED DURING THE LINE BUFFER LOAD CYCLE. WHEN THE TERMINAL IS IN THE ROLL MODE, "INHIBIT BUFFER CLOCK" CAUSES THE PAGE CLOCK SIGNAL TO THE MEMORY ADDRESS REGISTER TO BE STOPPED AFTER THE LAST CHARACTER ON THE DISPLAY IN ORDER TO IMPLEMENT THE SCROLL.

LINE BUFFER LOAD GENERATOR

THIS BLOCK DERIVES A SIGNAL DURING SCAN 9 TO LOAD LINE SHIFT REGISTERS (ON MEM) WITH THE NEXT 80 CHARACTERS TO BE DISPLAYED.

MEMORY ADDRESS REGISTER ("MAR")

THIS CIRCUIT INCREMENTS IN STEP WITH PAGE SHIFT REGISTERS TO KEEP TRACK OF DATA WITHIN MEMORY. BECAUSE THE MEMORY IS ORGANIZED AS TWO HALF PAGES OF 12 LINES EACH IN PARALLEL (I.E.1024 X 16 BITS), THE COUNTING RANGE OF THE "MAR" IS 0 TO 1023.

CURSOR ADDRESS COMPARATOR

THIS SECTION PRODUCES SIGNALS TO INDICATE WHEN THE X AND Y POSITIONS OF CURSOR ADDRESS (CUR) ARE THE SAME AS THOSE OF "MAR".

PAGE MEMORY STOP COMPARATOR

THIS BLOCK PRODUCES A SIGNAL TO STOP THE RECIRCULATION OF THE PAGE MEMORY AT THE BEGINNING OF THE NEXT LINE TO BE LOADED INTO THE LINE BUFFER.

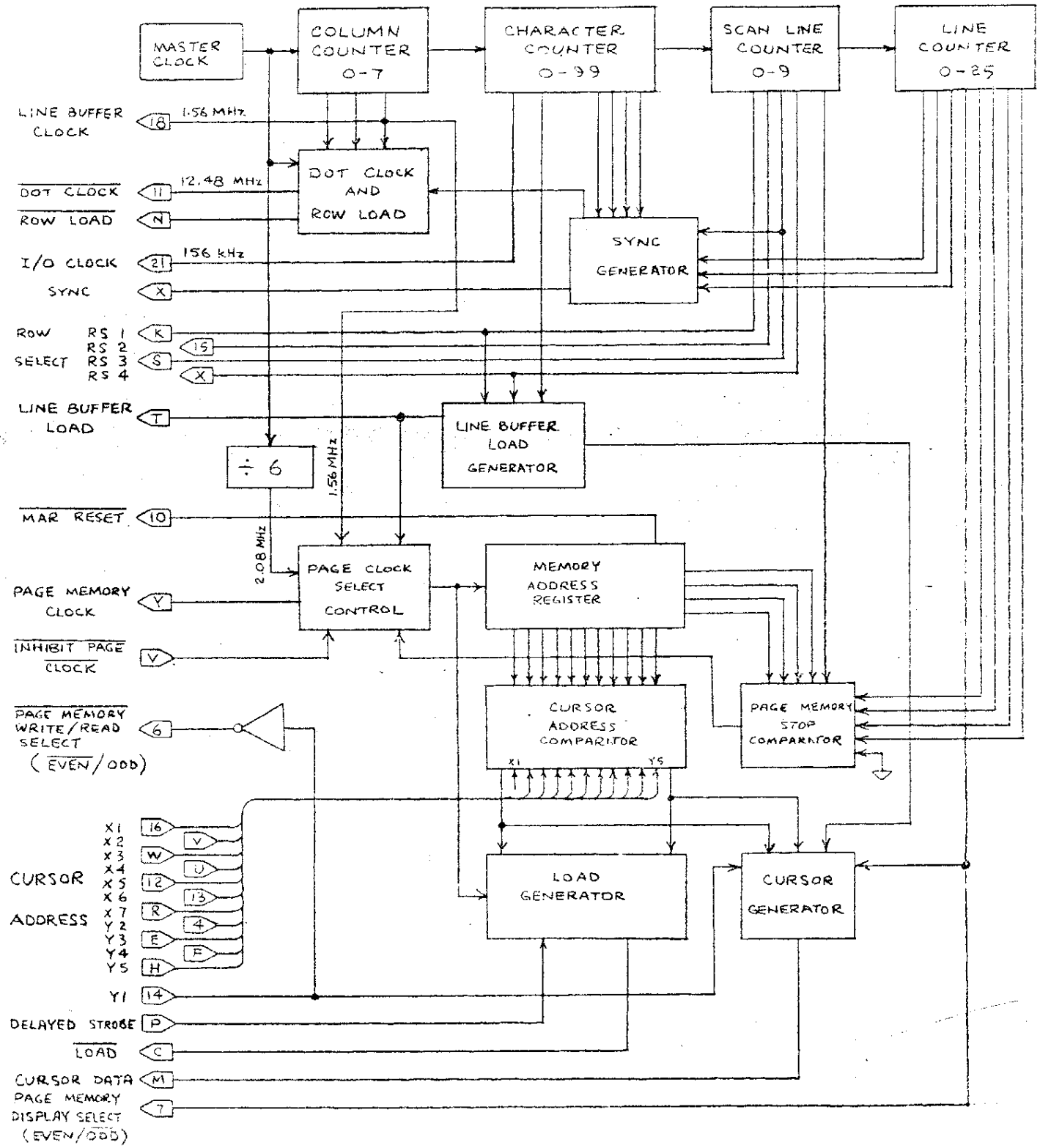
LOAD GENERATOR

THE ARRIVAL OF A DELAYED STROBE PULSE TO THE TIMING CARD INDICATES THAT A CHARACTER IS WAITING TO BE OPERATED UPON BY THE CURSOR CARD. WHEN THE CURSOR ADDRESS COMPARATOR INDICATES THAT THE "MAR" IS AT THE CORRECT ADDRESS, A LOAD PULSE IS GENERATED.

CURSOR GENERATOR

THIS CIRCUIT IS ENABLED WHILE THE LINE INDICATED BY THE CURSOR IS BEING LOADED INTO THE LINE BUFFER. THE CURSOR SIGNAL APPEARS 10 SCANS LATER SO AS TO UNDERSCORE THE LINE BEING DISPLAYED.

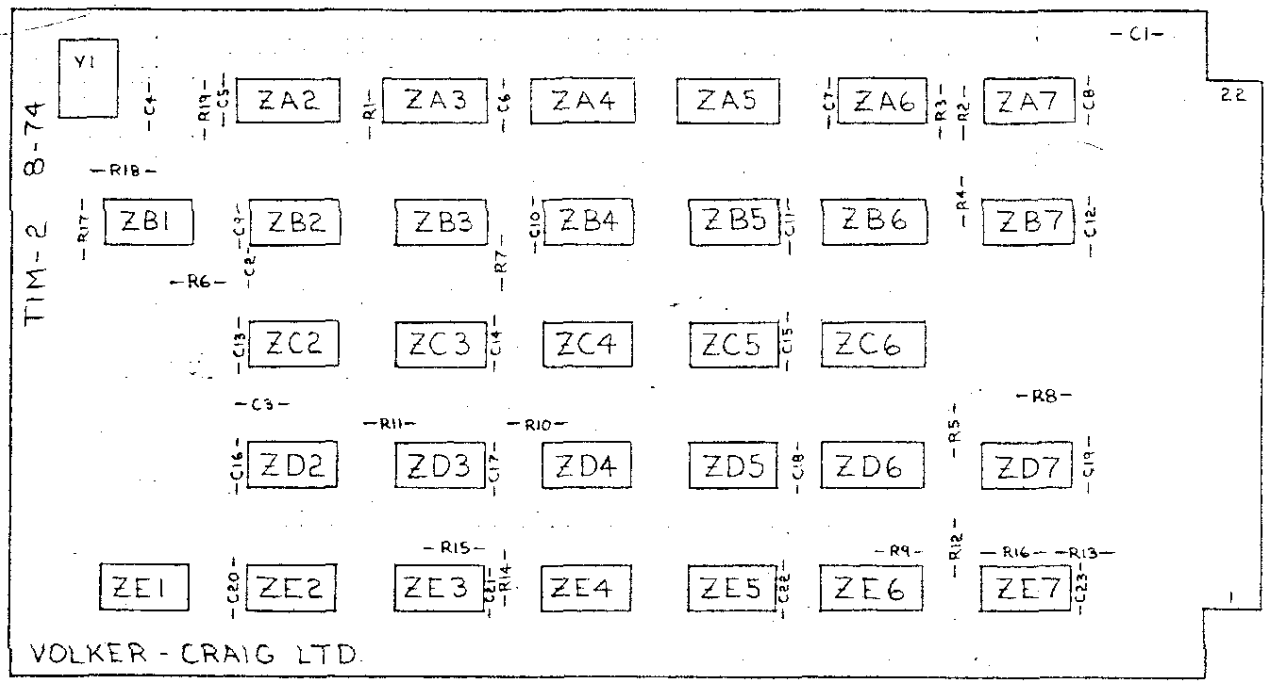
TIMING BOARD



PIN FUNCTIONS

PIN NUMBER		DESCRIPTION	TO(<),FROM(>)
1	+5VDC	VCC FOR ALL TTL	>REG
2	VERTICAL SYNC'	LOW FOR 256.4US. REPEATED AT 60HZ (16.667 MS.)	<NOT USED
3	COUNTER CLEAR'	PULL LOW TO CLEAR ALL COUNTERS	>NOT USED
4	Y2	CURSOR ADDRESS LINE POSN BIT 2	>CUR-4
5	RFN STROBE	HIGH O/P DURING LOAD O/P AFTER PAGE CLOCK GOES LOW	<KSR-N
6	PAGE MEM WR/RD SELECT'	HIGH FOR ODD LINES,LOW FOR EVEN	<MEM-26
7	PAGE MEM DISP SELECT	HIGH FOR EVEN LINES,LOW FOR ODD	<MEM-35
8	RS4	ROW SELECT TO CHAR GEN BIN 8	<MEM-15
9	ADDRESS EQUAL'	LOW WHEN CUR AND MEM ADDRESS EQUAL	<NOT USED
10	MAR RESET'	LOW FOR 50NS EVERY 1024 PAGE CLOCK CYCLES, LOADS MAR WITH 0.	<CUR-W
11	DOT CLOCK'	12.48MHZ,GATED HIGH FOR ROW LOAD	<MEM-3
12	X5	CURSOR ADDRESS CHAR POSN BCD 10	>CUR-K
13	X6	CURSOR ADDRESS CHAR POSN BCD 20	>CUR-L
14	Y1	CURSOR ADDRESS LINE POSN BIN 1	>CUR-14
15	RS2	ROW SELECT TO CHAR GEN BIN 2	<MEM-50
16	X1	CURSOR ADDRESS CHAR POSN BCD 1	>CUR-8
17	N.C.		
18	LINE BUFFER CLOCK	1.56MHZ SQUARE WAVE (T=641 NS)	<MEM-28,<CUR-C
19	INHIBIT PAGE S/R CLK'	PULL LOW TO FORCE PAGE MEMORY CLOCK HIGH	>NOT USED
20	INHIBIT PAGE CLOCK'	PULL LOW FOR DISPLAY ROLL-UP	>CUR-V
21	I/O CLOCK	156KHZ(2.564US HIGH EVERY 6.41US)	<KSR-P
22	GND	LOGIC GROUND 0.0VDC	
A	VCC	LOGIC VCC SUPPLY 5.0VDC	
B	BLINK	1SHZ SQUAREWAVE (TO BLINK CURSOR)	<MEM-30
C	LOAD'	LOW FOR 1 PERIOD OF PAGE CLOCK AFTER DELAYED STROBE RECEIVED	<CUR-16
D	LOAD BUSY'	LOW AFTER RECEIPT OF DELAYED STROBE UNTIL END OF LOAD' PULSE	<CUR-17
E	Y3	CURSOR ADDRESS LINE POSN BIN 4	>CUR-15
F	Y4	CURSOR ADDRESS LINE POSN BIN 8	>CUR-P
H	Y5	CURSOR ADDRESS LINE POSN BIN 16	>CUR-13
J	N.C.		
K	RS1	ROW SELECT TO CHAR GEN BIN 1	<MEM-52
L	LINE END	CHANGES STATE AT END OF EACH MEMORY LINE (EVERY 80 CHARS)	<CUR-21
M	CURSOR DATA	HIGH FOR 641NS DURING SCAN #9 OF LINE INDICATED BY CURSOR	<MEM-29
N	ROW LOAD'	LOW FOR 40NS AFTER COLUMN COUNT #6 UNLESS INHIBITED FOR BLANK SCAN	<MEM-27
P	DELAYED STROBE	POSITIVE EDGE DENOTES CHARACTER AVAILABLE ON CUR FOR LOADING	>CUR-19
R	X7	CURSOR ADDRESS CHAR POSN BCD 40	>CUR-9
S	RS3	ROW SELECT TO CHAR GEN BIN 4	<MEM-48
T	LINE BUFFER LOAD	HIGH FOR 51.28US,EVERY 641US	<MEM-31,<CUR-19
U	X4	CURSOR ADDRESS CHAR POSN BCD 8	>CUR-J
V	X2	CURSOR ADDRESS CHAR POSN BCD 2	>CUR-10
W	X3	CURSOR ADDRESS CHAR POSN BCD 4	>CUR-M
X	SYNC	HIGH FOR 6.41US EVERY 64.1US (HOR) HIGH FOR 256.4US EVERY 16.67MS(VT)	<MEM-21
Y	PAGE MEMORY CLOCK	DURING RECIRCULATE MODE-2.08MHZ, GATED HIGH AT BEGINING OF NEXT LINE TO BE LOADED,1.56MHZ DURING LINE BUFFER LOAD	<MEM-23
Z	GND		

COMPONENTS LAYOUT - TIM-2



COMPONENTS LIST - TIM-2

All resistors, unless otherwise noted, are ¼W, 5%.
All capacitors, unless otherwise noted, are 25V or greater.

C1	n47
C2	4n7
C3	n47
C4	n47
C5	4n7
C6	4n7
C7	4n7
C8	4n7
C9	4n7
C10	4n7
C11	4n7
C12	4n7
C13	4n7
C14	4n7
C15	4n7
C16	4n7
C17	4n7
C18	4n7
C19	4n7
C20	4n7
C21	4n7
C22	4n7
C23	4n7

R1	2K2
R2	1K5
R3	1K5
R4	1K5
R5	470
R6	220
R7	1K5
R8	1K5
R9	1K5
R10	2K2
R11	2K2
R12	2K2
R13	2K2
R14	1K5
R15	2K2
R16	1K5
R17	2K2
R18	100
R19	100

Y1	QUARTZ CRYSTAL 12.4800 MHz

ZA1	NOT USED
ZA2	74193
ZA3	74192
ZA4	74192
ZA5	74192
ZA6	7410
ZA7	8242
ZB1	7400
ZB2	7402
ZB3	7404
ZB4	7400
ZB5	7402
ZB6	74192
ZB7	8242
ZC1	NOT USED
ZC2	7410
ZC3	7474
ZC4	7400
ZC5	7404
ZC6	74193
ZC7	NOT USED
ZD1	NOT USED
ZD2	7404
ZD3	7474
ZD4	7474
ZD5	8242
ZD6	74193
ZD7	8242
ZE1	7492
ZE2	7474
ZE3	7474
ZE4	7474
ZE5	7410
ZE6	74193
ZE7	8242

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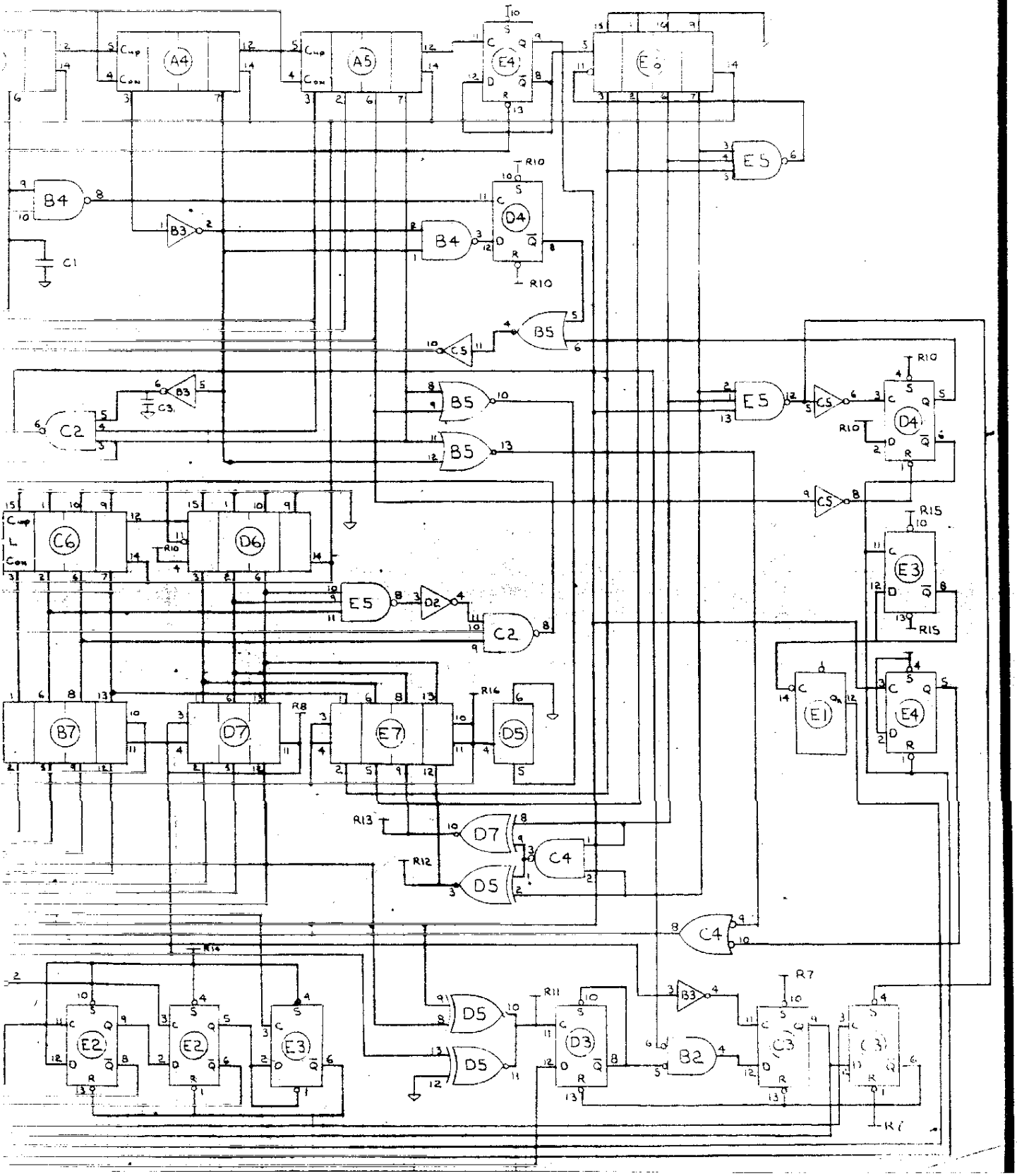

SC

TIM

TIMING BOARD

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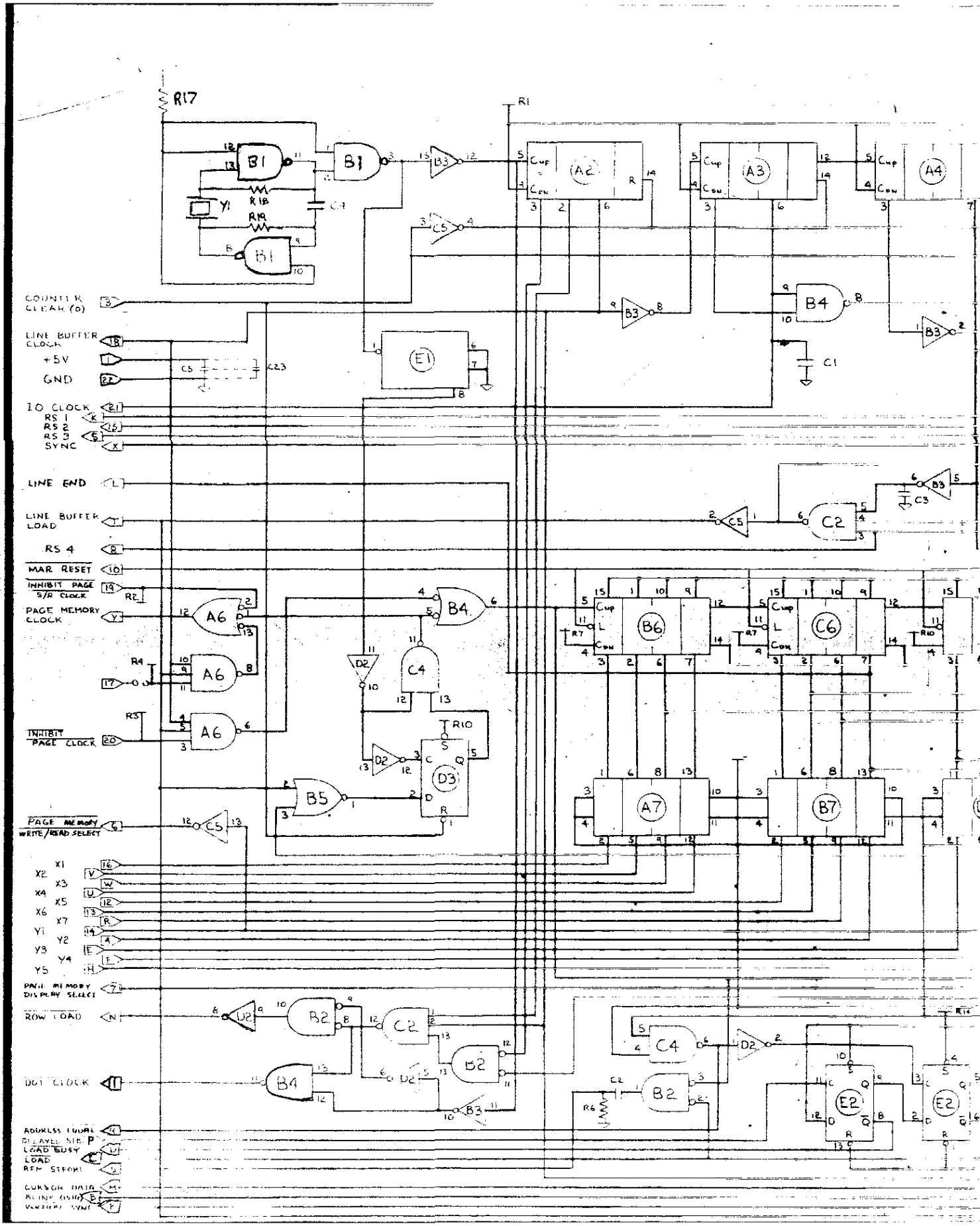


1	BOARD DATE LAST REVISION MAY 5/1/75	SHEET 1 OF 2 ORIGINAL CT 7/12/74	TIM-2-SC

MEMORY CIRCUIT CARD (MEM) SERVICE INFORMATION

THE MEMORY CARD CONTAINS THE CHARACTER STORAGE, CHARACTER GENERATION, AND VIDEO OUTPUT CIRCUITRY. THE PAGE (AS DISPLAYED) OF CHARACTERS IS STORED IN A SERIAL/PARALLEL SHIFT REGISTER ARRANGEMENT WITH A CAPACITY OF 1920 CHARACTERS.

IN UPPER-CASE ONLY TERMINALS, CHARACTER GENERATION IS PERFORMED BY A MOS ROM INSERTED IN A SOCKET ON THE MEMORY BOARD.

FOR LOWER-CASE TERMINALS, A "PIGGY-BACK" CIRCUIT BOARD IS INSERTED INTO THE SOCKET INSTEAD OF THE ROM. THE 'PIGGY-BACK" BOARD CONTAINS THE ADDITIONAL CIRCUITRY REQUIRED TO GENERATE LOWER-CASE CHARACTERS AND TO CORRECTLY POSITION THE FIVE LOWER-CASE CHARACTERS WITH DESCENDERS (I.E.TAILS). THERE ARE A NUMBER OF DIFFERENT VERSIONS OF THE PIGGY-BACK ALTHOUGH THEY ALL PERFORM ESSENTIALLY THE SAME FUNCTION.

BLOCK DIAGRAM DESCRIPTION

NEW CHARACTER SELECT

THIS SECTION CONTROLS THE RECIRCULATION OF THE PAGE MEMORY AND THE LOADING OF CHARACTERS INTO MEMORY. WHEN A CHARACTER IS TO BE LOADED FROM THE CURSOR BOARD INTO MEMORY, THE MULTIPLEXERS ROUTE THE CHARACTER INTO THE ODD OR EVEN BANK OF SHIFT REGISTERS. AT ALL OTHER TIMES THE MULTIPLEXERS RECIRCULATE THE OUTPUTS OF THE PAGE MEMORY SHIFT REGISTERS BACK INTO THEIR RESPECTIVE INPUTS.

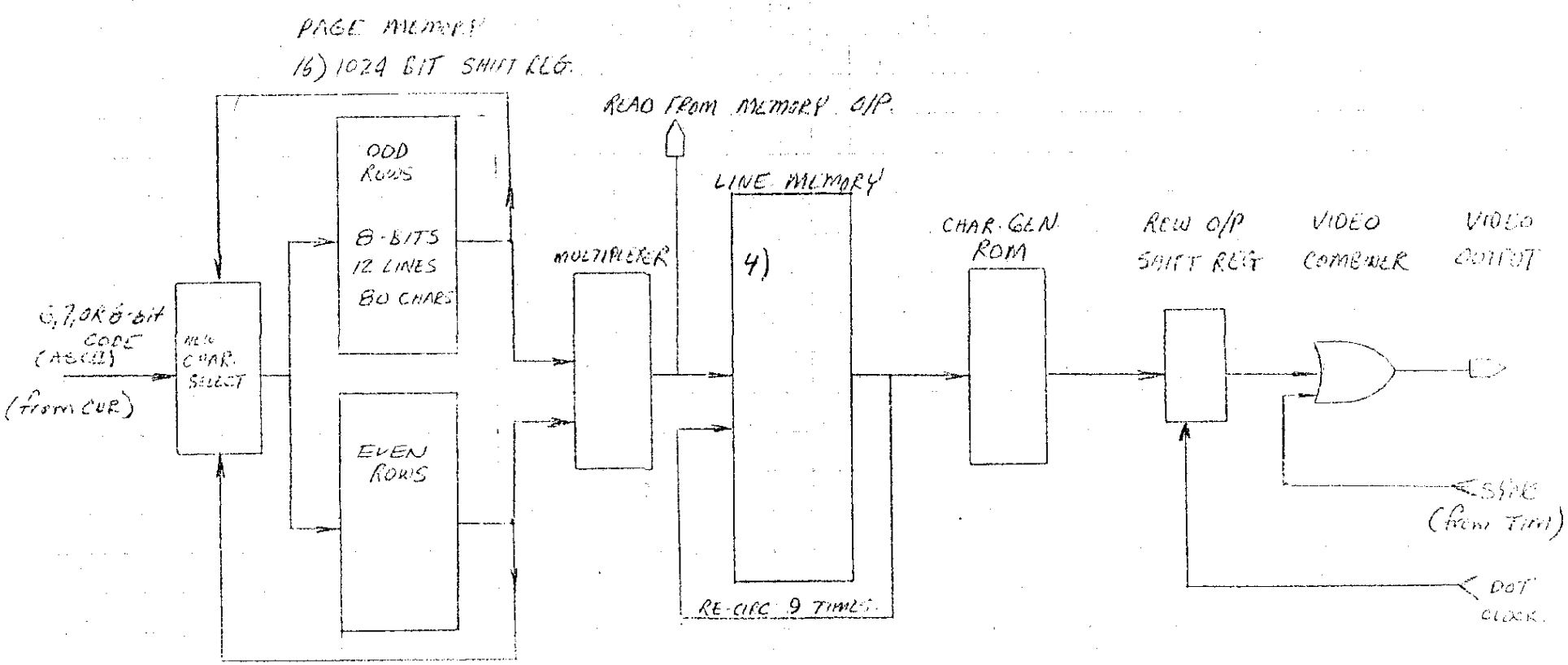
PAGE MEMORY

THE PAGE MEMORY CONSISTS OF 12 (FOR UPPER-CASE ONLY) OR 14 (FOR UPPER&LOWER-CASE) 1024 X 1 MOS SHIFT REGISTERS. THEY ARE ORGANISED INTO TWO GROUPS OF 6 OR 7. ONE GROUP IS ASSIGNED TO EVEN LINES OF CHARACTER DISPLAY AND THE OTHER GROUP IS ASSIGNED TO ODD LINES. EACH GROUP STORES 12 LINES OF 80 CHARACTERS/LINE.

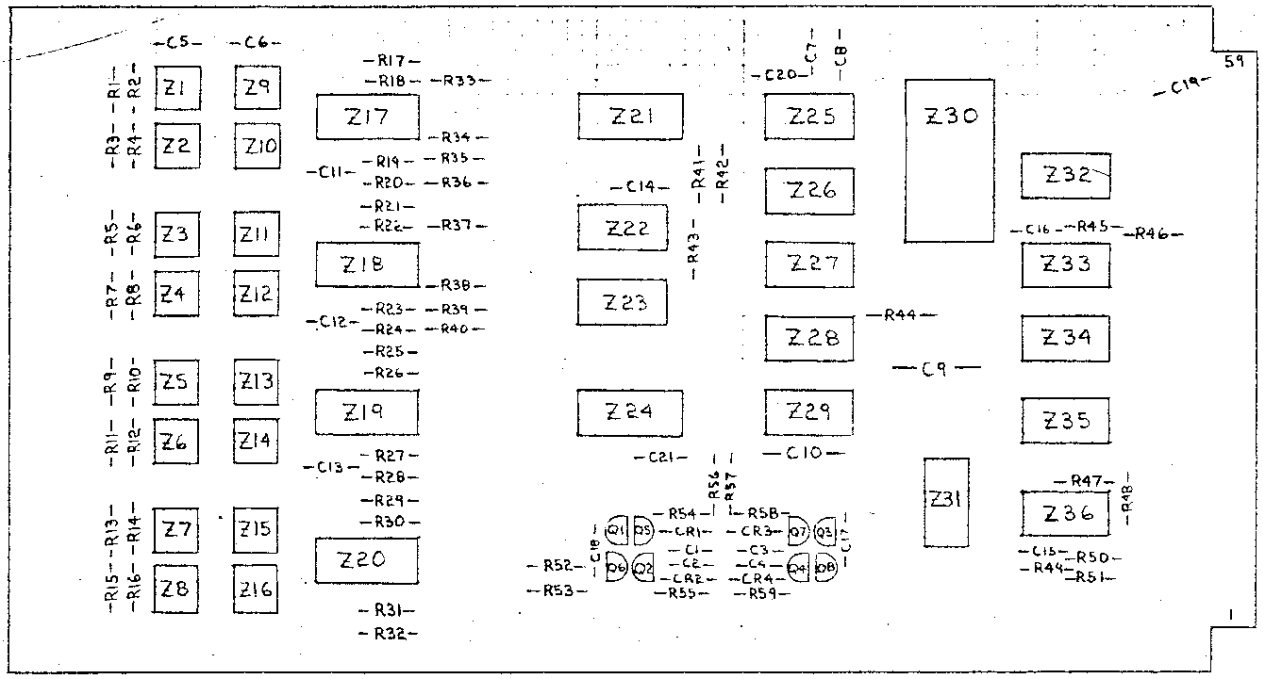
CLOCK DRIVER

THIS SECTION DERIVES A TWO-PHASE NON-OVERLAPPING CLOCK FROM THE PAGE MEMORY CLOCK SIGNAL RECEIVED FROM THE TIMING BOARD. THE GROUPS OF TRANSISTORS IN THIS SECTION PROVIDE THE LEVEL SHIFTING AND A LOW IMPEDANCE SOURCE TO DRIVE THE LARGE CPACITIVE LOAD (APPROX.2000PF) PRESENTED BY THE SHIFT REGISTERS.

MEMORY PCB. MEM-1



COMPONENTS LAYOUT - MEM-1



COMPONENTS LIST - MEM-1

All resistors, unless otherwise noted, are ¼W, 5%.
All capacitors, unless otherwise noted, are 25V or greater.

C1	n22	Q7	2N4401	R30	3K3	Z2	2504	
C2	n22	Q8	2N4401	R31	3K3	Z3	2504	
C3	n22			R32	3K3	Z4	2504	
C4	n22			R33	3K3	Z5	2504	
C5	22uF	R1	3K3	R34	3K3	Z6	2504	(VC 44)
C6	22uF	R2	3K3	R35	3K3	Z7	2504	
C7	22uF	R3	3K3	R36	3K3	Z8	NOT USED	
C8	22uF	R4	3K3	R37	3K3	Z9	2504	
C9	22uF	R5	3K3	R38	3K3	Z10	2504	
C10	22uF	R6	3K3	R39	3K3	Z11	2504	
C11	4n7	R7	3K3	R40	3K3	Z12	2504	
C12	4n7	R8	3K3	R41	3K3	Z13	2504	
C13	4n7	R9	3K3	R42	3K3	Z14	2504	(VC 44)
C14	4n7	R10	3K3	R43	3K3	Z15	2504	
C15	4n7	R11	3K3	R44	3K3	Z16	NOT USED	
C16	4n7	R12	3K3	R45	3K3	Z17	93L22	
C17	4n7	R13	3K3	R46	3K3	Z18	93L22	
C18	4n7	R14	3K3	R47	3K3	Z19	93L22	
C19	4n7	R15	3K3	R48	27	Z20	93L22	
C20	4n7	R16	3K3	R49	100	Z21	74157	
C21	4n7	R17	3K3	R50	270	Z22	7474	
		R18	3K3	R51	3K3	Z23	7400	
		R19	3K3	R52	10	Z24	74157	
CR1	1N4148	R20	3K3	R53	10	Z25	2510	
CR2	1N4148	R21	3K3	R54	27	Z26	2510	
CR3	1N4148	R22	3K3	R55	27	Z27	2510	
CR4	1N4148	R23	3K3	R56	470	Z28	2510	(VC 44)
		R24	3K3	R57	470	Z29	7400	
		R25	3K3	R58	27	Z30	2513 CM2140 (VC 33)	
Q1	2N4403	R26	3K3	R59	27		6061D + PIGGY-BACK(VC44)	
Q2	2N4403	R27	3K3			Z31	7402	
Q3	2N4403	R28	3K3			Z32	7495	
Q4	2N4403	R29	3K3	Z1	2504	Z33	7495	Z35 7404
Q5	2N4401					Z34	7400	Z36 8242
Q6	2N4401							

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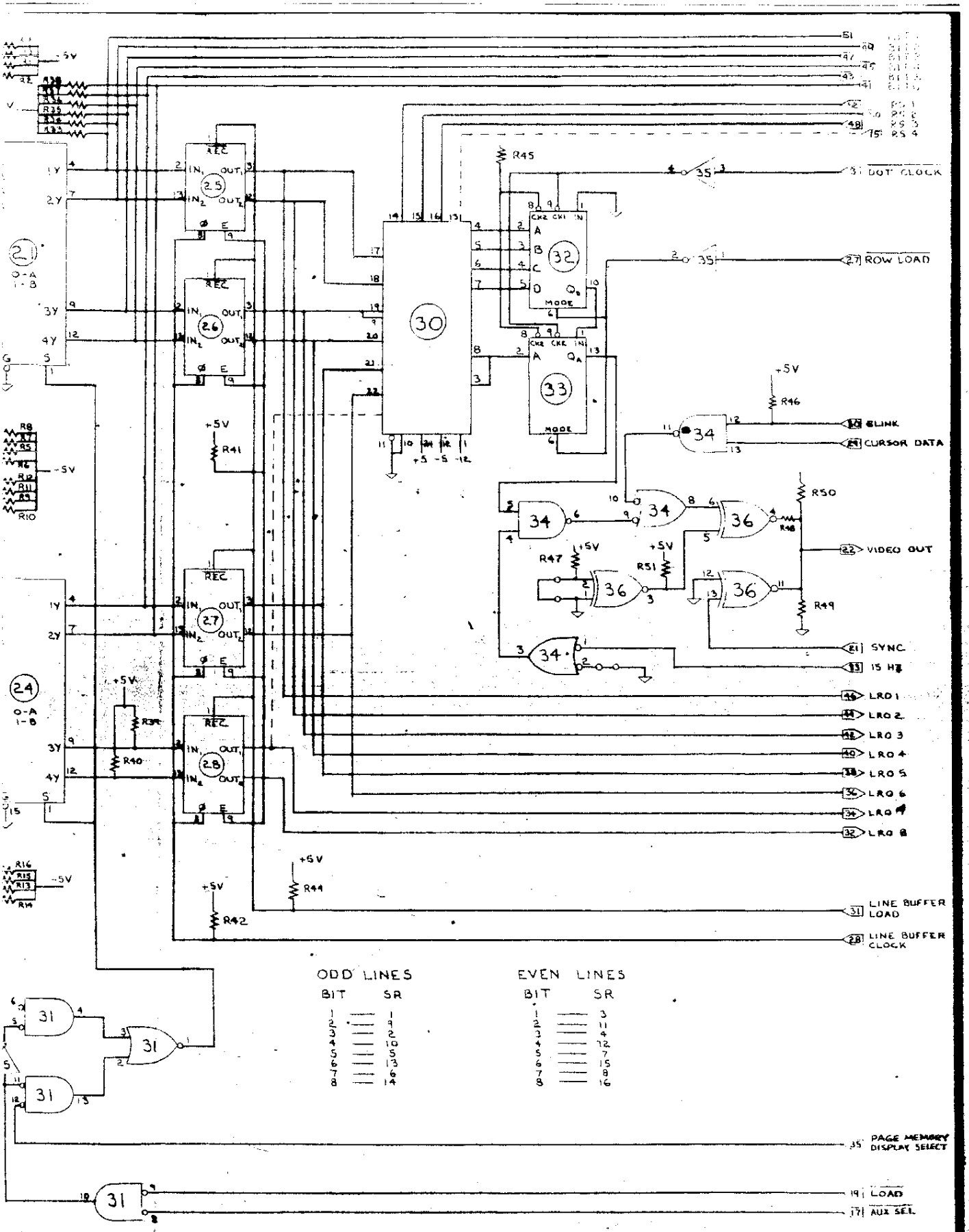

ODD LINES

BIT	SR
1	1
2	9
3	2
4	10
5	5
6	13
7	6
8	14

EVEN LINES

BIT	SR
1	3
2	11
3	4
4	12
5	7
6	15
7	8
8	16

MEM

MEMORY BOARD

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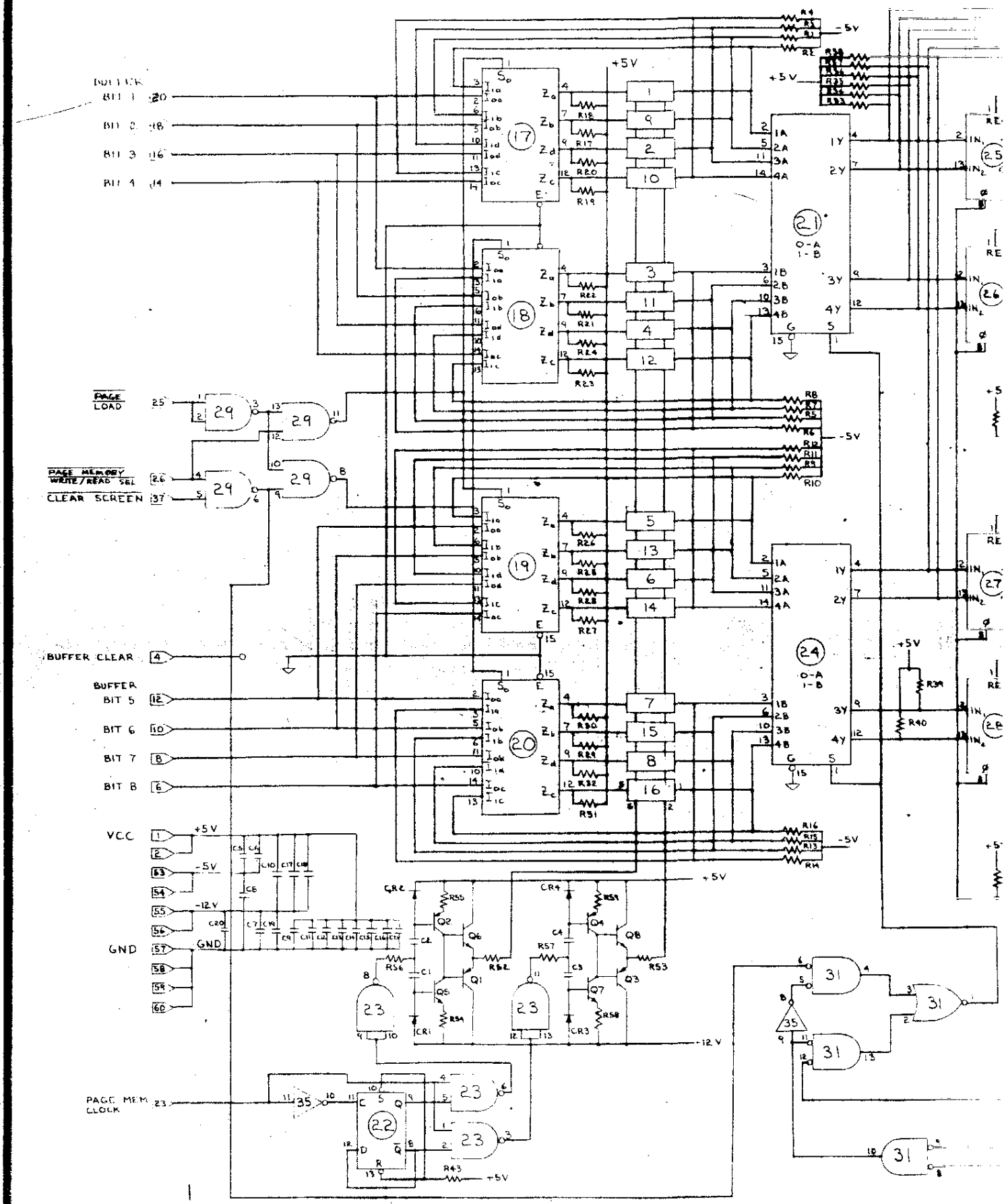
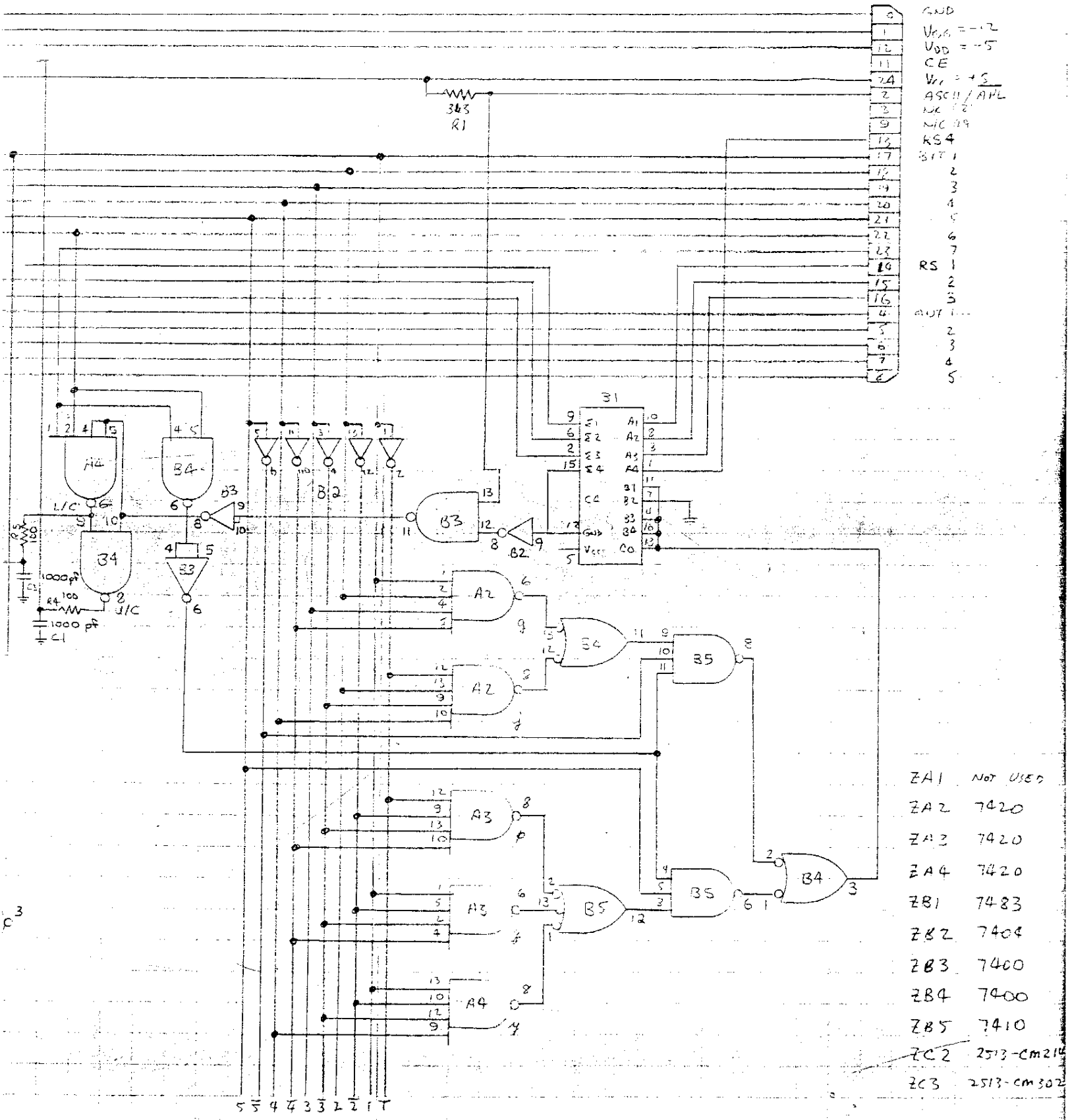


1	BOARD DATE	SHEET 1 OF 2	MEM-1-SC
	LAST REVISION DAY 25/02/75	ORIGINAL CT 17/10/74	



ZA1	NOT USED
ZA2	7420
ZA3	7420
ZA4	7420
ZB1	7483
ZB2	7404
ZB3	7400
ZB4	7400
ZB5	7410
~~ZC2~~	2513-CM216
ZC3	2513-CM302

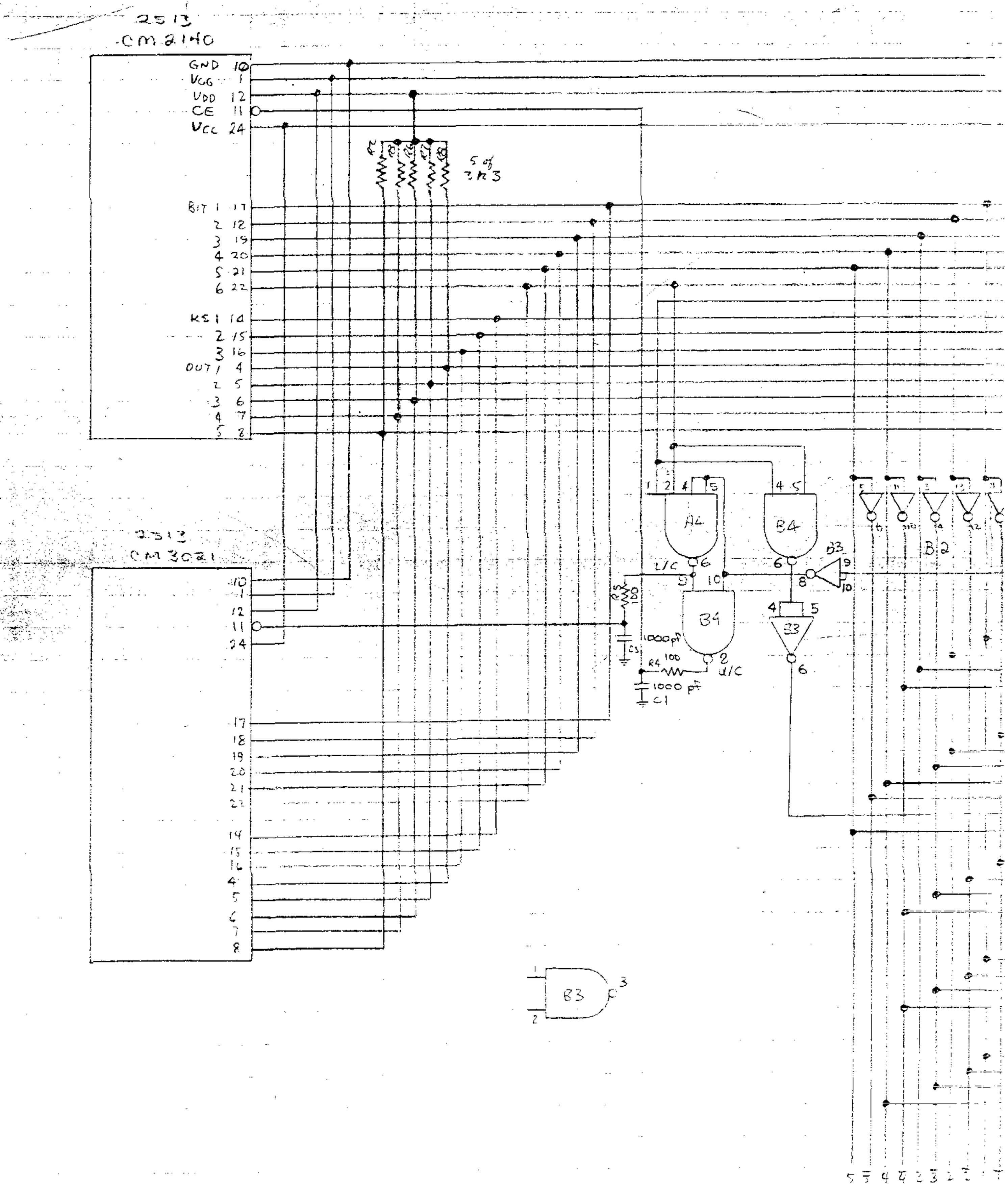
C3

C11 PIGGY-BACK BOARD FOR 2513's

CR-4

20 NOV 74 DAY

R1 27 DEC 74 R2 4 MAR 75



DESCENDED ASCII PIGGY-BACK BOARD