# CPU BOARD
## TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>SUBJECT</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>KIT CONTENTS</td>
<td>2</td>
</tr>
<tr>
<td>CIRCUIT DIAGRAM</td>
<td></td>
</tr>
<tr>
<td>PARTS LAYOUT</td>
<td></td>
</tr>
<tr>
<td>TOOLS AND MATERIALS REQUIRED FOR ASSEMBLY</td>
<td>3</td>
</tr>
<tr>
<td>SOLDERING TECHNIQUE</td>
<td>4</td>
</tr>
<tr>
<td>REMOVAL OF MULTI-PIN SOLDERED-IN PARTS</td>
<td></td>
</tr>
<tr>
<td>PREPARATION FOR ASSEMBLY</td>
<td>5</td>
</tr>
<tr>
<td>ASSEMBLY SEQUENCE</td>
<td></td>
</tr>
<tr>
<td>RESISTORS</td>
<td>6</td>
</tr>
<tr>
<td>DIODE</td>
<td></td>
</tr>
<tr>
<td>CRYSTAL</td>
<td></td>
</tr>
<tr>
<td>AXIAL ELECTROLYTIC CAPACITORS</td>
<td></td>
</tr>
<tr>
<td>SOCKETS</td>
<td></td>
</tr>
<tr>
<td>DISC CAPACITORS</td>
<td>7</td>
</tr>
<tr>
<td>REGULATORS AND HEATSINK</td>
<td></td>
</tr>
<tr>
<td>PRELIMINARY TESTS</td>
<td></td>
</tr>
<tr>
<td>INTEGRATED CIRCUITS</td>
<td>8</td>
</tr>
<tr>
<td>FUNCTIONAL DESCRIPTION</td>
<td>9</td>
</tr>
<tr>
<td>S-100 BUS LISTING</td>
<td>10, 11</td>
</tr>
<tr>
<td>STATUS SIGNAL DEFINITIONS</td>
<td>12</td>
</tr>
<tr>
<td>ACKNOWLEDGE AND CONTROL SIGNALS</td>
<td>13</td>
</tr>
<tr>
<td>S-100 BUS DISABLE SIGNALS</td>
<td></td>
</tr>
<tr>
<td>JUMPER INSTALLATION</td>
<td></td>
</tr>
<tr>
<td>USERS GUIDE</td>
<td>14</td>
</tr>
<tr>
<td>PRIORITY INTERRUPT DEMONSTRATION PROGRAM</td>
<td></td>
</tr>
<tr>
<td>REAL TIME CLOCK DEMONSTRATION PROGRAM</td>
<td>15</td>
</tr>
<tr>
<td>TROUBLE SHOOTING GUIDE</td>
<td>16</td>
</tr>
<tr>
<td>WARRANTY</td>
<td></td>
</tr>
</tbody>
</table>
INTRODUCTION

THE VECTOR GRAPHIC INC. CENTRAL PROCESSOR UNIT (CPU) PROVIDES ALL THE CENTRAL PROCESSING AND LOGIC FUNCTIONS FOR YOUR MICROCOMPUTER SYSTEM. THE HEART OF THIS BOARD IS THE 8080A LSI MICROPROCESSOR, COUPLED WITH THE SINGLE LSI CHIP ARE VARIOUS PERIPHERAL CIRCUITS TO PERFORM TIMING, CONTROL, BUS INTERFACE, AND POWER SUPPLY REGULATION TO OBTAIN A RELIABLE AND VERSATILE CPU.

ESPECIALLY USEFUL FEATURES OF THE VECTOR GRAPHIC CPU ARE THE B LEVEL VECTORED PRIORITY INTERRUPT CIRCUITS AND A REAL TIME CLOCK. PROVISION OF A REAL TIME CLOCK ALLOWS FOR SOPHISTICATED TIMING AND CONTROL FUNCTIONS ONLY FOUND IN ADVANCED INDUSTRIAL MINICOMPUTERS. A PROGRAMMABLE PRIORITY INTERRUPT STRUCTURE ALLOWS THE USER TO ASSIGN DIFFERENT LEVELS OF PRIORITIES OR IMPORTANCE OF THE INTERRUPT INPUTS TO THE MICROCOMPUTER. ASSIGNMENT OF PRIORITY LEVEL IS FULLY PROGRAMMABLE ALLOWING FOR ADAPTIVE OPERATION UNDER PROGRAM CONTROL.

ALL INTERFACE BETWEEN THE CPU BOARD AND THE STANDARD S-100 BUS ARE FULLY BUFFERED FOR ISOLATION AND RELIABLE OPERATION.

A STABLE CLOCK FOR THE 8080A IS PROVIDED BY A CRYSTAL CONTROLLED OSCILLATOR AND CLOCK DRIVER. THIS INSURES OPERATION OF THE 8080A WITHIN THE MANUFACTURERS SPECIFICATIONS FOR TROUBLE FREE OPERATION.

CAREFUL ATTENTION TO GOOD DESIGN PRACTICE PROVIDES USER WITH A CPU GUARANTEED TO OPERATE RELIABLY WITHOUT CONSTANT ADJUSTMENT AND MAINTENANCE.

ASSEMBLY INSTRUCTIONS

! CAUTION !

THE 8080A MICROPROCESSOR IS A MOS DEVICE AND THEREFORE SENSITIVE TO ELECTROSTATIC DISCHARGE. HANDLING OF THIS DEVICE SHOULD BE MINIMIZED AND IT SHOULD BE STORED IN THE PROTECTIVE HOLDER RECEIVED WITH THIS KIT.

COMMON SENSE PRECAUTION ON THE PART OF THE KIT BUILDER SHOULD BE EXERCISED TO ELIMINATE ANY EXCESSIVE ELECTROSTATIC CHARGES.
<table>
<thead>
<tr>
<th>QUANTITY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PRINTED CIRCUIT BOARD</td>
</tr>
<tr>
<td>1</td>
<td>8080A CENTRAL PROCESSOR A4</td>
</tr>
<tr>
<td>2</td>
<td>8212 8 BIT LATCH B6, C7</td>
</tr>
<tr>
<td>1</td>
<td>8214 PRIORITY INTERRUPT CONTROL UNIT C1</td>
</tr>
<tr>
<td>1</td>
<td>8224 CLOCK GENERATOR A5</td>
</tr>
<tr>
<td>9</td>
<td>8097/74367 HIGH SPEED HEX BUFFER INVERTERS A3, A8, B3, B4, B5, B7, C3, C4, C6</td>
</tr>
<tr>
<td>1</td>
<td>74LS02 QUADRUPLE 2-INPUT POSITIVE NOR GATE A2</td>
</tr>
<tr>
<td>2</td>
<td>74LS04 HEX INVERTER A8, C2</td>
</tr>
<tr>
<td>1</td>
<td>74LS74 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP B1</td>
</tr>
<tr>
<td>1</td>
<td>74LS00 QUADRUPLE 2-INPUT POSITIVE NAND GATE B2</td>
</tr>
<tr>
<td>1</td>
<td>74LS30 8-INPUT POSITIVE NAND GATE C5</td>
</tr>
<tr>
<td>1</td>
<td>7805 REGULATOR</td>
</tr>
<tr>
<td>1</td>
<td>79105 REGULATOR</td>
</tr>
<tr>
<td>1</td>
<td>78L12 REGULATOR</td>
</tr>
<tr>
<td>2</td>
<td>25 MFD 12V CAPACITORS</td>
</tr>
<tr>
<td>1</td>
<td>0.001 MFD 1000V CERAMIC DISC CAPACITOR</td>
</tr>
<tr>
<td>11</td>
<td>0.1 MFD 10V CERAMIC DISC CAPACITORS</td>
</tr>
<tr>
<td>2</td>
<td>150 PF 1000V CERAMIC DISC CAPACITORS</td>
</tr>
<tr>
<td>1</td>
<td>10 PF 600V CERAMIC DISC CAPACITORS</td>
</tr>
<tr>
<td>2</td>
<td>4.7 MFD 50V ELECTROLYTIC CAPACITORS</td>
</tr>
<tr>
<td>2</td>
<td>27 OHM 1 WATT RESISTORS (BANDS OF RED, VIOLET, BLACK)</td>
</tr>
<tr>
<td>33</td>
<td>1K 1/4 WATT RESISTORS (BANDS OF BROWN, BLACK, RED)</td>
</tr>
<tr>
<td>2</td>
<td>47K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, ORANGE)</td>
</tr>
<tr>
<td>9</td>
<td>4.7K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, RED)</td>
</tr>
<tr>
<td>1</td>
<td>15K 1/4 WATT RESISTOR (BANDS OF BROWN, GREEN, ORANGE)</td>
</tr>
<tr>
<td>1</td>
<td>100 OHM 1/4 WATT RESISTOR (BANDS OF BROWN, BLACK, BROWN)</td>
</tr>
<tr>
<td>1</td>
<td>18 MHZ CRYSTAL</td>
</tr>
<tr>
<td>1</td>
<td>1N270 DIODE</td>
</tr>
<tr>
<td>1</td>
<td>LM358 OP-AMP</td>
</tr>
<tr>
<td>1</td>
<td>HEATSINK</td>
</tr>
<tr>
<td>1</td>
<td>40 PIN SOCKET</td>
</tr>
<tr>
<td>3</td>
<td>24 PIN SOCKETS</td>
</tr>
<tr>
<td>11</td>
<td>16 PIN SOCKETS</td>
</tr>
<tr>
<td>5</td>
<td>14 PIN SOCKETS</td>
</tr>
<tr>
<td>1</td>
<td>8 PIN SOCKET</td>
</tr>
<tr>
<td>1</td>
<td>#6-32 x 3/8 SCREW, NUT AND LOCK WASHER</td>
</tr>
</tbody>
</table>
## TOOLS AND MATERIALS REQUIRED FOR ASSEMBLY

The following minimum set of tools and materials is required for the assembly of Vector Graphic Inc. kits:

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volt - Ohmmeter</td>
<td>Inexpensive</td>
</tr>
<tr>
<td>Screwdriver - Straight Slot</td>
<td>For #5 and #8 screws</td>
</tr>
<tr>
<td>Screwdriver - Phillips Head*</td>
<td>For #8 screws</td>
</tr>
<tr>
<td>Cutters - Diagonal</td>
<td>4&quot;, Flush Cutting</td>
</tr>
<tr>
<td>Pliers - Needle Noosed</td>
<td>6&quot;</td>
</tr>
<tr>
<td>Pliers - Regular</td>
<td>Medium</td>
</tr>
<tr>
<td>Wire Stripper</td>
<td>For 8 AWG to 20 AWG</td>
</tr>
<tr>
<td>Soldering Iron</td>
<td>30 Watts maximum with chisel tip</td>
</tr>
<tr>
<td>Solder</td>
<td>.030 ga 60/40 tin-lead rosin core</td>
</tr>
<tr>
<td>Sponge</td>
<td>For cleaning soldering iron</td>
</tr>
<tr>
<td>Pen Knife</td>
<td>Or 'X-Acto' Knife</td>
</tr>
<tr>
<td>Cleaning Solvent</td>
<td>Trichloroethane or isopropyl alcohol. Do not use acetone</td>
</tr>
<tr>
<td>Cardboard</td>
<td>To protect table top during soldering</td>
</tr>
<tr>
<td>Heat Sink Grease</td>
<td>Or high temperature plumbers grease</td>
</tr>
<tr>
<td>Ruler*</td>
<td>To measure wire lengths</td>
</tr>
</tbody>
</table>

*Note: Required for mainframe cabinet assembly only
SOLDERING TECHNIQUE

THE SOLDER
USE A #20 GAUGE (.030") ROsin CORE SOLDER WITH A RATIO OF AT LEAST 60% TIN AND 40% LEAD. "KESTER" AND "ERSON" ARE TWO DEPENDABLE BRANDS OF SOLDER. ACID CORE SOLDERS OR ACID FLUX MUST NOT BE USED AS THEY WILL CORRODE THE PRINTED CIRCUIT BOARD.

THE SOLDERING IRON
USE A SMALL, 30 WATT MAXIMUM IRON WITH A SMALL, CHISEL SHAPED TIP. TOO MUCH HEAT WILL DAMAGE BOTH COMPONENTS AND BOARDS. SOLDERING GUNS ARE TOO HOT AND SHOULD NOT BE USED.

HEAT THE IRON, WIPE ITS TIP QUICKLY ON THE DAMP SPONGE, AND APPLY A TINY AMOUNT OF SOLDER TO THE TIP - JUST ENOUGH TO MAKE IT SILVER IN COLOR BUT NOT SO MUCH THAT IT WILL DRIP OFF. THIS CLEANING PROCEDURE SHOULD BE REPEATED WHENEVER THE TIP OF THE SOLDERING IRON BEGINS TO TAKE ON A BROWNISH COLOR.

THE PROCEDURE
THE ENTIRE SOLDERING OPERATION SHOULD TAKE LITTLE MORE THAN TWO SECONDS PER JOINT. THE SEQUENCE IS AS FOLLOWS:

TOUCH THE TIP OF THE SOLDERING IRON TO THE JOINT, AS SHOWN BELOW, SO THAT BOTH CONDUCTORS TO BE JOINED ARE SIMULTANEOUSLY HEATED SUFICIENTLY TO MELT THE SOLDER.

TOUCH THE SOLDER TO THE JOINT, AS SHOWN ABOVE, JUST LONG ENOUGH TO MELT ENOUGH SOLDER TO FORM A FILLET ON THE JOINT. TOO MUCH SOLDER MAY SHORT CIRCUIT THE BOTTOM OF THE BOARD OR FLOW THROUGH THE HOLES AND INTO THE SOCKETS. THE MELTED SOLDER WILL APPEAR WET AND SHINY. IT WILL QUICKLY FLOW COMPLETELY AROUND THE WIRE AND OVER THE SURFACE TO WHICH THE WIRE IS ATTACHED.

REMOVE THE SOLDERING IRON AS SOON AS BOTH SURFACES HAVE BEEN COMPLETELY WETTED. REMEMBER, THE TOTAL TIME FROM APPLICATION TO REMOVAL OF THE SOLDERING IRON SHOULD BE ONLY TWO OR THREE SECONDS. REMOVAL OF THE SOLDERING IRON TOO SOON MAY RESULT IN A COLD SOLDER JOINT AND LEAVING THE SOLDERING IRON IN CONTACT TOO LONG MAY CAUSE HEAT DAMAGE TO EITHER THE COMPONENTS OR THE BOARD.

REMOVAL OF MULTI-PIN SOLDERED-IN PARTS

CAUTION
IF FOR ANY REASON, IT BECOMES NECESSARY TO REMOVE A SOLDERED-IN PART HAVING MORE THAN JUST TWO LEADS, DO NOT TRY TO REMOVE THE PART INTACT. IT CAN BE DONE BUT ONLY WITH RISK OF DAMAGING THE PRINTED CIRCUIT BOARD IN THE PROCESS.

HOLD THE PRINTED CIRCUIT BOARD IN A PADDED VISE TO AVOID DAMAGE.

REMOVAL OF SOLDERED-IN IC SOCKETS


CLEAR THE HOLES OF ANY EXCESS SOLDER USING A SOLDER SUCKER OR WICK.
REMOVAL OF SOLDERED-IN INTEGRATED CIRCUIT CHIPS
CUT EACH PIN WITH A PAIR OF DIAGONAL CUTTERS AT A POINT BETWEEN THE CHIP AND THE PRINTED CIRCUIT BOARD WHICH IS AS CLOSE TO THE CHIP AS POSSIBLE SO THAT THERE IS ENOUGH OF THE PIN SHOWING ABOVE THE BOARD TO BE GRASPED BY NEEDLE NOSED PLIERS WHILE REMOVING AS DESCRIBED ABOVE.

PREPARATION FOR ASSEMBLY

WORKING AREA AND TOOLS
A WELL LIGHTED, CLEAN TABLE OR WORK BENCH AND THE PROPER TOOLS AND MATERIALS ARE MOST IMPORTANT FOR PRODUCING TROUBLE FREE ASSEMBLIES. THE WORK SURFACE SHOULD BE CLEAN AND FREE OF ALL ITEMS EXCEPT FOR THE TOOLS AND KIT COMPONENTS BEING USED. A CLEAN PIECE OF CARDBOARD OR HAND TOWEL IS SUGGESTED TO PROTECT THE TABLE TOP WHEN SOLDERING.

CHECK KIT CONTENTS
VERIFY THE CONTENTS OF YOUR KIT AGAINST THE KIT CONTENTS LIST IN THE FRONT OF THIS MANUAL. CHECK EACH PART VISUALLY FOR DAMAGE IN SHIPPING. IF THERE ARE ANY MISSING OR DAMAGED ITEMS, PLEASE NOTIFY THE DEALER FROM WHOM YOU BOUGHT YOUR KIT IMMEDIATELY. THERE MAY BE SLIGHT VARIATIONS FROM THE PARTS SPECIFIED, BUT THE COMPONENTS SHOULD BE FUNCTIONALLY EQUIVALENT.

PARTS LAYOUT AND ASSEMBLY SEQUENCE
THE FRONT OF THE BOARD IS THE SIDE ON WHICH THE PARTS LAYOUT HAS BEEN SILK SCREENED. ALL PARTS WILL BE ON THE FRONT OF THE PRINTED CIRCUIT BOARD. THEIR LEADS OR PINS WILL PASS THROUGH THE BOARD AND BE SOLDERED ON THE REAR.

PLACE THE BOARD WITH ITS FRONT SIDE UP AND THE GOLD EDGE CONTACTS NEAREST YOU. IN THAT POSITION, WE WILL REFER TO THE UPPER PORTION OF THE BOARD AS BEING FURTHEST AWAY FROM YOU.

SHOULD YOU USE SOCKETS?
WE RECOMMEND THE USE OF SOCKETS FOR TWO REASONS. ONE IS THAT SOLDERED-IN CHIPS CANNOT BE RETURNED FOR REPLACEMENT. ANOTHER IS THAT, SHOULD YOU HAVE TO REPLACE A CHIP, IT IS POSSIBLE TO DO CONSIDERABLE DAMAGE TO THE P. C. BOARD, UNLESS YOU ARE EXPERIENCED AT IC REMOVAL AND HAVE THE PROPER TOOLS.

CPU BOARD ASSEMBLY SEQUENCE

INSERTION OF RESISTORS
ORIENTATION IS OF NO CONCERN WITH RESISTORS, BUT BE SURE THAT THE STRIPED COLOR CODE WHICH IDENTIFIES THE RESISTANCE VALUE IS AS SHOWN BELOW FOR THE PARTICULAR LOCATION.

FIRST 3 COLOR BANDS IDENTIFIED ABOVE

33 1K 1/4 WATT RESISTORS (BANDS OF BROWN, BLACK, RED)
9 4.7K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, RED)
2 47K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, ORANGE)
1 15K 1/4 WATT RESISTOR (BANDS OF BROWN, GREEN, ORANGE)
1 100 OHM 1/4 WATT RESISTOR (BANDS OF BROWN, BLACK, BROWN)
2 27 OHM, 1 WATT RESISTORS (BANDS OF RED, VIOLET, BLACK)
DIODE
INSTALL THE 1N270 DIODE AS INDICATED ON THE ASSEMBLY DRAWING AND SOLDER. OBSERVE CORRECT POLARITY!!

CRYSTAL
MEASURE AND BEND THE LEADS OF THE CRYSTAL. INSTALL THE CRYSTAL AS SHOWN ON THE ASSEMBLY DRAWING AND SOLDER. TIGHTLY LOOP A PIECE OF BARE HOOK UP WIRE OVER THE CRYSTAL AND INSTALL IN 2 HOLES ON EACH SIDE OF THE CRYSTAL. SOLDER THE WIRE IN PLACE.

AXIAL ELECTROLYTIC CAPACITORS
AGAIN REFERING TO THE COMPONENT PLACEMENT DIAGRAM, INSERT THE AXIAL ELECTROLYTIC CAPACITORS AND SOLDER IN PLACE IN THE SAME MANNER AS DESCRIBED FOR RESISTORS.

2 25 MFD 12V CAPACITORS
2 4.7 MFD 50V CAPACITORS

SOCKETS
PLACE THE PRINTED CIRCUIT BOARD (PCB) WITH THE VECTOR GRAPHIC INC. FACING DOWN, AND THE COMPONENT SIDE UP ON TOP OF THE TERRY CLOTH TOWEL. INSTALL THE SOCKETS WITH THE PIN 1 INDEX (TRIANGLE FILL IN) ON THE PCB IN THE FOLLOWING SEQUENCE. DO NOT SOLDER!

1 40 PIN SOCKET
3 24 PIN SOCKETS
11 16 PIN SOCKETS
5 14 PIN SOCKETS
1 8 PIN SOCKET

INSURE THAT NO 14 PIN SOCKETS ARE MISTAKENLY INSTALLED IN THE 16 PIN POSITIONS.

SOLDERING SOCKETS
ON EACH SOCKET, SOLDER TWO CORNER PINS THAT ARE DIAGONALLY OPPOSITE EACH OTHER. TOUCH THE PIN AND PAD WITH THE IRON TIP ALLOWING ENOUGH SOLDER TO FLOW TO FORM A RILLET BETWEEN PIN AND PAD. AFTER DOING THIS TO ALL SOCKETS, RETURN TO THE FIRST AND SOLDER ALL PINS. USE A MINIMUM OF SOLDER TO AVOID SOLDER BRIDGES [SHORTS]. AFTER ALL THE SOCKETS ARE CORRECTLY INSTALLED HOLD THE BOARD UP AND SIGHT ALONG THE SOCKETS TO BE SURE THAT THE PINS ARE PROPERLY SEATED. PLACE THE STIFF CARDBOARD OR MAGAZINE ON TOP OF THE SOCKETS TO HOLD THEM IN PLACE AND TURN THE BOARD OVER AND PLACE IT ON THE TOWEL. NOW PROCEED TO SOLDER ALL PINS ON THE SOCKETS.

INSERTION OF DISC CAPACITORS
DISC CAPACITORS DO NOT REQUIRE SPECIAL ORIENTATION. HOWEVER, THEY OFTEN HAVE THEIR COATING EXTENDING DOWN FROM THEIR BODY ALONG THEIR LEADS. IF TOO FAR ALONG THE LEAD, IT MAY BE CRACKED OFF BY SQUEEZING IT WITH PLIERS. IN ANY EVENT, BE SURE THAT THIS INSULATIVE COATING DOES NOT EXTEND INTO THE PRINTED CIRCUIT BOARD HOLE.

INSERT THE LEADS OF THE 15 DISC CAPACITORS THROUGH THE PROPER HOLES AS INDICATED ON THE PARTS LAYOUT. BEND THE LEADS SLIGHTLY OUTWARD TO HOLD THE CAPACITOR IN POSITION WHILE SOLDERING. THE DISC CAPACITORS SHOULD BE SPACED UNIFORMLY ABOVE THE PRINTED CIRCUIT BOARD ABOUT 1/16" SO AS TO GIVE A NEAT APPEARANCE OF THE FINISHED BOARD. SOLDER IN PLACE WHILE HOLDING IN THIS POSITION.
CERAMIC DISC
REFFERING TO THE COMPONENT PLACEMENT DIAGRAM, BEND THE LEADS AND INSTALL THE DISC CAPACITORS IN THE FOLLOWING SEQUENCE AND SOLDER

<table>
<thead>
<tr>
<th>Qty</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>0.1 MFD 10V CAPACITORS</td>
</tr>
<tr>
<td>2</td>
<td>150 PF 1000V CAPACITORS</td>
</tr>
<tr>
<td>1</td>
<td>10 PF 600V CAPACITOR</td>
</tr>
<tr>
<td>1</td>
<td>0.001 1000V MFD CAPACITOR</td>
</tr>
</tbody>
</table>

APPROX. 1/16" P.C. BOARD

INSPECT FOR PROPER LOCATION AND FOR PROPER SOLDER JOINTS, AND THEN CLIP OFF EXCESS LEAD LENGTH WITH DIAGONAL CUTTER.

REGULATORS AND HEATSINK

NEXT INSTALL THE +12V AND -5V REGULATORS AS INDICATED ON THE ASSEMBLY DRAWING. OBSERVE CORRECT ORIENTATION OF THE DEVICES.

PRELIMINARY TESTS
FIRST INSTALL ALL OF THE INTEGRATED CIRCUITS WITH 14 OR 16 PINS. APPLY POWER TO THE BOARD BY PLUGGING IT INTO YOUR COMPUTER OR BY CONNECTING IT TO A SUITABLE POWER SUPPLY AND MEASURE THE REGULATED OUTPUT OF EACH REGULATOR. IF LESS THAN +4.75, -4.75, VOLTS IS MEASURED, CHECK FOR A SHORT CIRCUIT. CAUTION! SHORTED REGULATORS SOMETIMES EXPLODE - STAY CLEAR OF THE REGULATOR SIDE OF THE BOARD WHILE TESTING IT. IF MORE THAN +5.25, -5.25, OR +12.6 VOLTS IS MEASURED, THE REGULATOR MAY BE BAD.

DO NOT CONTINUE WITHOUT MAKING THE FOLLOWING TEST. FAILURE TO DO SO COULD RUIN YOUR WHOLE DAY!

NEXT CHECK PIN 20 OF THE 40 PIN SOCKET FOR +5V, PIN 11 FOR -5V AND PIN 28 FOR +12V. FAILURE TO READ THESE VOLTAGES INDICATES MOST PROBABLY A SOLDER SHORT OR BROKEN RUN ON THE PCB.
ORIENTATION OF INTEGRATED CIRCUIT CHIPS
CARE MUST BE TAKEN TO INSURE THAT EACH INTEGRATED CIRCUIT CHIP IS SO ORIENTED, PRIOR TO INSERTION IN ITS SOCKET, THAT PIN #1 IS AT THE LOCATION SO DESIGNATED ON THE PRINTED CIRCUIT BOARD OR IN THE INDIVIDUAL ASSEMBLY INSTRUCTIONS FOR THE KIT.

PIN #1 IS, UNFORTUNATELY, DESIGNATED IN A VARIETY OF WAYS DEPENDING UPON THE INTEGRATED CIRCUIT MANUFACTURER. SEVERAL METHODS ARE INDICATED IN THE DRAWING BELOW. WITH THE LEADS OF THE CHIP POINTING AWAY FROM THE VIEWER, PIN #1 IS IN THE POSITION INDICATED WITH RESPECT TO THE VARIOUS END NOTCHES OR TINY CIRCULAR MARKINGS OR DEPRESSIONS IN ONE CORNER.

INSERTION OF INTEGRATED CIRCUIT CHIPS
BE SURE ALL LEADS ARE STRAIGHT AND PARALLEL. IF NOT, GENTLY STRAIGHTEN AND ALIGN THE BENT PINS WITH NEEDLE NOSED PLIERS.

INTEGRATED CIRCUIT CHIPS USUALLY COME FROM THE MANUFACTURER WITH THEIR ROWS OF LEADS SPREAD WIDER THAN THE SOCKET. TO BEND THE PINS IN A UNIFORM MANNER, PLACE THE CHIP ON ITS SIDE ON A FLAT SURFACE SO THAT ONE ROW OF PINS IS FLAT AGAINST THE SURFACE AS SHOWN ON THE FOLLOWING PAGE.

HOLDING EACH SIDE OF THE CHIP FIRMLY AGAINST THE FLAT SURFACE WITH BOTH HANDS, ROTATE IT A SHORT DISTANCE UNTIL THE PINS ARE BENT PERPENDICULAR TO THE BODY.

INSTALLING THE INTEGRATED CIRCUITS:
PUT THE REST OF THE ICs INTO THE SOCKETS. BE SURE THE LEADS ARE NOT BENT AND THAT THE PIN 1 INDEX IS TOWARD THE LEFT OR TOWARD THE TOP OF THE BOARD. IT IS VERY EASY TO FOLD PINS UNDER THE CHIPS WHILE INSTALLING THEM.

CLEAN THE BOARD WITH A FLUX REMOVING SOLVENT, THE FLUX HAS NO ELECTRICAL EFFECT, AND MAY BE LEFT ON THE BOARD IF DESIRED.
FUNCTIONAL DESCRIPTION

THE VECTOR GRAPHIC CPU BOARD IS DESIGNED AROUND THE INTEL 8080A MICROPROCESSOR CHIP. THIS BOARD IS S-100 BUS COMPATIBLE WITH ALL "ALTAIR™" AND IMSAI PRODUCTS, PROVIDING INTERCHANGEABILITY BETWEEN THE VARIOUS SYSTEMS.

SIMPLICITY OF DESIGN HAS BEEN STRESSED TO ENHANCE RELIABILITY OF OPERATION BY THE USE OF LSI AND MSI INTEGRATED CIRCUITS. THIS GOAL HAS BEEN ACHIEVED WHILE NOT SACRIFICING ANY LOSS IN PERFORMANCE.

INPUT POWER TO THE BOARD IS ±16V AND +8V. TO ACHIEVE THE REQUIRED LEVELS OF +12V AND ±5V, THREE VOLTAGE REGULATORS ARE USED. THEY ARE THE:

7805 FOR THE +5V (ON THE HEAT SINK)
79L05 FOR -5V
78L12 FOR +12V

AMPLE BYPASS AND FILTERING IS PROVIDED BY ELECTROLYTIC AND CERAMIC CAPACITORS DISTRIBUTED ON THE BOARD.

THE CENTRAL TIMING FUNCTION IS PROVIDED BY AN 8224 CLOCK GENERATOR I.C., WITH AN 18MHZ CRYSTAL USED AS THE PRIMARY FREQUENCY CONTROL ELEMENT FOR THE OSCILLATOR. THE OUTPUTS FROM THIS CHIP ARE Ø1 AND Ø2 FOR THE 8080A PLUS A Ø2 SUITABLE FOR DRIVING TTL CIRCUITS. BUFFERED Ø1 AND Ø2 CLOCKS ARE AVAILABLE ON THE S-100 BUS ON PINS 25(Ø1) AND 24(Ø2).

PROCESSOR TIMING IS DIVIDED INTO TWO BASIC CYCLES. THEY ARE THE MACHINE CYCLE AND INSTRUCTION CYCLE. AN INSTRUCTION CYCLE IS DEFINED AS THE TIME REQUIRED TO FETCH AND EXECUTE AN INSTRUCTION. DURING THE FETCH CYCLE A SELECTED INSTRUCTION IS READ FROM MEMORY AND DEPOSITED IN THE CPU. DURING THE EXECUTION PHASE THE INSTRUCTION IS DECODED AND TRANSLATED INTO SPECIFIC PROCESSING ACTIVITIES. EVERY INSTRUCTION CYCLE CONSISTS OF FROM ONE TO FIVE MACHINE CYCLES. A MACHINE CYCLE IS NEEDED EACH TIME THE PROCESSOR ACCESSES MEMORY OR AN I/O PORT. EACH MACHINE CYCLE CONSISTS OF FROM THREE TO FIVE STATES. A STATE IS DEFINED AS THE INTERVAL BETWEEN TWO Ø1 CLOCK PULSES.

THE 8224 PROVIDES THE RESET AND READY INPUTS TO THE 8080A. THESE SIGNALS ARE SYNCHRONIZED TO THE Ø2 CLOCK PULSE AND ARE INITIATED FROM S-100 BUS INPUTS. A RESET MAY BE GENERATED BY THE PRESET (PIN 75) INPUT FROM THE S-100 BUS OR BY AN RC TIME CONSTANT ON THE BOARD WHEN THE SYSTEM IS INITIALLYTurned ON. THE RESET SIGNAL ALSO GENERATES THE POWER ON CLEAR POC (PIN 99) OUTPUT ON THE S-100 BUS.

THE READY OUTPUT FROM THE 8224 INDICATES TO THE 8080A THAT VALID DATA IS AVAILABLE ON THE INPUT DATA LINES. THIS SIGNAL IS GENERATED BY THE PRDY (PIN 72) OR XRDY (PIN 3) INPUTS FROM THE S-100 BUS. FOR EXAMPLE, THE VECTOR GRAPHIC PROM/RAM BOARD GENERATES THE PRDY SIGNAL WHEN DATA IS AVAILABLE FROM THAT BOARD FOR USE BY THE CPU.

DATA I/O LINES ON THE 8080A ARE DO TO D7. THESE LINES ALLOW FUNCTIONAL DATA COMMUNICATION BETWEEN THE 8080A AND THE REST OF THE COMPUTER SYSTEM. INTERFACE BETWEEN THE 8080A DATA LINES AND THE S-100 BUS IS THROUGH 8097 TRISTATE BUS DRIVERS. THESE CIRCUITS ALLOW THE BOBBA TO OUTPUT DATA TO THE D0 BUS OR INPUT DATA FROM THE DI BUS AT THE CORRECT TIMES. STATUS SIGNALS DESCRIBING THE CURRENT MACHINE CYCLE ARE PROVIDED ON THE 8080A DATA LINES DURING THE FIRST PART OF EACH MACHINE CYCLE. THIS INFORMATION IS STORED IN AN 8212 8 BIT STATUS LATCH WHICH IS GATED ON TO THE S-100 BUS BY 8097 DRIVERS AT THE CORRECT TIME. THE FUNCTION OF EACH STATUS SIGNAL ON THE S-100 BUS IS DEFINED BELOW.
1. +8V  UNREGULATED INPUT TO +5V REGULATORS
2. +16V  UNREGULATED INPUT TO +12V REGULATORS
3. XRDY  ANDED WITH PRDY AND GOES TO 8080 RDY
4. V0    VECTORED INTERRUPT REQUEST 0
5. V1    VECTORED INTERRUPT REQUEST 1
6. V2    VECTORED INTERRUPT REQUEST 2
7. V3    VECTORED INTERRUPT REQUEST 3
8. V4    VECTORED INTERRUPT REQUEST 4
9. V5    VECTORED INTERRUPT REQUEST 5
10. V6   VECTORED INTERRUPT REQUEST 6
11. V7   VECTORED INTERRUPT REQUEST 7
12. XRKY2
13.
14.
15.
16.
17.
18. STD  STATUS BUFFER DISABLE
19. C/C  COMMAND/CONTROL BUFFER DISABLE
20. UNPR  INPUT TO MEMORY PROTECT CIRCUITRY ON
       MEMORY BD.
21. SS   INDICATES MACHINE IS IN SINGLE STEP MODE
22. ADD  ADDRESS BUFFER DISABLE
23. DOO  DATA OUT (FROM CPU) BUFFER DISABLE
24. X1   PHASE TWO CLOCK TTL LEVELS
25. X2   PHASE ONE CLOCK TTL LEVELS
26. PHDA  HOLD ACKNOWLEDGE, BUFFERED 8080 OUTPUT
27. PWAIT  WAIT ACKNOWLEDGE, BUFFERED 8080 OUTPUT
28. PI  INTERRUPT ENABLE, BUFFERED 8080 OUTPUT
29. A5  BUFFERED ADDRESS LINE 5 (32)
30. A4  BUFFERED ADDRESS LINE 4 (16)
31. A3  BUFFERED ADDRESS LINE 3 (8)
32. A15 BUFFERED ADDRESS LINE 15 (32768)
33. A12 BUFFERED ADDRESS LINE 12 (4096)
34. A9  BUFFERED ADDRESS LINE 1 (2)
35. D01 BUFFERED DATA OUT LINE 1
36. D00 BUFFERED DATA OUT LINE 0
37. A10 BUFFERED ADDRESS LINE 10 (1024)
38. D04 BUFFERED DATA OUT LINE 4
39. D05 BUFFERED DATA OUT LINE 5
40. D06 BUFFERED DATA OUT LINE 6
41. D12 DATA INPUT LINE 2
42. D13 DATA INPUT LINE 3
43. D17 DATA INPUT LINE 7
44. SMI LATCHED 8080 M1 STATUS
45. SOUT LATCHED 8080 OUT STATUS
46. SINP LATCHED 8080 INP STATUS
47. SMEMR LATCHED 8080 MEMR STATUS
48. SHLT  LATCHED 8080 HLTA STATUS
49. CLOCK 2 MHZ CLOCK, CRYSTAL CONTROLLED
50. GND  LOGIC AND POWER GROUND RETURN
51. + 8V UNREGULATED INPUT TO + 5V REGU-
LATORS
52. -16V UNREGULATED INPUT TO NEGATIVE
REGULATORS
53. SSW 05B  SENSE SWITCH DISABLE
54. EXT CLR  CLEAR SIGNAL FOR I/O DEVICES
55. CHASSIS GROUND
56. STSB  STROBE SIGNAL (BY 8224 CLOCK
CHIP 8800B D/C BOARD)
57. Digi ENABE SIGNAL FOR CPU DI DRIVERS
8800B
58. FRDY 8800B FRONT PANEL READY SIGNAL
59. 60. 61.
62. 63. 64.
65. 66. PHANTOM
67. MVR  WRITE ENABLE SIGNAL FOR MEMORY
68. PS  INDICATES IF ADDRESSED MEMORY IS
PROTECTED
69. PROT  INPUT TO MEMORY PROTECT CIRCU-
TRY ON MEMORY 80.
70. RUN INDICATES MACHINE IS IN RUN MODE
71. PARITY ANDED WITH XRDY AND GOES TO
8080 RDY
72. PINT  INPUT TO 8080 INTERRUPT REQUEST
73. PHOLD  INPUT TO 8080 HOLD REQUEST
74. PRESET  CLEAR SIGNAL FOR CPU
75. PSYN  BUFFERED 8080 SYNC SIGNAL
76. PWR  BUFFERED 8080 WRITE ENABLE SIGNAL
77. 78. 79. A0  BUFFERED ADDRESS LINE 0 [1]
80. A1  BUFFERED ADDRESS LINE 1 [2]
81. A2  BUFFERED ADDRESS LINE 2 [4]
82. A6  BUFFERED ADDRESS LINE 6 [64]
83. A7  BUFFERED ADDRESS LINE 7 [128]
84. A8  BUFFERED ADDRESS LINE 8 [256]
85. A13  BUFFERED ADDRESS LINE 13 [8192]
86. A14  BUFFERED ADDRESS LINE 14 [16384]
87. A11  BUFFERED ADDRESS LINE 11 [2048]
88. DC2  BUFFERED DATA OUT LINE 2
89. DC3  BUFFERED DATA OUT LINE 3
90. DC7  BUFFERED DATA OUT LINE 7
91. DI4  DATA INPUT LINE 4
92. DI5  DATA INPUT LINE 5
93. DI6  DATA INPUT LINE 6
94. DI1  DATA INPUT LINE 1
95. DI0  DATA INPUT LINE 0
96. SINTA  LATCHED 8080 INTA STATUS
97. SW0  LATCHED 8080 WO STATUS
98. STSTACK  LATCHED 8080 STACK STATUS
99. F0C  LO DURING POWER UP, RESET
100. GND  LOGIC AND POWER GROUND RETURN
STATUS SIGNAL DEFINITIONS

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>DEFINITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINTA [PIN 96]</td>
<td>ACKNOWLEDGE SIGNAL FOR AN INTERRUPT REQUEST</td>
</tr>
<tr>
<td>SWO [PIN 97]</td>
<td>INDICATES THAT THE CURRENT MACHINE CYCLE IS A MEMORY WRITE OR OUTPUT OPERATION.</td>
</tr>
<tr>
<td>SSTACK [PIN 98]</td>
<td>INDICATES THAT THE ADDRESS BUS HOLDS THE PUSHDOWN STACK ADDRESS FROM THE STACK POINTER</td>
</tr>
<tr>
<td>SHTLA [PIN 48]</td>
<td>ACKNOWLEDGE SIGNAL FOR THE HALT INSTRUCTION</td>
</tr>
<tr>
<td>SOUT [PIN 45]</td>
<td>INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN OUTPUT DEVICE</td>
</tr>
<tr>
<td>SMI [PIN 44]</td>
<td>INDICATES THAT THE BOBOA IS IN THE FETCH CYCLE FOR THE FIRST BYE OF AN INSTRUCTION</td>
</tr>
<tr>
<td>SINP [PIN 46]</td>
<td>INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN INPUT DEVICE</td>
</tr>
<tr>
<td>SMEMR [PIN 47]</td>
<td>INDICATES THAT THE BUS WILL BE USED FOR A MEMORY READ OPERATION</td>
</tr>
</tbody>
</table>

A SOCKET CONNECTOR TO THE BOBOA DATA LINES IS ALSO PROVIDED IN THE EVENT IT IS NEEDED TO INTERFACE A CONTROL PANEL TO THE CPU BOARD.

THERE ARE SIXTEEN ADDRESS LINES ON THE BOBOA. THIS ALLOWS THE CPU TO ACCESS UP TO 65,536 [64K WHERE K = 1024] MEMORY LOCATIONS. THESE ADDRESS LINES ARE CONNECTED TO THE S-100 BUS THROUGH 8297 DRIVERS AND GATED AT APPROPRIATE TIMES.

A POWERFUL PRIORITY VECTORED INTERRUPT STRUCTURE IS PROVIDED ON THE CPU BOARD. THIS IS ACCOMPLISHED USING AN 8214 PRIORITY INTERRUPT CONTROL I.C. AND AN 8212 LATCH TO GENERATE THE RST INSTRUCTION. THESE CIRCUITS ALLOW THE VECTOR GRAPHIC MICROCOMPUTER TO OPERATE AS A REAL TIME INTERRUPT DRIVEN COMPUTER SYSTEM. FOR A DETAILED DESCRIPTION OF THE THEORY OF INTERRUPTS REFER TO THE INTEL BOBOA MICROCOMPUTER SYSTEMS MANUAL.

THERE ARE EIGHT INTERRUPT INPUTS TO THE COMPUTER, VIO TO V17, WHICH ARE CONNECTED TO THE 8214 I.C. WHEN AN INTERRUPT IS SENSED BY THE 8214, A SYNCHRONIZED INTERRUPT SIGNAL IS SENT TO THE BOBOA. THE NUMBER OF THE INTERRUPT IS ENCODED AND SENT TO THE 8212 FOR USE IN GENERATING THE ADDRESS FOR THE INTERRUPT HANDLING SOFTWARE UNIQUE TO THAT INTERRUPT. THE PRIORITY FUNCTION IS PROVIDED WHEN MORE THAN ONE INTERRUPT IS RECEIVED BY THE 8214 BY COMPARING THE NUMBERS OF THE INTERRUPTS WITH A PRIORITY LEVEL STORED IN THE DEVICE. THIS PRIORITY LEVEL IS DETERMINED BY THE USER AND MAY BE CHANGED UNDER SOFTWARE CONTROL. THE INTERRUPT OF HIGHEST PRIORITY IS THE ONE WHICH IS PROCESSED.

OTHER INTERRUPT REQUESTS MAY BE GENERATED AND ENTERED INTO THE CPU BOARD BY THE PINT [PIN 73] INPUT FROM THE S-100 BUS. THE BOBOA MAY BE REQUESTED TO ENTER THE HOLD STATE BY THE PHOLD [PIN 74] INPUT FROM THE S-100 BUS. THE HOLD STATE ALLOWS AN EXTERNAL DEVICE TO GAIN CONTROL OF THE ADDRESS AND DATA LINES. WHEN THE PHOLD SIGNAL IS REMOVED THE BOBOA RESUMES NORMAL PROCESSING.

ANOTHER POWERFUL FEATURE OF THE VECTOR GRAPHIC CPU BOARD IS THE PROVISION OF A REAL TIME CLOCK. THIS FEATURE ALLOWS THE USER TO GENERATE A REAL TIME CLOCK OR EXECUTE TIME SEQUENCED OPERATIONS. A STABLE OP-AMP DIFFERENTIATOR SENSES THE 120 Hz RIPPLE ON THE +5V LINE TO GENERATE PRECISE 8.33 MSEC TIME INTERVALS. JUMPER CONNECTIONS ARE PROVIDED FROM THE CLOCK TO THE VECTORED INTERRUPT INPUTS. UNDER SOFTWARE CONTROL THE USER CAN GENERATE 8.33 MSEC INTERRUPTS TO THE BOBOA FOR TIMING OPERATIONS.

THERE ARE NUMEROUS ACKNOWLEDGE AND CONTROL SIGNALS FROM THE BOBOA AVAILABLE ON THE S-100 BUS. THESE SIGNALS ARE USEFUL FOR DETERMINING MACHINE STATUS AND CONTROLLING PERIPHERAL OPERATIONS. THEY ARE DEFINED BELOW.
ACKNOWLEDGE AND CONTROL SIGNALS

**SIGNAL**
- PSYNC (PIN 76)
- PWR (PIN 77)
- PDIN (PIN 78)
- PINT (PIN 28)
- PHLD (PIN 28)
- PWAIT (PIN 27)

**DEFINITION**
- PROVIDES A SIGNAL TO INDICATE THE BEGINNING OF EACH MACHINE CYCLE
- USED FOR MEMORY WRITE OR I/O OPERATIONS. DATA IS STABLE WHEN PWR IS LOW
- INDICATES THAT THE 8080A DATA BUS IS IN THE INPUT MODE
- INDICATES CONTENTS OF THE 8080A INTERRUPT ENABLE FLIP FLOP
- INDICATES THAT THE 8080A IS IN THE HOLD STATE
- INDICATES THAT THE 8080A IS IN THE WAIT STATE

There are a number of signals which will disable various portions of the S-100 bus. When these signals are active they effectively disconnect that portion of the CPU board from the S-100 bus, thus allowing external devices to control the S-100 bus. This feature is useful in DMA applications and multiprocessor systems. They are defined below.

S-100 BUS DISABLE SIGNALS

**SIGNAL**
- CC DSB (PIN 19)
- ADDR DSB (PIN 22)
- DO DSB (PIN 23)
- SSW DSB (PIN 53)
- STAT DSB (PIN 18)

**FUNCTION**
- DISABLES THE ACKNOWLEDGE AND CONTROL SIGNALS
- DISABLES THE ADDRESS LINES
- DISABLES THE OUTPUT DATA LINES
- DISABLES THE INPUT DATA LINES
- DISABLES THE STATUS LINES

All S-100 bus interfaces are provided with appropriate pull up resistors for optimum response of signals on the bus.

**JUMPER INSTALLATION**

If it is desired to use the real time clock function on the CPU board, a jumper must be installed to select which interrupt the clock will activate. Only one jumper should be used. This jumper will connect the real time clock output to the desired interrupt input. For example, if one wishes to have the clock enter on interrupt number 5 then a jumper should be installed from the clock to the V15 interrupt.

A pad is provided on the printed circuit board at the output of the real time clock. This point is identified on the assembly drawing as RTC. Simply solder a wire from RTC to the desired interrupt VIO to V17. Pads are provided for each interrupt and are labeled V16, V15, V14, V13, V12, V11, V10, and V7.

13
CLOCK DEMONSTRATION PROGRAM

A PROGRAM TO DEMONSTRATE THE USE OF INTERRUPTS AND THE REAL TIME CLOCK (RTC) IS
LISTED ON THE FOLLOWING PAGES. IN ORDER TO RUN THE PROGRAM, THE RTC INTERRUPT
MUST BE JUMPERED ON THE CPU BOARD TO VI0, WHICH CAUSES A "RST 7" TO BE EXECUTED
ON INTERRUPT. THIS IS DONE BY SOLDERING A JUMPER BETWEEN THE TWO BOTTOM PADS IN
THE COLUMN OF PADS IMMEDIATELY TO THE RIGHT OF C1. A VIDEO DISPLAY IS ASSUMED AT
ADDRESS D000.

THE PROGRAM CAN BE LOADED INTO RAM ON THE PROM/RAM BOARD AT CCOO USING THE "P"
COMMAND FROM THE MONITOR AND THEN SAVED ON TAPE. EXECUTE THE PROGRAM INITIALLY
AT CCB4 (TEST), WHICH HAS A DELAY LOOP TO SIMULATE THE RTC. THIS DOES NOT USE
THE INTERRUPTS, BUT WILL DISPLAY AN INCREMENTING TIME ON THE SCREEN TO MAKE SURE
THE PROGRAM IS FUNCTIONING.

NOTE: IF YOU HAVE A 3P+S BOARD IN YOUR SYSTEM, CHECK TO MAKE SURE THAT UNUSED
CIRCUITRY IS NOT PULLING SOME OF THE INTERRUPT LINES LOW. IT IS NECESSARY TO
LEAVE SEVERAL OF THE IC'S OUT IF THEIR INPUTS ARE NOT CONNECTED.

IF THE PROGRAM APPEARS TO BE FUNCTIONING, EXECUTE AT CCOO. THE FIRST
INSTRUCTIONS WRITE THE "JMP COUNT" INSTRUCTIONS AT LOCATION 0038F IN MEMORY,
INITIALIZE THE CURRENT STATUS REGISTER IN THE 8214 PRIORITY ENCODER BY
OUTPUTTING 8 TO PORT FD, AND ENABLE THE INTERRUPT FLIP-FLOP IN THE MPU. THIS
MUST BE DONE INITIALLY SINCE A POWER UP OR RESET ALSO RESETS THE INTERRUPT
FLIP-FLOP, AND IT MUST BE REPEATED AFTER EACH INTERRUPT, WHICH AUTOMATICALLY
RESETS THE 8214 AND DISABLES INTERRUPTS. AT THE END OF THIS ROUTINE, EXECUTION
RETURNS TO THE MONITOR, OR ANY OTHER PROGRAM THAT INITIALLY CALLS "START".

AN INTERRUPT, WHICH OCCURS EVERY 1/120TH SECOND, CAUSES NORMAL PROGRAM EXECUTION
TO BE SUSPENDED, AND THE "COUNT" ROUTINE TO BE EXECUTED. SINCE MANY PROGRAMS
HAVE A LIMITED SPACE ALLOCATED FOR THE STACK, THE STACK POINTER IS SAVED AND THE
STACK IS REINITIALIZED BELOW THE VIDEO DRIVER STORAGE LOCATIONS AND THEN ALL MPU
REGISTERS ARE SAVED. NOTICE THE ORDER IN WHICH THIS IS DONE. THE PSW MUST BE
SAVED ON THE OLD STACK BECAUSE DAD SP CHANGES THE CY FLAG.

A CALL TO "TICK" INCREASES THE TIME DIGITS STORED AT FACE IN BCD FORMAT AND
PROPOGATES A CARRY AS EACH DIGIT OVERFLOWS. THE NUMBER LOADED IN THE "B"
REGISTER WHEN "TOCK" IS CALLED DETERMINES THE MODULUS OF EACH REGISTER IN BCD,
NOT BINARY. FOR EXAMPLE, THE FIRST CALL TO "TOCK" DIVIDES THE INTERRUPT
FREQUENCY BY 12 TO PRODUCE A 10 HZ COUNT RATE. IF THE INCREMENTED REGISTER DOES
NOT OVERFLOW, "TOCK" RETURNS TWO LEVELS. THE FIRST DIGIT REGISTER IS EXAMINED,
AND IF IT IS ZERO, INDICATING THAT THE TIME HAS CHANGED AND THE DISPLAY MUST BE
UPDATED, "DISP" IS CALLED, WHICH WRITES THE DIGITS ON THE UPPER RIGHT HAND
CORNER OF THE SCREEN IN THE FOLLOWING FORMAT:

    AM - 09:36:25.3

THE TIME IS IN A MODIFIED MILITARY FORMAT; I.E., HALF PAST MIDNIGHT OR NOON =
00:30:00.0

BEFORE RETURNING TO THE PROGRAM INTERRUPTED, THE MPU REGISTERS AND THE STACK
POINTER ARE RESTORED, AND INTERRUPTS ARE ENABLED.
THE PROGRAM CAN BE USED WITH OTHER PROGRAMS THAT DO NOT USE THE RST 7 LOCATION OR DEPEND ON CRITICAL TIMING. INCLUDED IN THIS GROUP IS MITS BASIC. THE START Routine WILL OVERWRITE BASIC WITH THE NECESSARY CODE, INCLUDING EI AT LOCATION 0000, WHICH PERMITS RETURNING TO BASIC WITH THE CLOCK RUNNING.

THE PROGRAM CAN BE USED WITHOUT CHANGES WITH THE FOLLOWING VIDEO BOARDS:

- VECTOR GRAPHIC FLASH WRITER
- VDM-1
- POLYMORPHIC VTI
- SOLID STATE MUSIC

OPTIONALLY, "PRIAS" CAN BE SET TO 0 FOR ALL OF THE ABOVE EXCEPT VTI IF REVERSE VIDEO IS NOT DESIRED.

THE TIME IS SET USING THE MONITOR "P" COMMAND BY MODIFYING MEMORY LOCATIONS CC16 THROUGH CC1B.
0001  * CLOCK DEMONSTRATION PROGRAM
0002  * R. S. HARP 9/4/77
0004  PBIAS EQU 80H
0005  *
0006  * THIS ROUTINE PUTS THE PROPER CODE AT RST 7
0010  START LXI H, 38H
0020  MVI M, OC3H
0030  LXI H, COUNT
0040  SHLD 39H
0050  MVI A, OFBH
0060  STA 0
0070  MVI A, 008H
0080  OUT OFDH
0090  EI
0100  RET
0110  FACE DS 6
0140  COUNT PUSH H
0145  PUSH PSW
0150  LXI H, 00
0160  DAD SP
0170  LXI SP, OCFOOH
0180  PUSH H
0190  PUSH B
0200  PUSH D
0210  LXI H, FACE
0220  CALL TICK
0230  LXI H, FACE
0240  MOV A, M
0250  ORA M
0260  CZ DISP
0270  MVI A, 008H
0280  OUT OFDH
0290  POP D
0300  POP B
0310  POP H
0320  SPHL
0330  POP PSW
0340  POP H
0350  EI
0360  RET
0365  * FORMAT THE DISPLAY
0370  DISP LXI D, 0D03FH
0380  INX H
0390  CALL WRT2
0400  INX H
0410  MVI M, '.' + PBIAS
0420  XCHG
0430  DCX D
0440  CALL WRT2
0450  MVI M, '.' + PBIAS
0460  XCHG
0470  DCX D
0480  CALL WRT2
0490  MVI M, '.' + PBIAS
CC5A  EB  0500  XCHG
CC5B  1B  0510  DCX  D
CC5C  CD  70  CC  0520  CALL  WRT2
CC5F  EB  0530  XCHG
CC60  46  0540  MOV  B,M
CC61  EB  0550  XCHG
CC62  36  AD  0560  MVI  M,'-+'PBIAS
CC64  2B  0570  DCX  H
CC65  36  CD  0580  MVI  M,'M'+PBIAS
CC67  2B  0590  DCX  H
CC68  AF  0600  XRA  A
CC69  B8  0610  CMP  B
CC6A  36  C1  0620  MVI  M,'A'+PBIAS
CC6C  C8  0630  RZ
CC6D  36  D0  0640  MVI  M,'P'+PBIAS
CC6F  C9  0650  RET
CC70  7E  0655  * WRITE THE DIGITS ON THE SCREEN
CC71  E6  0F  0660  WRT2  MOV  A,M
CC73  F6  B0  0670  ANI  00FH
CC75  EB  0680  ORI  30H+PBIAS
CC76  77  0690  XCHG
CC77  EB  0700  MOV  M,A
CC78  1B  0710  XCHG
CC79  7E  0720  DCX  D
CC7A  1F  0730  MOV  A,M
CC7B  1F  0740  RAR
CC7C  1F  0750  RAR
CC7D  1F  0760  RAR
CC7E  E6  0F  0770  RAR
CC80  F6  B0  0780  ANI  00FH
CC82  EB  0790  ORI  30H+PBIAS
CC83  77  0800  XCHG
CC84  2B  0810  MOV  M,A
CC85  13  0820  DCX  H
CC86  C9  0830  INX  D
CC87  0840  RET
CC87  06  12  0845  * INCREMENT THE TIME
CC89  CD  A6  CC  0850  TICK  MVI  B,012H
CC8C  06  10  0855  CALL  TOCK
CC8E  CD  A6  CC  0860  MVI  B,010H
CC91  06  60  0870  CALL  TOCK
CC93  CD  A6  CC  0880  MVI  B,060H
CC96  06  60  0890  CALL  TOCK
CC98  CD  A6  CC  0900  MVI  B,060H
CC9B  06  12  0910  CALL  TOCK
CC9D  CD  A6  CC  0920  MVI  B,012H
CCA0  06  02  0930  CALL  TOCK
CCA2  CD  A6  CC  0940  MVI  B,002H
CAA5  C9  0950  CALL  TOCK
CAA6  7E  0960  RET
CAA6  7E  0970  * INCREMENT EACH DIGIT
CAA7  3C  0980  TOCK  MOV  A,M
CAA8  27  0990  INR  A
CAA9  B8  1000  DAA
CCAA  77  1010  CMP  B
CCAA  77  1020  MOV  M,A
CCAB C2 B2 CC 1030 JNZ NCAR
CCAE 36 00 1040 MVI M,O
CCBO 23 1050 INX H
CCB1 C9 1060 RET
CCB2 F1 1070 NCAR POP PSW
CCB3 C9 1080 RET
CCB4 CD 1C CC 1090 TEST CALL COUNT
CCB7 21 00 FE 1100 LXI H,0FE00H
CCBA 2C 1110 DELAY INR L
CCBB C2 BA CC 1120 JNZ DELAY
CCBE 24 1130 INR H
CCBF C2 BA CC 1140 JNZ DELAY
CCC2 C3 B4 CC 1150 JMP TEST
CCC5 9000 *

SYMBOL TABLE
COUNT CC1C DELAY CCBA DISP CC42 FACE CC16 NCAR CCB2 PBIAS 008C
START CC00 TEST CCB4 TICK CC87 TOCK CCA6 WRT2 CC70

$D CC00 CCC4
CC00 21 38 00 36 C3 21 1C CC 22 39 00 3E FB 32 00 00
CC10 3E 08 D3 FD FB C9 10 01 00 14 00 01 E5 F5 21 00
CC20 00 39 31 00 CF E5 C5 D5 21 16 CC CD 87 CC 21 16
CC30 CC 7E B6 CC 42 CC 3E 08 D3 FD D1 C1 E1 F9 F1 E1
CC40 FB C9 11 3F D0 23 CD 70 CC 23 36 AE EB 1B CD 70
CC50 CC 36 BA EB 1B CD 70 CC 36 BA EB 1B CD 70 CC EB
CC60 46 EB 36 AD 2B 36 CD 2B AF B8 36 C1 C8 36 D0 C9
CC70 7E E6 OF F6 B0 EB 77 EB 1B 7E 1F 1F 1F E6 0F
CC80 F6 B0 EB 77 2B 13 C9 06 12 CD A6 CC 06 10 CD A6
CC90 CC 06 60 CD A6 CC 06 60 CD A6 CC 06 12 CD A6 CC
CCA0 06 02 CD A6 CC C9 7E 3C 27 B8 77 C2 B2 CC 36 00
CCBO 23 C9 F1 C9 CD 1C CC 21 00 FE 2C C2 BA CC 24 C2
CCC0 BA CC C3 B4 CC

$
TROUBLESHOOTING HINTS

The CPU board is a sophisticated microprocessor with many time sequenced operations. Comprehensive trouble shooting techniques require the use of a high speed oscilloscope, and intimate knowledge of board operation. The hints provided here will allow the user to repair a board for 90% of most failures, since they are usually assembly errors, shorts or obviously failed parts.

If the CPU board fails to function properly, make the following checks:

1. Carefully inspect for solder shorts. A miniscule amount of solder across 2 printed traces is all that is needed for a short.
2. Carefully inspect for a crack in a PC trace. This type of failure has a lower probability of occurring.
3. Check the polarity of all diodes and electrolytic capacitors.
4. Insure that all ICs are properly installed with respect to pin orientation. (See the assembly drawing) The most common assembly error encountered is when the IC pins are bent under the chip. Carefully inspect for this type of mistake.
5. If an extender board is being used, and you experience seemingly ghost like failures, insert the CPU board directly in the motherboard. Transient noise can be caused by extender boards.
EXPERIMENTING WITH YOUR NEW COMPUTER

NOW THAT YOUR SHINY NEW COMPUTER IS ASSEMBLED AND CHECKED OUT, WHAT IS THE NEXT STEP? IF YOU HAVE NOT ALREADY DONE SO, YOU SHOULD READ THE INTEL 8080 MICROCOMPUTER SYSTEMS USER'S MANUAL AND BECOME FAMILIAR WITH THE INSTRUCTION SET AND EXACTLY WHAT GOES ON IN THE CPU CHIP FROM A PROGRAMMER'S POINT OF VIEW. THE NEXT STEP WOULD BE TO TRY YOUR HAND AT SOME SIMPLE ASSEMBLY LANGUAGE PROGRAMS. LENGTHY PROGRAMS ARE USUALLY WRITTEN WITH THE AID OF AN ASSEMBLER PROGRAM WHICH ENORMOUSLY SIMPLIFIES THE TASK OF MAKING CHANGES IN THE PROGRAM, SUCH AS ESP-1 WHICH IS AVAILABLE FROM VECTOR GRAPHIC INC. AT A NOMINAL CHARGE.

SHORT PROGRAMS CAN BE CODED BY HAND USING AN 8080 PROGRAMMING CARD AND THEN ENTERED IN THE COMPUTER MEMORY USING THE VECTOR 1 MONITOR. ASSEMBLY LANGUAGE PROGRAMMING CONSISTS OF BUILDING A PROGRAM USING GENERAL PURPOSE SUBROUTINES AS BUILDING BLOCKS. MOST PROGRAMS HAVE ROUTINES THAT READ THE KEYBOARD, OUTPUT TO A PRINTER, CONVERT FROM HEX TO BINARY AND BACK, COMPARE ADDRESSES AND SO ON. AN EXPERIENCED PROGRAMMER WILL HAVE A COLLECTION OF THESE ROUTINES IN HIS "BAG OF TRICKS" THAT HE CAN INSERT IN A PROGRAM WHEN NEEDED. THE DIFFICULT PART IS TO BE ABLE TO QUICKLY SCAN THROUGH THE ROUTINE AND UNDERSTAND EXACTLY WHAT IT DOES, HOW DATA IS PASSED BACK AND FORTH, AND WHICH REGISTERS ARE USED TO SEE IF IT INTERFERES WITH THE USE OF REGISTERS IN THE CALLING ROUTINE. IF THERE IS A CONFLICT, THE REGISTER CONTENTS MUST BE PUSHED ON THE STACK BEFORE THE ROUTINE IS CALLED AND POPPED BACK AFTER A RETURN.

A USEFUL COLLECTION OF SUBROUTINES IS CONTAINED IN THE VECTOR 1 MONITOR, AND THEY CAN BE CALLED BY ANY PROGRAM YOU WISH TO WRITE. AN EXAMPLE OF A SHORT PROGRAM CALLED SARCH IS SHOWN IN FIGURE 1. THE PURPOSE OF SARCH IS TO LOOK FOR SPECIFIC INSTRUCTIONS SUCH AS INPUT OR OUTPUT COMMANDS IN A LARGE PROGRAM. THIS PROGRAM WAS ASSEMBLED USING ESP-1 TO RUN IN RAM ON THE PROM/RAM BOARD AND CALLS SUBROUTINES FROM THE MONITOR. THE PROGRAM IS TYPED IN USING LINE NUMBERS TO IDENTIFY LINES IN THE FILE. THE FIRST INSTRUCTION IN CALL AH==, A SUBROUTINE IN THE MONITOR THAT INPUTS FOUR HEX DIGITS FROM THE KEYBOARD, ECHOES THEM TO THE PRINTER, CONVERTS THEM TO A 16 BIT BINARY ADDRESS IN REGISTERS H & L AND EXCHANGES H & L WITH D & E (REFER TO MONITOR LISTING). TWO SUCCESSIVE CALLS TO AH== RESULT IN A STARTING ADDRESS IN H & L, AND AN ENDING ADDRESS IN D & E. THE NEXT INSTRUCTIONS SAVE H, SET UP REGISTERS TO CONVERT ONLY 2 CHARACTERS TO BINARY AND THEN CALL A PORTION OF AH== TO INPUT A TWO DIGIT INSTRUCTION CODE FROM THE KEYBOARD. THIS CODE IS PUT IN REGISTER B, AND H IS RESTORED.

THE NEXT BLOCK OF INSTRUCTIONS IS REPEATED OVER AND OVER, SO A LABEL CONT IS GIVEN TO THIS POINT IN THE PROGRAM. MEMORY IS READ USING THE ADDRESS IN H & L AND COMPARED TO THE DESIRED OP CODE. IF THEY ARE NOT THE SAME, THE PROGRAM JUMPS TO SKP. IF THEY ARE THE SAME, PROGRAM EXECUTION PROCEEDS BY READING THE NEXT MEMORY LOCATION AND CALLING ERR WHICH PRINTS THE ADDRESS, OP CODE AND NEXT CODE IN THE PROPER FORMAT. BMP COMPARES THE CURRENT ADDRESS WITH THE FINISH ADDRESS IN D & E TO SEE IF IT IS TIME TO STOP, AND IF NOT, THE PROGRAM JUMPS BACK TO CONTINUE THE SEARCH.

STARTING AT LINE 0200 ARE FOUR INSTRUCTIONS CALLED PSEUDO OP CODES THAT SERVE TO GIVE THE ASSEMBLER ADDITIONAL INFORMATION IT NEEDS, NAMELY WHERE THE SUBROUTINES ARE ACTUALLY LOCATED. THE PARTICULAR ASSEMBLER USED REQUIRES THAT THE ADDRESSES IN HEX BE PRECEDED BY A 0 AND FOLLOWED BY 3 TO DENOTE HEX. NO OBJECT CODE IS GENERATED BY THESE INSTRUCTIONS. THE CODE PRODUCED BY THE ASSEMBLER IS SHOWN ON THE LEFT OF THE LISTING FOLLOWING THE 4 DIGIT HEX MEMORY LOCATION. MANY OF THE INSTRUCTIONS GENERATE MULTIBYTE CODES, AND THESE ARE LOADED IN SUBSEQUENT MEMORY LOCATIONS.

THE ASSEMBLER PRINTS AN ALPHABETICAL TABLE OF ALL THE LABELS USED IN THE PROGRAM FOLLOWED BY THE CORRESPONDING ADDRESS, SO THAT THESE POINTS CAN BE REFERENCED IN SUBSEQUENT PROGRAMS. BELOW THE SYMBOL TABLE, THE PROGRAM WAS EXECUTED BY TYPING G 1C00 FROM THE MONITOR. THE ADDRESS RANGE OF 1C00 TO 1CFF (THE MONITOR PROGRAM) WAS ENTERED AND THEN D3, THE 8080 CODE FOR "OUT". THE PROGRAM RESPONDED BY PRINTING OUT ALL LOCATIONS WHERE THE OUTPUT INSTRUCTION OCCURRED IN THE MONITOR PROGRAM FOLLOWED BY THE PORT NUMBER. YOU CAN TRY THIS ON YOUR SYSTEM BY ENTERING THE OBJECT CODE IN THE PROPER MEMORY LOCATION USING THE "P" MONITOR COMMAND.
FIGURE 1  EXPERIMENTING WITH YOUR NEW COMPUTER

A CC00
MEM LOC
CC00 CD 57 CO
CC03 CD 57 CO
CC06 E5
CC07 2E 00
CC09 0E 02
CC0B CD 5C CO
CC0E EB
CC0F 45
CC10 E1
CC11 7E
CC12 B8
CC13 C2 1C CC
CC16 23
CC17 7E
CC18 2B
CC19 CD 68 C1
CC1C CD F5 C1
CC1F C2 11 CC
CC22 C9
CC23
CC23
CC23
AHE1 C05C AHEX C057 BMP C1FS CONT CC11 ERP C168 SKP CC1C
SFCH CC00

G CO00

*G CO00 CO00 C1FF D3
CO08 D3 10
CO0C D3 10
CO0E D3 01
CO08 D3 6F
CO0E D3 6E
*G CO00 CO00 C1FF DB
CO76 DB 00
CO8B DB 00
CO92 DB 01
CO0C DB 6E
CO0E DB CO
C10F DB 6E
C116 DB 6F

SYMBOL TABLE

AHE1 C05C AHEX C057 BMP C1FS CONT CC11 ERP C168 SKP CC1C
SFCH CC00

G CO00

*G CO00 CO00 C1FF D3
CO08 D3 10
CO0C D3 10
CO0E D3 01
CO08 D3 6F
CO0E D3 6E
*G CO00 CO00 C1FF DB
CO76 DB 00
CO8B DB 00
CO92 DB 01
CO0C DB 6E
CO0E DB CO
C10F DB 6E
C116 DB 6F

*
GENERAL TROUBLE SHOOTING GUIDE

BECAUSE OF THE COMPLEXITY OF THE ENTIRE COMPUTER SYSTEM, BOTH THE HARDWARE AND SOFTWARE, IT IS ESSENTIAL TO ISOLATE ANY PROBLEM TO AN INDIVIDUAL BOARD OR PROGRAM.fortunately, ALL THE COMPUTER LOGIC IS ON EASILY REMOVABLE BOARDS. IT IS EXTREMELY VALUABLE TO HAVE ACCESS TO A TESTED COMPUTER SO THAT THE BOARDS CAN BE INDIVIDUALLY TESTED. ALTHOUGH THERE IS THE POSSIBILITY OF INTERACTION BETWEEN BOARDS DUE TO MARGINAL TIMING, OR DEFECTIVE COMPONENTS, THIS IS NOT THE USUAL CASE, AND IT IS BEST TO ASSUME THAT IF A BOARD WORKS IN COMPUTER A IT WILL ALSO WORK IN COMPUTER B.

THE MINIMUM SYSTEM CONSISTS OF THREE BOARDS, THE CPU BOARD, THE PROM/RAM BOARD, AND EITHER A VIDEO OR SERIAL I/O BOARD. MAKE SURE THAT THE MONITOR PROGRAM HAS BEEN PROPERLY PATCHED FOR THE PARTICULAR I/O CONFIGURATION OF YOUR SYSTEM. THERE IS TOTAL CONFUSION IN THE INDUSTRY CONCERNING PORT ASSIGNMENTS, LOGIC CONVENTIONS, AND STRAPPING OPTIONS. SEVERAL TYPES OF PROGRAMMABLE USBARDS ARE USED WHICH REQUIRE INITIALIZATION.

IF YOU HAVE CAREFULLY FOLLOWED THE ASSEMBLY INSTRUCTION FOR EACH OF THE BOARDS AND THE REGULATORS CHECK OUT, INSTALL ALL CHIPS. LET'S ASSUME YOU ARE USING A VIDEO DISPLAY. AS SOON AS YOU TURN THE COMPUTER ON, YOU SHOULD SEE A DISPLAY OF RANDOM MEMORY GARBAGE ON THE TV SCREEN. THIS WILL BE INDEPENDENT OF ANY FUNCTIONING OF THE COMPUTER OTHER THAN THE CLOCK OSCILLATOR. IF YOU DO NOT GET A PROPER DISPLAY, THE VIDEO INTERFACE MUST BE DEBUGGED FIRST. FEEL THE CHIPS ON THE BOARD, ANY THAT ARE HOT TO THE TOUCH MAY BE IN BACKWARDS (PROBABLY DESTROYED) OR MAY HAVE THEIR OUTPUTS SHORTED. THERE IS MORE THAN A FACTOR OF TEN DIFFERENCE IN THE POWER DISSIPATION OF TTL CHIPS, BUT THEY SHOULD NOT BE UNCOMFORTABLY HOT TO THE TOUCH.

REMOVE THE BOARD AND INSPECT IT CAREFULLY. ABOUT HALF OF THE PROBLEMS CAN BE FOUND SIMPLY BY VISUAL INSPECTION. LOOK WITH A MAGNIFYING GLASS OR INSPECTION SCOPE AT EACH PIN ON THE BOTTOM FOR UNSOLDERED PINS, MISSING PINS THAT MAY BE BENT UNDER OR BROKEN OFF. SOLDER BRIDGES BETWEEN PINS OR TO ADJACENT TRACES, AND ETCR BRIDGES BETWEEN TRACES (VERY HARD TO SEE). A CAREFUL EXAMINATION WILL TAKE 15 MINUTES, BUT MAY SAVE YOU A LOT OF GRIEF, AND YOU MAY DISCOVER PROBLEMS LIKE UNSOLDERED PINS THAT MAY REVEAL THEMSELVES ONLY LATER AS INTERMITTENT PROBLEMS. EXAMINE THE TOP OF THE BOARD TO BE SURE THE PROPER CHIPS ARE INSTALLED IN THE RIGHT PLACES. SIGHT ALONG THE EDGE OF THE CHIPS TO FIND BENT UNDER PINS. CHIPS ARE SOMETIMES INSERTED WITH A WHOLE ROW OF PINS THAT MISS THE SOCKET HOLES.

IF THE VISUAL INSPECTION FAILS TO GET THE VIDEO DISPLAY WORKING, A COMPONENT MAY BE BAD (USUALLY AN IC). TRY EXCHANGING IDENTICAL COMPONENTS TO SEE IF THE SYMPTOMS CHANGE. AT THIS POINT IT IS WISE TO GO BACK AND CAREFULLY REREAD THE MANUAL TO BE SURE YOU UNDERSTAND THE WAY THE BOARD WORKS AND THAT YOU HAVE SELECTED THE PROPER JUMPER OPTIONS. AFTER THIS, YOU WILL PROBABLY WANT TO TAKE THE UNIT TO A DEALER IF YOU ARE NOT FAMILIAR WITH DIGITAL TROUBLE SHOOTING PROCEDURES, OR GO THROUGH THE CIRCUIT BLOCK BY BLOCK WITH A SCOPE OR LOGIC PROBE IF YOU ARE EXPERIENCED.

AFTER THE VIDEO DISPLAY OR SERIAL I/O IS WORKING, THE RESET SWITCH SHOULD CAUSE A "*" PROMPT TO BE WRITTEN. IF THIS DOES NOT WORK, FOLLOW THE SAME PROCEDURE ON THE CPU AND PROM/RAM BOARDS. THE CPU BOARD CONSISTS MOSTLY OF 8087 BUS DRIVERS WHICH CAN BE EXCHANGED ONE BY ONE. THE VECTORED INTERRUPT AND REAL TIME CLOCK COMPONENTS, IC 180, 180D ARE NOT NECESSARY IN THE BOARD AT THIS TIME AND SHOULD BE REMOVED. USING A SCOPE, EXAMINE THE OUTPUT PINS OF ALL CHIPS. LOW LOGIC LEVELS ARE NORMALY LESS THAN 0.2 VOLTS AND HIGH GREATER THAN 3.0 VOLTS. A LEVEL OF 0.4 VOLTS MAY INDICATE SHORTS BETWEEN OUTPUTS WHERE ONE IS TRYING TO PULL HIGH AND THE OTHER LOW. A LEVEL OF 1.2 VOLTS INDICATES AN OPEN CIRCUIT INPUT. NMOS CHIPS HAVE SIMILAR LOGIC LEVELS, WHILE PMOS CHIPS CAN PULL TTL INPUTS TO -0.6V WHERE THE INPUT CLAMP DIODE LIMITS THE VOLTAGE. DO NOT BE SURPRISED AT HOW STRANGE SOME OF THE WAVEFORMS ON THE BUS LOCK, SUCH AS THE D LINES. THERE ARE PERIODS OF TIME DURING WHICH THE BUS IS NOT BEING ACTIVELY DRIVEN, AND THE VOLTAGE MAY DRIFT DUE TO RECEIVER INPUT CURRENT. ABNORMAL OPERATION IS INDICATED PRINCIPALLY BY ABNORMAL LOGIC LEVELS MAINTAINED CONSTANT FOR AT LEAST ONE CLOCK PERIOD (500 MICROSECONDS).

ONCE YOUR BASIC SYSTEM IS WORKING, CHECK OUT OF MEMORY BOARDS AND OTHER INTERFACES IS RELATIVELY STRAIGHTFORWARD USING THE MEMORY TEST PROGRAM IN THE MONITOR, OR SIMPLY DIAGNOSTIC ROUTINES YOU CAN PROGRAM IN MEMORY ON THE PROM/RAM BOARD. AFTER YOUR SYSTEM IS UP AND RUNNING, IT SHOULD BE QUITE RELIABLE. SINCE MANY MICROCOMPUTER SYSTEMS ARE MEMORY INTENSIVE, THE MEMORY IS THE MOST LIKELY SOURCE OF COMPONENT FAILURE. A SYSTEM WITH 32 K OF STATIC MEMORY MAY CONTAINS 75% OF ITS COMPONENTS ON THE MEMORY BOARDS. IF A PROBLEM IS EXPERIENCED RUNNING A PROGRAM, FIRST SUSPECT THE MEMORY AND USE THE MONITOR TEST PROGRAM. WE HAVE YET TO EXPERIENCE A PROBLEM WITH OUR 8K MEMORY BOARDS THAT WAS NOT REVEALED BY THE TEST PROGRAM. IF YOU DO MUCH REARRANGING OF YOUR SYSTEM, IT IS A GOOD PRACTICE TO TEST MEMORY FOR A FEW SECONDS WHEN YOU FIRST TURN ON THE COMPUTER TO MAKE SURE THE BOARDS ARE ADDRESSED PROPERLY OR THAT THEY ARE IN THE COMPUTER. THIS MAY SAVE SOME HEAD SCRATCHING WHEN THE PROGRAM YOU HAVE JUST LOADED FAILS TO RESPOND TO YOUR EAGER KEYBOARD TOUCH. IF YOU SUSPECT TEMPERATURE SENSITIVE CHIPS, REMOVE THE COVER OF THE COMPUTER TO INTERRUPT AIR FLOW BETWEEN BOARDS. WE DO NOT RECOMMEND OBLITERATING THE AIR FLOW THROUGH THE COMPUTER BY PLACING A SHEET OF PAPER OVER THE LEFT SIDE. A FULL COMPUTER MAY DISSIPATE OVER 300 WATTS AND REACH UNACCEPTABLE TEMPERATURES IF NO AIRFLOW IS PERMITTED.
ERRATA - CPU BOARD REV. 2

AN ERROR ON THE CPU BOARD REV. 2 RESULTS IN THE RESTART ADDRESSES GOING TO THE S-100 BUS IN IMPROPER ORDER.

A LOW ON PIN 11 OF THE S-100 WILL GIVE A RESTART 7.

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>6</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IF THE USER NEEDS THE PROPER ORDER OF RESTART ADDRESSES:

1. CUT THE TRACE FROM PIN 10 OF THE 8214 TO PIN 9 OF THE 8212.
2. CUT THE TRACE FROM PIN 8 OF THE 8214 TO PIN 18 OF THE 8212.
3. INSTALL A JUMPER FROM PIN 10 OF THE 8214 TO PIN 18 OF THE 8212.
4. INSTALL A JUMPER FROM PIN 8 OF THE 8214 TO PIN 9 OF THE 8212.