FEATURES:

SYSTEM COMPATIBILITY
. S-100 bus computer systems.

DISPLAY
. 64 or 32 characters per line (DIP switch selectable), 16 lines;
  Graphics -- 128 X 48 matrix.
. Character generator (MCM6571A) includes upper case, lower case, and Greek char-
  acters, and symbols and numbers; 7 X 9 dot character matrix; Character exten-
  sions below base line; Black-on-white or white-on-black.
. Left and right horizontal margins of 8%, upper vertical margin of 6%.
. Timing -- 60Hz vertical rate, 16.2KHz horizontal rate; Crystal -- 12.44MHz.

INTERFACE
. Parallel and composite video output (US TV signals); Separate video, horizontal
  and vertical sync; Output to video monitor or video amplifier in TV set.

SOFTWARE
. Powerful software included (object listing & paper tape) for cursor control --
  up, down, forward, back and home; Video reverse; Scrolling; and X-Y graphic
  control.

OTHER FEATURES
. Memory mapped; 1K bytes of 2102AL-2 RAMs, DIP switch addressable in 1K increments.
. Fully buffered address & data lines.
. High grade glass epoxy PC board with gold plated edge contacts; Low profile soc-
  kets provided for all ICs.
. Power requirements -- +8V @ 1.4A, +12V @ 30mA, -12V @ 15mA typical.

We used to be Solid State Music. We still make the blue boards.
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VB1 VIDEO INTERFACE BOARD

1.0 Assembly Instructions (Refer to VB1 Assy. Dwg.)

☐ Check kit contents against parts list.

☐ Check PC board for possible warpage & straighten if required

☐ Insert the 25 sixteen-pin sockets into the component side of the board with the "pin 1" index toward the top of the board. (The component side is the side on which "Solid State Music" is printed.) DON'T SOLDER.

☐ Insert the 9 fourteen-pin sockets. DON'T SOLDER.

☐ Insert the 3 eight-pin sockets. DON'T SOLDER.

☐ Insert the 3 twenty-four-pin sockets with "pin 1" toward the left of the board. DON'T SOLDER.

☐ Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.

☐ Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all the socket pins are thru the holes.)

NOTE: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or steel wool.

☐ On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.

☐ Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on top while reheatting each solder pin.

☐ Complete soldering the remaining pins on each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a fillet between pin and pad. Keep the tip against the pin and pad just long enough to produce the fillet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron tip is recommended.

☐ Observing polarity, insert and solder the 8 tantalum capacitors.

☐ Observing polarity, insert and solder the 2 zener diodes.

☐ Insert and solder the 21 one-fourth watt resistors. DO NOT insert the 2 three-watt resistors.
1.0 Assembly Instructions (cont'd)

- Observing polarity, insert and solder the transistor.
- Insert and solder the crystal.
- Insert and solder the DIP switch with the word "OPEN" to the left of the board.
- Insert and solder the 2 connectors. Be sure the teflon bases sit flat against the board.
- Insert and solder the 10 0.01\(\mu\)F capacitors and the 50pf capacitor.
- Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending to match the board holes--allow for bend radius.
- Bend regulator leads to match holes in board.
- If available, apply thermal compound to the back side of each regulator case (the side that will contact the heat sink). Use just a little thermal compound. Too much is worse than none at all.
- On the front (component side) of the board, first put on the heat sink (See VBI Assy. Dwg.), next the regulator, and finally insert the #6 screws for each of 2 regulators. Secure firmly from front side with lock nuts. Be sure the screws are tight and the regulator, heat sink, and board all fit together flatly for a good thermal connection. Now solder the regulator leads.
- At this point the only parts yet to be mounted are the two power resistors and all the IC's. DO NOT MOUNT THESE YET.
- Apply power (+8 volts approx.) to board by plugging into computer or by connection from a suitable power supply. Measure the regulated output of each regulator. If less than 4.8 volts is measured (allowing for meter accuracy) check for shorts or wiring errors. CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY-KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!
- Apply power (+16 volts) to the board by plugging into computer or by connection to a suitable power supply. Check for voltage on zener D1 of approx. 12 volts.
Apply power (-16 volts) to the board by plugging into computer or by connection to a suitable power supply. Check for voltage on D2 of approx. -3 volts.

Insert and solder the 2 power resistors. Important: mount these resistors up off the board about one-eighth inch. This gives the resistors better cooling and keeps them from discoloring the circuit board.

Finally, insert the IC's into their sockets, observing polarity.

Now, look the board over carefully. Check for poor solder joints or bridges. Using the component layout drawing, look for improper part location or polarity. A few minutes of careful inspection may save a few hours of troubleshooting.
2.0 SET-UP

2.1 HARDWARE REQUIREMENTS

Computer with S-100 bus. (Altair 8800, IMSAI, etc.)
ASCII keyboard or teletype
Two parallel input ports (for keyboard)
1K of RAM (located at 3C00 hex)

2.2 KEYBOARD INTERFACE

The Console Input (CI) and Console Status (CSTS) subroutines contained within the Demo programs supplied assume a standard (MITS rev. 1) keyboard interface. This interface uses Input Port 1 for data input, and Input Port 0 bit 0 (1s1) for a status bit (data available). Other input configurations can be accommodated by modifying these subroutines.

2.3 BOARD ADDRESSING

VB1 RAM address space is EC00 hex to EFFF hex for specified software.
Set address selection switches on VB1 as follows:

| A15 | OFF | A12 | ON |
| A14 | OFF | A11 | OFF |
| A13 | OFF | A10 | OFF |

2.4 SYSTEM OPERATION (Demo Programs)

A. Load programs in specified locations.
B. Momentarily set the RESET.
C. EXAMINE starting address of program to set program counter.
D. Turn off sense switches (A15-A0) & hit the RUN switch.

2.5 PROGRAM LOADING

The software supplied may be loaded into the computer by any one of the following methods:

1) Paper-tape Program:
   a. Put an Intel-format loader program into computer (user supplied).
   b. Run object program tape (supplied with VB1)

2) PROM Program: Run program from PROM (pre-programmed PROMs are available from Solid State Music with a 2K 8080 monitor program)

3) Source Listing:
   a. Load an Assembler program into computer.
   b. Enter Source program in software listing.

4) Object Listing: Enter Object program in software listing directly into memory.
2.0 SET-UP (cont'd)

2.6 SENSE SWITCH FUNCTIONS:

Additional control flexibility is provided for thru the use of the sense switches on the front panel of your mainframe. Setting sense switches to the "O" position will perform functions as defined below:

A8: output stops at bottom of page

A9: truncate line after 63 characters

2.7 MONITORS

CAUTION: HIGH VOLTAGE may be present in set even if unplugged. Service or modifications should be preformed ONLY by qualified personnel.

2.7.1 MONITOR CONNECTION

CAUTION: DO NOT USE A TRANSFORMERLESS TV FOR A MONITOR.

1) Most monitors can be connected directly to the composite video output with a single coax.

2) Some monitors may require the parallel video outputs provided.

3) Most TV sets will require one of the following:

   A. The addition of a jack connected to the input of the video amplifier (other inputs must be disconnected).

   B. Use of an RF Modulator to process the composite video signal for connection directly to antenna terminals.

2.7.2 MONITOR ADJUSTMENTS

The monitor or TV may need to have the horizontal and vertical size adjusted in order to get all of the data field on the screen. (Monitors set-up for TV pictures run the picture off the screen in order to eliminate "borders".)
3.0 TROUBLE SHOOTING HINTS

a. Check for proper settings of DIP switches.

b. Verify that all ICs are in the correct sockets.

c. Visually inspect all ICs to be sure that leads are in the sockets and not bent under.

d. Verify that the output voltage of each regulator is correct.

e. Inspect back side of board for solder bridges, running a small sharp knife blade between traces that appear suspicious. A magnifying glass is a must for this.

f. If you have an addressing problem:
   1) Check U42 (DM 8131) for addresses A10 thru A15.
   2) Check inputs & outputs of address buffers U23, U35, & U40 for shorts as well as proper operation.

g. If you have a problem with data output (consistent missing bits):
   1) Check inputs & outputs of buffers U28, U40, & U41 for shorts as well as proper operation.
   2) Check memory chips U24-U27 & U36-U39.

h. If you have a problem with horizontal sync:
   1) Check signals on U20, U31, U32, U19 & U10.

i. If you have problems with the vertical sync:
   1) Check signals on U12, U33, U29 & U17.

4.0 THEORY OF OPERATION

(Design improvements over VB-1A by LYNN COCHRAN)

4.1 GENERAL

The VB1 video interface is essentially a computer memory combined with an interface circuit that connects the memory to a video monitor. The memory data may be displayed in either alphanumeric form using the internal character generator, or in a direct form (graphics). Characters may be presented either white-on-black or black-on-white. Mixing characters and graphics is also possible.
4.0 THEORY OF OPERATION (cont'd)

4.1 GENERAL

The MCM6571AP Character Generator can display 128 different characters. Other generators with different character sets are available.

Sixteen lines of characters are produced and either 32 or 64 characters per line may be selected. Total memory consists of eight 1024-bit RAMs. Ten of the computer's memory address lines are connected to these RAMs, allowing the computer to selectively address each display position. The computer's remaining 6 address lines are used for addressing the board's memory location, as selected by a DIP switch on the circuit board.

4.2 SYNC GENERATION

Figure 1 shows the 12.4MHz crystal oscillator feeding a series of two counters, U31 and U32. Counter U31 divides the 12.44MHz signal by eight and passes the resulting 1.5375MHz signal to U32 for further division by sixteen. The DOT CLOCK is a square wave timing signal used in shifting out video. The LOAD signal is a pulse occurring once every eight DOT CLOCKS. Both the DOT CLOCK and the LOAD signal must be selected for either 32 or 64 character-per-line operation. If the "64/32" switch is open, the 6.22MHz from U31, QA is selected to be the DOT CLOCK; if the switch is closed, 12.4MHz from the oscillator is selected.

For the LOAD signal, switch "open" selects a 777.5 KHz signal and switch "closed" selects a +5 volt level. The LOAD signal is modified by the 1.5550 MHz pulse signal from the output of U10, pin 16, to become a series of narrow pulses at either 777.5 KHz
4.0 THEORY OF OPERATION (cont'd)

4.2 SYNC GENERATION (cont'd)

(64/32 switch open) or 1.5550 MHz (switch closed).
The 97.2 KHz carry signal from U32 is the input for the horizontal timing circuitry shown in figure 2. Both U11 flipflops and U20, pins 8-13, are used to divide the 97.2KHz from U32 by six to give horizontal blanking signals at 16.20 KHz. U13 generates a delayed horizontal sync pulse from U21, but only during horizontal blanking. U20, pins 1-6, develops the horizontal drive signal. Waveforms are shown as aids to troubleshooting in figures 1 thru 3.

In figure 3, the BIT SELECTOR CLOCK (16.20 KHz) goes to the bit select counter U29. The outputs from U29, QA thru QD, give the row select address for the character generator. When address 1110₂ is reached, U29 is loaded with 0000₂ on the next clock pulse to start a new cycle. The load signal is a negative pulse at 1079.9 Hz which is sent to flipflop U12 and vertical line counter U33. In addition to 4 bits of RAM address, U33 puts out negative pulses at 60.0 Hz on CY. U12 derives negative pulses at 60.0 Hz for both VERT DRIVE (1ms pulse width) and VERT BLANK (2ms pulse width). VERT BLANK and HORIZ BLANK are combined by an AND gate to give a composite BLANKING signal. The other 6 bits of RAM address come from counters U14 and U22 (on sheet 2), which are reset by HORIZ BLANK. U22's clock is the LOAD signal from fig. 1.

4.3 ADDRESSING

The eight 1024-bit RAMs are addressed by the computer
4.0 THEORY OF OPERATION (cont'd)

4.3 ADDRESSING (cont'd)

using the 10 address lines A0 thru A9. 6 additional lines form a prefix to specify the video board's address. This 6 bit prefix is set by the DIP switch on the board. U42 compares the address sent by the computer against the switch. If they agree the SELECT signal goes low actuating the 10 address gates (A0 thru A9), the output gates, (D10 thru D17), and the write gate U17. SELECT signal low also turns off the output gates of counters U14, U22, and U33. With the memory now "listening", the computer may store data on the video board to be displayed. When the address from the computer no longer matches the switch the SELECT line goes high and the memory is isolated once again.

4.4 PICTURE FORMATION

When in the normal character display mode, the memory is continually addressed by the counters U14, U22, and U33. The memory puts out an 8-bit word for each address. Only 7 bits go into the character generator data input to specify a character or into the multiplexers U5 and U15 for graphical output. Both the output of the character generator and the graphics multiplexers are fed into two data selectors, U6 and U7. If the GRAPHICS signal is low it passes the graphics data from U5 and U15. If GRAPHICS is high it passes the character generator output. In either case the data selectors' output are loaded into parallel-in/serial-out shift register U8. The data is then shifted out to the display monitor.
Solid State Music

4.0 THEORY OF OPERATION (cont'd)

4.4 PICTURE FORMATION (cont'd)

That eighth bit of memory is a control bit whose function depends on the VID REV/GRAPHICS switch. If the switch is open, GRAPHICS is high and the character generator output is going into output shift register U8. The eighth bit then turns the video reverse on or off by setting flipflop U13. This controls the VIDEO REVERSE signal thru gate U2. If VIDEO REVERSE is low the shift register output is unchanged, but if VIDEO REVERSE is high then gate U4 inverts the output giving a reversed video effect on the monitor. If the VID REV/GRAPHICS switch is closed the VIDEO REVERSE signal stays low unafflicting the shift register output. Now the eighth bit directly controls the GRAPHICS signal. If GRAPHICS is high then the character generator output is selected. If GRAPHICS is low then the graphics data is used.

4.5 POWER SUPPLIES

Power supply voltages of +8V and +16V are used to run the video board. The +8V input is regulated down to +5V by two 3-terminal regulators. R21 and R22 power resistors keep the power dissipation low in the regulators. Typical 8V current drain is 1.3A. The +16V input is regulated down to 12V by zener diode D1. The 16V current is about 40mA. Similarly, the -16V input is zener regulated down to -3V by D2. The -16V current is about 13mA.

5.0 WARRANTY

Solid State Music warrants its products to be free from defects in materials and/or workmanship for a period of 90 days for kits and bare boards, and one (1) year for factory assembled boards. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or mat-
5.0 WARRANTY (cont'd)

material, then, upon return of the product (postage paid) to Solid State Music at 2116A Walsh Ave., Santa Clara, California, 95050 "Attention Warranty Claims Department", Solid State Music will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by Solid State Music without charge for parts or labor when the product is returned within the specified period of the date of purchase. This warranty applies only to the original purchaser.

This warranty will not cover failure of Solid State Music products which, at the discretion of Solid State Music, shall have resulted from accident, abuse, negligence, alteration, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of Solid State Music products, Solid State Music assumes no liability in any events which may arise from the use of said technical information.

This warranty is in lieu of all other warranties, expressed or implied, including warranties of merchantability and fitness for use. In no event will Solid State Music be liable for incidental and consequential damages arising from or in any way connected with the use of its products.
FIGURE 2
<table>
<thead>
<tr>
<th>TITLE</th>
<th>PAGE</th>
<th>REV</th>
<th>DATE</th>
<th>BY</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOGIC DIAGRAM: CENTRAL TIMING, HORIZ-VENT SIGNAL GENERATORS, MEMORY ADDRESS COUNTER</td>
<td>2</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
<tr>
<td>LOGIC DIAGRAM: CANN AND MEMORY ADDRESS BUS</td>
<td>3</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
<tr>
<td>LOGIC DIAGRAM: READ/WRITE MEMORY</td>
<td>4</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
<tr>
<td>LOGIC DIAGRAM: INPUT/OUTPUT BUS, GRAPHICS GENERATOR</td>
<td>5</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
<tr>
<td>LOGIC DIAGRAM: ROW DOT CHARACTER GENERATOR LOGIC MONITOR INTERFACE POWER SUPPLIES</td>
<td>6</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
<tr>
<td>ASSEMBLY DRAWING: VBI, VIDEO BOARD 1</td>
<td>7</td>
<td>0</td>
<td>11-29-77</td>
<td></td>
</tr>
</tbody>
</table>

PAGE REFERENCE:

TO PAGE  FROM PAGE

SIGNAL ORIGIN  SIGNAL DESTINATION

WHERE, D = TO PAGE  S = FROM PAGE  K = MNEMONIC OF SIGNAL

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NEW SOFTWARE PACKAGE

The following software package is completely new and consists of 4 programs:

1) A Teletype Simulator program that can easily be patched-in to work with BASiC or other working software.

2) A TTY Simulator Demo program which may be used with the TTY Simulator in order to use the program without other software. The Demo includes cursor movement & video inverse capability using the following characters:

   CNTRL U = UP
   CNTRL D = DOWN
   CNTRL F = FORWARD
   CNTRL B = BACK
   CNTRL H = HOME
   CNTRL L = FORM FEED (blanks screen)
   ESC = INVERT VIDEO

3) A Graphics Interface Subroutines program which provides the ability to generate graphics by specifying the coordinates of a particular "dot" and whether it is to be light or dark.

4) A "Doodle" demonstration program that may be used with the Graphics Interface subroutines in order to use them without other user software. "Doodle" enables a user to "paint a picture" by moving the cursor to various locations and setting each location light or dark. These functions are performed thru the use of the following characters:

   W = white       D = down
   Q = black       F = forward
   Y = up          S = back

Additionally, up to 10 pictures may be saved by typing an "S" followed by a digit from 0 to 9. The picture may be retrieved by typing a "G" followed by the digit corresponding to the desired picture. This feature does require an additional 10x of memory starting at 1000 hex, however.
PATCHING INTO 3.1 *MITS BASIC

Mits basic has two output routines, one for the main console I/O and one for their "out" command. Only the main console routine needs to be altered. In 3.1 Basic the output routine looks like the following:

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BYTES</th>
<th>MNEMONIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$4 BF</td>
<td>DB,00</td>
<td>Stat: IN 0; input status</td>
</tr>
<tr>
<td>$4 C1</td>
<td>E6,80</td>
<td>ANI $88H; check dak flag</td>
</tr>
<tr>
<td>$4 C3</td>
<td>C2,BF,04</td>
<td>JNZ stat</td>
</tr>
<tr>
<td>$4 C6</td>
<td>F1</td>
<td>POP PSW; restore data</td>
</tr>
<tr>
<td>$4 C7</td>
<td>D3,01</td>
<td>OUT 1</td>
</tr>
<tr>
<td>$4 C9</td>
<td>C9</td>
<td>RET</td>
</tr>
</tbody>
</table>

In 3.2 Basic (without cassette routines), this output routine will be at about $4E4 Hex.

Two mnemonics that are boxed-in may be altered if you are using an Altair Rev. 0 interface instead of Rev. 1 as shown. The patch is to replace the routine called STAT with the following:

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BYTES</th>
<th>MNEMONIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$4 BF</td>
<td>F1</td>
<td>PATCH: POP PSW; restore data</td>
</tr>
<tr>
<td>$4 C0</td>
<td>B7</td>
<td>ORA A</td>
</tr>
<tr>
<td>$4 C1</td>
<td>C8</td>
<td>RZ; return if a null</td>
</tr>
<tr>
<td>$4 C2</td>
<td>C5</td>
<td>PUSH B</td>
</tr>
<tr>
<td>$4 C3</td>
<td>4F</td>
<td>MOV C, A</td>
</tr>
<tr>
<td>$4 C4</td>
<td>CD,00,3F</td>
<td>CALL VDTTY (see video driver)</td>
</tr>
<tr>
<td>$4 C7</td>
<td>C1</td>
<td>POP B</td>
</tr>
<tr>
<td>04 C8</td>
<td>C9</td>
<td>RET</td>
</tr>
</tbody>
</table>

Remember, when you put in the VB-1 software, Basic should not be allowed to write over it. This is done by re-assembling the VB-1 software for uncommitted memory or when MITS Basic is initialized and prints out "memory size" then type-in 16120.

* MITS, Inc., Albuquerque, New Mexico 87106
Solid State Music

; VIDEO BOARD DRIVER

; THIS SUBROUTINE FACILITATES THE USE
; OF THE SOLID STATE MUSIC VBI BOARD
; AND A VIDEO DISPLAY DEVICE AS A
; CONSOLE OUTPUT DEVICE.
; ASCII CHARACTERS PRESENTED TO THE
; SUBROUTINE IN THE C REGISTER ARE
; DISPLAYED ON THE SCREEN. CERTAIN
; CHARACTERS LISTED BELOW RECEIVE
; SPECIAL TREATMENT. ALL REGISTERS
; ARE PRESERVED BY THIS SUBROUTINE.

; LOC IS THE BEGINNING ADDRESS OF THE
; SUBROUTINE. IT MAY BE IN RAM OR ROM.

3F00  LOC EQU  3F00H

; VID IS THE BEGINNING ADDRESS ASSIGNED
; TO THE DISPLAY RAM LOCATED ON THE VBI
; BOARD.

EC00  VID EQU  0EC00H

; THREE BYTES OF RAM ARE REQUIRED FOR
; HOUSEKEEPING. THESE BYTES MUST BE
; IN AN AREA UNUSED BY OTHER PROGRAMS.

3FEA  VDPTR  EQU  LAST   :CURSOR POINTER
3FEC  VDHLD  EQU  VD PTR+2 :CHARACTER HOLD

; NON-DISPLAYABLE CHARACTERS

000C  FF   EQU  $CH   :FORM FEED, CONTROL-L
000A  LF   EQU  $AH   :CLEAR SCREEN, HOME CURSOR
000D  CR   EQU  $DH   :DOWN ONE LINE, CLEAR LINE
0015  UP   EQU  $8H   :CONTROL-U
0004  DN   EQU  $4H   :CONTROL-D
0006  FV   EQU  $6H   :CONTROL-F
0002  BK   EQU  $2H   :CONTROL-B
0008  HM   EQU  $8H   :CONTROL-H
Solid State Music

; NORMAL ENTRY POINT

3F00 E5
VDTTY: PUSH H ;SAVE HL
3F01 21EA3F
LXI H, VDptr ;ADDR OF CURSOR POINTER

; ALTERNATE ENTRY POINT
; THIS ENTRY POINT MAY BE USED IF
; THE CURSOR POINTER AND CHARACTER
; HOLD ARE AT LOCATIONS OTHER THAN
; THOSE SPECIFIED ON THIS LISTING.
; THE USER MUST SUPPLY SUBROUTINE
; ENTRY CODE AS FOLLOWS:
; JENTRI: PUSH H ;SAVE HL
; LXI H, PTR ;ADDR OF CURSOR POINTER
; JMP ALTVD ;JOIN THIS CODE

3F04 D5
ALTVD: PUSH D ;SAVE DE
3F05 C5
PUSH B ;SAVE BC
3F06 F5
PUSH PSW ;SAVE AF
3F07 5E
MOV E, H ;LPTR
3F08 23
INX H ;
3F09 7E
MOV A, M ;HPTR
3F0A E603
ANI 3 ;CONVERT TO VIDEO
3F0C C6EC
ADI VID SHR B ;RAM ADDRESS
3F0E 57
MOV D, A ;
3F0F 23
INX H ;
3F10 46
MOV B, M ;CHAR UNDER CURSOR
3F11 7F
XCHG ;PNTR TO HL
3F12 7F
MOV H, B ;RESTORE PREV CHAR

; IDENTIFY INPUT CHAR

3F13 79
MOV A, C ;NEW CHAR
3F14 FC0C
CPI FF ;
3F16 CA763F
JZ UIDFF ;FORM FEED
3F19 FE0D
CPI CR ;
3F1B C843F
JZ VDOR ;CARRIAGE RETURN
3F1E FE0A
CPI LF ;
3F20 C8B3F
JZ VIDLFE ;LINE FEED

; THE FOLLOWING INSTRUCTIONS
; (MARKED YYYY) MAY BE REMOVED
; IF CURSOR CONTROL IS NOT
; REQUIRED.

3F23 FE15
CPI UP YYYY
3F25 CAD23F
JZ CHUP YYYY
3F28 F004
CPI DN YYYY
3F2A CAD53F
JZ CRDN YYYY
Solid State Music

```
3F2D FE06  CPI   FW   YYYY
3F2F CA4C3F  JZ    CRRT  YYYY
3F32 FE02  CPI   BK    YYYY
3F34 CADE3F  JZ    CRLT  YYYY
3F37 FE08  CPI   HM    YYYY
3F39 CAE43F  JZ    CRHM  YYYY

; DISPLAYABLE CHARACTER

; THE FOLLOWING INSTRUCTIONS
; (MARKED XXXX) MAY BE REMOVED
; IF SENSE SWITCHES ARE NOT
; TO BE USED.

; CHECK FOR END LINE

3F3C 7D  MOV    AL    XXXX
3F3D E63F  ANI   3FH    XXXX
3F3F FE3F  CPI   3FH    XXXX
3F41 C24B3F  JNZ   VID80    XXXX

; IGNORE CHARACTER IF END OF
; LINE AND SENSE SWITCH 2 OFF

3F44 DBFF  IN     2FFH    XXXX
3F46 E682  ANI   E     XXXX
3F48 CA623F  JZ    VIDRT    XXXX
3F4B 71  VIDB0:  MOV    M,C    ;
3F4C 010100  CRRT:  LXI    B,1    ;

; ADJUST CURSOR POINTER

3F4F 09  CRADJ:  DAD    B    ;

; CHECK FOR OVERFLOW

3F50 7C  MOV    AXH    ;
3F51 FE00  CPI   (VID+1824) SHR 8    ;
3F53 C2623F  JNZ   VIDRT    ;
3F56 26EF  MOV   M:VID+960:    SHR 8    ;
3F58 7D  MOV    AXL    ;
3F59 F6C0  CPI   9C86    ;
3F5B 6F  MOV    DX:    ;
3F5C CDAA3F  CALL   WLD2B    ;
3F5F C3683F  JMP   VID81    ;

; COMMON EXIT CODE
; NORMALIZE CURSOR POINTER

3F62 7C  VIDRT:  MOV    AXH    ;
3F63 E683  ANI   3    ;
3F65 C6EC  ADI   V', SHR 8    ;
```
Solid State Music

3F67 67 MOV AL, A
3F68 7E VIDRI: MOV AL, A MOV AH, 0
3F69 367F MVI BL, 0
3F6B EB XCHG
3F6C 77 MOV AL, A
3F6D 2B DCX H
3F6E 72 MOV AL, D
3F6F 2B DCX H
3F70 73 MOV AL, E

; RESTORE REGISTERS, EXIT
3F71 F1 POP PSW
3F72 C1 POP B
3F73 D1 POP D
3F74 E1 POP H
3F75 C9 RET

; PROCESS FORM FEED
; FALL SCREEN WITH SPACES,
; MOVE CURSOR TO TOP LEFT
3F76 2100EC VIDFF: LXI H, VID
3F79 E5 PUSH H
3F7A 3620 VIDFFG: MVI M, 0
3F7C 23 INX M
3F7D 7C MOV AL, M
3F7E FEF0 CPI (VID+1024) SHR 8
3F80 DA7A3F JG VIDFFG
3F83 E1 POP H

; PROCESS CARTRIDGE RETURN
; MOVE CURSOR TO BEGINNING
; OF LINE
3F84 7D VIDCR: MOV AL, L
3F85 E6C0 ANI 0C0H
3F87 6F MOV L, A
3F88 C3623F JMP VIDRT

; PROCESS LINE FEED
; MOVE CURSOR DOWN ONE LINE,
; FILL NEW LINE WITH SPACES
3F8B D5 VIDLF: PUSH D
3F8C 114000 LXI D, 0
3F8F 19 DAD D
3F90 7C MOV AL, M
3F91 FEF0 CPI (VID + 1024) SHR 8
3F93 C2C13F JNZ VIDLF3
THE FOLLOWING INSTRUCTION
(MARKED XXXX) MAY BE REMOVED
IF SENSE SWITCHES ARE NOT
TO BE USED.

WAIT UNTIL SENSE SWITCH 1 IS ON
BEFORE ROLLING UP ONE LINE.

3F96 DBFF VDLF2: IN 0FFH XXXX
3F98 E601 ANI 1 XXXX
3F9A CA963F JZ VDLF2 XXXX

ROLL THE SINGLE DISPLAY UP ONE
LINE.

3F9D CDAA3F CALL ROLLS 1
3FA3 7D MOV A,L 1
3FA1 F6C0 ORL $C00 1
3FA3 6F MOV L,A 1
3FA4 26EF MOVL $L,VID+960 SHR 8 1
3FA6 D1 POP D 1
3FA7 C3623F JMP VIDRT 1

ROLL SUBROUTINE

3FAA D5 ROLL0: PUSH D 1
3FAB E5 PUSH H 1
3FAC 1100EC LXI D,VID 1
3FAF 2140EC LXI H,VID+64 1
3FB2 7E ROLL1: MOVL A,M 1
3FB3 12 STAX D 1
3FB4 3620 MVI M,20H 1
3FB6 13 INX D 1
3FB7 23 INX H 1
3FB8 7C MVI A,A 1
3FB9 FEF0 CPI (VID+1024) SHR 8 1
3FBB C2B23F JNZ ROLL1 1
3FBE E1 POP H 1
3FBD D1 POP D 1
3FC0 C9 RET 1

FILL NEW LINE WITH SPACES

3FC1 E5 VDLF3: PUSH H 1
3FC2 7D MOV A,L 1
3FC3 E6C0 ANI $C00 1
3FC5 6F MOV L,A 1
3FC6 3620 VDLF4: MVI H,$ ' 1
3FCA 23 INX H 1
3FC9 1D DCR E 1
3FCD C2C63F JNZ VDLF4 1
3FCE E1 POP H 1
3FCE D1   POP D ;
3FCF C3623F  JMP VIDRT ;

; THE FOLLOWING INSTRUCTIONS,
; ALONG WITH THOSE MARKED
; YYYY ABOVE, MAY BE REMOVED
; IF CURSOR CONTROL IS NOT
; REQUIRED.

; CURSOR CONTROL PROCESSING

3FD2 01C0FF CRUP: LXI B,-64 YYYY
3FD5 C34F3F  JMP CRADJ YYYY
3FD8 014000 CRDN: LXI B,64 YYYY
3FD8 C34F3F  JMP CRADJ YYYY
3FDE 01FFFF CRLT: LXI D,-1 YYYY
3FE1 C34F3F  JMP CRADJ YYYY
3FE4 210000 CRHM: LXI H,0 YYYY
3FE7 C3623F  JMP VIDRT YYYY
3FEA 00 LAST: NOP

0000 END
Solid State Music

; VDTTY DEMONSTRATION ROUTINE

; LOC IS THE BEGINNING ADDRESS OF THE ROUTINE. IT MUST BE IN RAM.
3E00 LOC EQU 3E00H

; VID IS THE BEGINNING ADDRESS ASSIGNED TO THE DISPLAY RAM LOCATED ON THE VBI BOARD.
EG00 VID EQU 0EG00H

; VDTTY IS THE VIDEO DRIVER ROUTINE.
3F00 VDTTY EQU 3F00H
3E00 STACK EQU 3E00H

; NON-DISPLAYABLE CHARACTERS
001B INV EQU 1BH \SESC\AA\E
002C FF EQU 0CH \SFORM FEED\(CONTROL-L)\E
003A LF EQU 0AH \SLINE FEED\E
003D CR EQU 0DH \SCARRIAGE RETURN\E
0035 UP EQU 15H \SCONTROL U\E
0004 DN EQU 04H \SCONNROL D\E
0006 FW EQU 06H \SCONTROL F\E
0002 BK EQU 02H \SCONTROL B\E
0008 HM EQU 08H \SCONTROL H\E

3E00 ORG LOC

3E00 31003E DEMO: LXI SI, STACK
3E03 CD4C3E DI: CALL GI
3E06 E67F ANI TPW
3E08 4F MOV CA
3E09 FE0C CPI FF
3E0B CA453E JZ DISPI
3E0E FE0D CPI CR
3E10 CA453E JZ DISPI
3E13 FE0A CPI LF
3E15 CA453E JZ DISPI
3E18 FE15 CPI UP
3E1A CA453E JZ DISPI
3E1D FE04 CPI DN
3E1F CA453E JZ DISPI
3E22 FE06 CPI FW
3E24 CA453E JZ DISPI
3E27 FE02 CPI BK
3E29 CA453E JZ DISPI
3E2C FE08 CPI SM
3E2E CA453E JZ DISPI
3E31 FE1B CPI BV
3E33 3A4B3E LEA E1TA
Solid State Music

3E36 C2433E JNZ DISP
3E39 E680 ANI 80H
3E3B EE80 XRI 80H
3E3D 32433E STA BITB
3E40 C3033E JMP D1
3E43 81 DISP:ORA C
3E44 4F MOV CLR
3E45 CD003F DISPLAY CALL VDTTY
3E48 C3033E JMP D1
3E4B 86 BITB:DB 0

; CONSOLE INPUT SUBROUTINE

3E4C DB00 CH:IN 0
3E4E E601 ANI 1
3E50 C2430E JM2 CH
3E53 DB01 IN A
3E55 09 BST

0000 END
Solid State Music

GRAPHICS INTERFACE SUBROUTINES

These subroutines facilitate the use of the Solid State Music VBI board as a video display device and a graphics display device.

These subroutines treat the display screen as a matrix of dots, 48 dots high by 128 dots wide. Each dot is specified in terms of its vertical coordinate (0-47) and its horizontal coordinate (0-127). Dot 0,0 is at the lower left corner of the screen.

The subroutines have similar interfaces with their calling programs. Register 0 is preserved.

Entry Conditions:
- \( H = \text{vertical coordinate} \)
- \( L = \text{horizontal coordinate} \)

Exit Conditions:
- \( A = \text{differs by subroutine} \)
- \( H = \text{preserved} \)
- \( C = \text{bit mask for specified dot} \)
- \( L = \text{memory address of dot} \)
- \( M = \text{vertical coordinate} \)
- \( L = \text{horizontal coordinate} \)
- \( H \) and \( L \) are converted (if necessary)

Module 46 and 128 respectively.

LOC is the beginning address of these subroutines. It may be in RAM or ROM.

LOC

vid is the beginning address assigned to the display RAM located on the VBI board.

vid

THE CHECK SUBROUTINE SETS THE ZERO FLAG TO INDICATE WHETHER THE SPECIFIED DOT IS WHITE OR BLACK. IF THE DOT IS CURRENTLY WHITE THE ZERO FLAG IS SET ON. IF THE DOT IS BLACK THE FLAG IS SET OFF. FOR A REGISTER CONTAINS ZERO IF THE DOT IS WHITE; THE BIT MASK IS TO BE CLEAR.

3E80 C993E CHECK CALL (WITH)
Solid State Music

3E83 A1
3E84 C9

; THE WHITE SUBROUTINE SETS THE
; SPECIFIED DOT WHITE. REGISTER
; A CONTAINS THE NEW CONTENTS OF
; THE MEMORY LOCATION.

3E85 CD9A3E WHITE:
3E88 E6BF
3E8A F600
3E8C B1
3E8D A9
3E8E 12
3E8F C9

; THE BLACK SUBROUTINE SETS THE
; SPECIFIED DOT BLACK. REGISTER
; A CONTAINS THE NEW CONTENTS OF
; THE MEMORY LOCATION.

3E90 CD9A3E BLACK:
3E93 E6BF
3E95 F600
3E97 B1
3E98 12
3E99 C9

; THE CNVRT SUBROUTINE PERFORMS
; THE COORDINATE TO ADDRESS -
; BIT MASK CONVERSION. REGISTER
; A CONTAINS THE CURRENT CONTENTS
; OF THE MEMORY LOCATION.

3E9A C5 CNVRT:
3E9B 7D
3E9C E67F
3E9E 6F
3E9F 7C
3EA0 D630
3EA2 F2A03E
3EA5 G630
3EA7 FAA53E
3EAA 67
3EAB E5

; NORMALIZE THE COORDINATES

3EAC 44
3EAD 4D
3EAE 5C
3EAF 1600
3EB1 210100
3EB4 19
3EB5 29

; CONVERT COORDINATES TO ADDRESS
; IN DE
Solid State Music

3EB6 29 DAD H ;
3EB7 19 DAD D ;
3EB8 29 DAD H ;
3EB9 29 DAD H ;
3EBA 19 DAD D ;
3EBB 54 MOV D, H ;
3EBC 7D MOV A, L ;
3EBD E6C0 ANI 0C0H ;
3EBF 5F MOV E, A ;
3EC0 19 DAD D ;
3EC1 19 DAD D ;
3EC2 29 DAD H ;
3EC3 29 DAD H ;
3EC4 78 MOV A, B ;
3EC5 94 SUB H ;
3EC6 47 MOV B, A ;
3EC7 3EC0 MOV1 A, (VID+960) AND 0FFH
3EC9 53 SUB D ;
3ECA 7F MOV E, A ;
3ECB 3EEF MOV1 A, (VID+960) SHR 8
3ECD 5A MOV D, A ;
3ECE 57 MOV A, C ;
3ECF 79 MOV D, A ;
3ED0 1F RAR ;
3ED1 B3 ORA E ;
3ED2 5F MOV E, A

; GENERATE BIT MASK

3ED3 79 MOV A, C ;
3ED4 1F RAR ;
3ED5 76 MOV A, B ;
3ED6 17 RAL ;
3ED7 4F MOV C, A ;
3ED8 0600 MOV1 B, 0 ;
3EDA 21E43E LDI R, DTAB ;
3EDD 09 DAD B ;
3EEE 7E MOV A, H

; PREPARE FOR EXIT

3EEB E1 POP H ;
3EEC 01 POP D ;
3EE1 4F MOV C, A ;
3EE2 1A LDAK D ;
3EE3 09 RET ;

3EE4 04 DTAB: DB 04H
3EE5 20 DB 20H
3EE6 02 DB 02H
3EE7 10 DB 10H
3EE8 01 DB 01H
3EE9 08 DB 08H

0000 END
Solid State Music

DOODLE (GRAPHICS DEMO)

EC00 VID EQU 0EC00H
3E00 STACK EQU 3E00H
3E80 CHECK EQU 3E80H
3E85 WHITE EQU 3E85H
3E90 BLACK EQU 3E90H

3D00 ORG 3D00H

3D00 3103E DOODL EQU SP, STACK ;
3D03 2103E LXI H, VID ;
3D06 3E80F D0: MVI M, 0BFH ;
3D08 23 INX H ;
3D09 7C MOV A, H ;
3D0A FEF0 CPI (VID+1024) SHR 8 ;
3D0C C263D JMZ D8 ;
3D0F C3153D JMP D2 ;
3D12 22CD3D D1: SHLD CURS ;
3D15 2ACD3D D2: LMFD CURS ;
3D18 CD803E CALL CHECK ;
3D19 1A LDAX D ;
3D1C F680 ORI B0H ;
3D1E 32CF3D D3: STA OLD ;
3D21 3ACF3D D4: LDA OLD ;
3D24 A9 XRA C ;
3D25 12 STAX D ;
3D26 0610 MVI B, 0H ;
3D28 CDBB3D CALL WAIT ;
3D2B C23A3D JNZ D5 ;
3D2E 3ACF3D LDA OLD ;
3D31 12 STAX D ;
3D32 0620 MVI B, 20H ;
3D34 CDBB3D CALL WAIT ;
3D37 CA213D JZ D4 ;
3D3A 3ACF3D D5: LDA OLD ;
3D3D 12 STAX D ;
3D3E CDD03D CALL CI ;
3D41 FE51 CPI 'Q' ;BLACK
3D43 CA743D JZ BLK ;
3D46 FE57 CPI 'W' ;WHITE
3D48 CA7A3D JZ WHT ;
3D4B FE53 CPI 'S' ;SAVE
3D4D CA803D JZ SAVE ;
3D50 FE47 CPI 'G' ;GET
3D52 CA863D JZ GET ;
3D55 2C INR L ;
3D56 FE46 CPI 'F' ;FORWARD
3D58 CA123D JZ D1 ;
3D5B 2D DCR L ;
3D5C 2D DCR L ;
3D5D FE42 CPI 'B' ;BACK
3D5F CA123D JZ D1 ;
3D62 2C INR L ;
3D63 2A INR H ;
3D64 FE55 CPI 'H' ;JUP
3D66 CA123D JZ D1 ;
3D69 25 DCR H ;
Solid State Music

3D6A 25       DCR    H
3D6B FE44     CPI    'D'   :DOWN
3D6D CA123D  JZ     D1    :
3D70 24       INR    H
3D71 C31E3D   JMP    D3    :

3D74 CD903E  BLK:    CALL    BLACK   :
3D77 C3153D  JMP    D2    :

3D7A CD853E  WHT:    CALL    WHITE   :
3D7D C3153D  JMP    D2    :

3D80 CD903D  SAVE:   CALL    NUM   :
3D83 C38A3D  JMP    SG    :

3D86 CD903D  GET:    CALL    NUM   :
3D89 EB      XCHG    :

3D8A CDAA3D  SG:     CALL    MOVE   :
3D8D C3153D  JMP    D2    :

3D90 CDD03D  NUM:    CALL    CI    :
3D93 D630     SUI    '0'    :
3D95 FA903D  JN     NUM    :
3D98 FE0A     CPI    10    :
3D9A F2903D  JP     NUM    :
3D9D 67      MOVU   R,A    :
3D9E 2E00     MVI    L,0    :
3DA0 29      DAD    R    :
3DA1 29      DAD    R    :
3DA2 110004  LXI    D,STORE   :
3DA5 19      DAD    B    :
3DA6 1100EC  LXI    D,VID    :
3DA9 C9      RET    :

3DAA 6604   MOVE:   MVI    E,4   :
3DAC 1A     MVI:    LDAX    D    :
3DAD E6BF    AMI    3BFH   :
3DAF 77      NOV    M,A    :
3DB0 13      INX    D    :
3DB1 2C      INR    L    :
3DB2 C2AC3D  JNZ    MVI    :
3DB5 24      INR    H    :
3DB6 05      SGR    B    :
3DB7 C2AC3D  JNZ    MVI    :
3DBA C9      RET    :

3DBB C5      WAIT:   PUSH    E    :
3DBC CDDC3D  W1:    CALL    CSTS   :
3DBF B7      GRA    A    :
3DC0 C2CB3D  JNZ    W2    :
3DC3 0D      DCR    C    :
3DC4 C2BC3D  JNZ    W1    :
3DC7 05      DCR    B    :
3DC8 C2BC3D  JNZ    W1    :
3DCB C1      W2:    POP    E    :
3DCC C9      RET    :

3DCC 6000  CURS:    DW    W
Solid State Music

3DCF 00  OLD:  DB  0

; CONSOLE INPUT SUBROUTINE

3DD0 DB00  CI:  IN  0  ;
3DD2 E601  ANI  1  ;
3DD4 C2D03D  JNZ  CI  ;
3DD7 DB01  IN  1  ;
3DD9 E67F  ANI  7FH  ;
3DDB C9  RET  ;

; CONSOLE STATUS SUUOUTINE

3DDC DB00  CSTS:  IN  0  ;
3DDE E601  ANI  1  ;
3DE0 D601  SUI  1  ;
3DE2 9F  SBB  A  ;
3DE3 C9  RET  ;

0400  ORG 1024

0400  STORE:  DS 10240

0000  END
THIS SIMPLE PROGRAM WAS DESIGNED TO DISPLAY 
THE OUTPUT OF THE SOLID STATE MUSIC VIII 
VIDEO INTERFACE BOARD.

THE UPPER HALF OF THE DISPLAY SHOWS THE 64 
UNIQUE GRAPHIC CHARACTERS WHILE THE LOWER 
HALF DISPLAYS THE ASCII CHARACTER SET.

NOTE: TO SELECT GRAPHICS MODE THE 
GRAPHICS POSITION OF S1, THE 
DIP SWITCH, MUST BE CLOSED 
AND DATA BIT D7 SET TO A 
ONE.

THE DIFFERENT GRAPHIC CHARACTERS 
ARE CREATED BY SETTING DATA BITS 
D0-DS. (REFER TO FIG 1) IF THE 
DATA BIT IS SET TO A ONE THE COR- 
RESPONDING SECTION OF THE GRAPHIC 
CHARACTER WILL BE BLACK. IF IT IS 
SET TO ZERO THAT SECTION WILL BE 
WHITE.

EC00 VID 20H MEG00H JVIDEO STARTING ADDRESS

0100 ORS 100H
0102 LXI MVID
0103 3EFH A,0FH
0105 MVI A,0FFH
0107 BC LOOP1: CMP H
0108 CA1001 JZ PROG
010A 78 MOV A,B
010C 23 INX M
010D C30701 JMP LOOP1
0110 2100EC PROG1: LXI MVID
0113 0E09 MVI C,09H
0115 3EFF MVI A,0FFH
0117 114000 LOOP2: LXI D,40H
011A 19 DAD B
011B 0D DCR C
011C CA1001 STUCK1: JZ STUCK
011F 77 LOOP3: MOV M,A
0120 23 INX M
0121 23 INX V
0122 3D DCR A
0123 1D DCR E
0124 1D DCR E
0125 CA1701 JZ LOOP2
0128 C31F01 JMP LOOP3
0000 END

By David Bruce Maerske
VBl-B Parts List

Chip Pack

1 - U17 74LS00
1 - U10 74S04
1 - U21 7408
1 - U18 7432
4 - U11,12,13,20 7474
1 - U4 7486
2 - U5,15 74150
1 - U19 74153
2 - U6,7 74157
1 - U8 74166
4 - U14,22,32,33 74193/74LS193
2 - U29,31 74161
6 - U23,28,34,35,40,41 74367/8097
1 - U42 8131
3 - U1,2,3 75451

Diode Pack

2 - C14,15 2.7uf 20v tant
3 - C3,10,16 39uf 10v tant
1 - D2 IN746/ 3.3volt
1 - D1 IN5242 12volt, 1/2w
1 - Q1 2N2222/2N2222A/2N3904

Socket Pack

3 24 pin sockets
3 8 pin sockets
1 - S1 8 position DIP switch

Hardware Pack

2 sets #6 hardware
1 - J1 4 pin molex plug
1 - J2 2 pin molex plug
1 4 pin moles socket
1 2 pin molex socket
6 molex pins
2 heat sinks
### Memory Pack

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U16</td>
<td>MCM6571AP</td>
</tr>
<tr>
<td>8</td>
<td>U24-27,36-39</td>
<td>2102AL-2 (250 nsec)</td>
</tr>
</tbody>
</table>

### Resistor Pack

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Part Number</th>
<th>Resistance</th>
<th>Tolerance</th>
<th>Color Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>R1,2,5,6,7,8</td>
<td>100 ohm 1/4w 5%</td>
<td>(brown,black,brown)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R3,19</td>
<td>220 ohm 1/4w 5%</td>
<td>(red,red,brown)</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>R4,11-18</td>
<td>2.7K 1/4w 5%</td>
<td>(red,violet,red)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R20,23</td>
<td>1K 1/4w 5%</td>
<td>(brown,black,red)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R21,22</td>
<td>15 ohm 3w</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R9,10</td>
<td>470 ohm 1/4W 5%</td>
<td>(yellow,violet,brown)</td>
<td></td>
</tr>
</tbody>
</table>

### Capacitor Pack

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>C1,2,5,6,7,8,9,C11,12,13</td>
<td>.01uf disc</td>
</tr>
<tr>
<td>1</td>
<td>C4</td>
<td>47-56 pf disc</td>
</tr>
</tbody>
</table>

### Regulator/Xtal Pack

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>U9,30</td>
<td>7805/340T-5</td>
</tr>
<tr>
<td>1</td>
<td>Y1</td>
<td>12.44 mhz xtal</td>
</tr>
</tbody>
</table>

### Misc

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PC board</td>
</tr>
<tr>
<td>25</td>
<td>16 pin sockets</td>
</tr>
<tr>
<td>9</td>
<td>14 pin sockets</td>
</tr>
</tbody>
</table>