ARISIA MICROSYSTEMS

SD SALES COMPANY

P.O. BOX 28810 • DALLAS, TEXAS 75228

Z8800 CPU CARD

by

S. D. SALES

SD SALES COMPANY
P.O. BOX 28810 • DALLAS, TEXAS 75228

Dear Customer,

When we originally designed the Z80 Kit, we assigned non-maskable interupt (NMI) to an unused pin (namely pin 67) on the S100 bus. Unfortunatly, it appears as though the Vector-Graphics Reset and Go board also uses pin 67. In order for our Z80 CPU card to work in a system along with the Reset and Go, the trace on our card going to pin 67 will have to be cut.

Thank you,

SD Sales

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ENGINEERING CHANGE NOTICE

We recommend that the following modifications be made during construction of the Z-80 Kit to correct a timing disparity between the CPU Kit and some of the peripheral boards now on the market. This modification allows the Z-80 Kit to be used with video terminal interfaces and should be used in lieu of the modification outlines on pages 26 and 27. It must be made for any Interface board requiring that PSync and Ø1 be coincidental.

Cut the P.C. Traces to:

IC	PIN
1	4
4	12
5	12,13,3 (Trace 3 is on component side of board)
10	5 (component side of Board)
17	10
19	10
20	10

Connect:

IC	PIN	TO	IC	PIN
2	22		18	8
5	3		18	9
5	3		19	10
5	10		10	12
5	12		8	7
5	13		9	7
10	3		10	11
10	12		24	11
17	10		20	15
18	10		20	10

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STATEMENT OF LIMITED WARRANTY

Most components* sold by S. D. Sales Company are purchased through normal factory distrubution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 90 days following the date of purchase. The defective part must be returned postpaid to S. D. Sales Company within the warranty period.

Any malfunctioning module, purchased as a kit and returned to S. D. Sales Company within the warranty period, which in the judgement of S. D. Sales Company has been assembled with care and not subjected to electrical or mechanical abuse, will either be restored to proper operating condition and returned, regardless of cause of malfunction, at no charge, or a new kit sent to original purchaser, at our option.

Any modules purchased as a kit and returned to S. D. Sales Company which in the judgement of S. D. Sales Company are not covered by the above conditions will be repaired. In no case will this charge exceed $20.00 without prior notification and approval of the owner.

As always, if you are not satisfied with your S. D. Kit, you may return it (within 14 days) in unused (unassembled) condition for a full refund.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

*Used in this kit

1.0 Introduction

Micronix, a high technology consulting firm, has designed the Z8800 CPU Card to the specifications of S. D. Sales Company. The engineering staffs of both Micronix and S. D. Sales Company have performed rigorous testing of the Z8800 in various system configurations to assure of full S-100 compatibility.

The printed circuit card described in the following pages is a very high quality design which will provide the extended capability of the Zilog/Mostek Z-80 microprocessor for those that own an existing Altair or IMSAI. The Z8800 simply replaced the CPU card in either the Altair or IMSAI chassis.

2.0 General

The Z8800 card is a 5 inch by 10 inch printed circuit card kit that is complete in that nothing but a soldering iron and some solder is required to construct it. It comes complete with all hardware, components, and the Z-80 microprocessor chip. After completing the simple construction, which should take 2 to 3 hours, all that is necessary for operation is to replace the existing CPU card of an Altair or an IMSAI and compute away.

The criteria of the design of the Z8800 are as follows:

1. Provide a high quality glass epoxy PC card with tinned copper, plated through holes and gold flashed contacts.

2. Provide every required component for construction.

3. Provide low power schottky logic to take advantage of low power logic.

4. Provide adequate buffering of the bus signals.

5. Provide all of the signals that are presently defined on the Altair bus. The few minor exceptions are fully described in section 5.0.

6. Provide a good quality design which meets or exceeds the worst case conditions expected in the hobbyist environment.

3.0 Software Considerations

"Now that I've got the durn thing together, what do I do next," is probably the most frequently asked question among those who practice the black arts of personal computing. Unless you are in the hobby for the physical therapy of putting electronic kits together, your next step will involve that vile and disgusting perversion, the writing of software. The purpose of this section is to acquaint you with the instruction set of the Zilog Z-80 and to compare it, at a gross level, with the instruction set of the Intel 8080A.

Please keep in mind that the Z-80 will execute 158 instruction types including all 78 of the instruction types found in the Intel 8080A. The only differences between the execution of an 8080A instruction on the 8080A and on the Z-80 are some timing differences summarized in Table 3.1 and that one of the status bits is used to indicate both parity of the accumulator after a logical operation (such as AND) and the arithmetic overflow condition after an arithmetic operation (such as ADD). The additional 80 instructions are unique to the Z-80 and help to provide it with the most powerful instruction set of its kind. The mnemonic structure of the Z-80 instruction set has been divised to provide a logically consistent format.

Table 3.1

Instruction	Clock Cycles 8080A	Z-80
LD r1,r2	5	4
INC r	5	4
INC (HL)	5	4
DEC r	5	4
DEC (HL)	5	4
HALT	7	4
JMP (HL)	5	4
CALL cc,nn	11/17	10/17
RET cc	5/11	5/10
LD SP,HL	5	6
EX (SP), HL	18	19
INC rP	5	6
DEC rP	5	6
OUT n, A	10	11

where

cc = condition (ie: Z, NZ, C, NC, OV, PE, PO)
(rp) = contents of the register pair used as an address
nn = 16 bit number
n = 8 bit number
r = 8 bit register
rp = register pair

All operations are relative to the first operand. As an example, LD B,(HL) will cause the B register to be loaded with the byte found in the memory location pointed to by the HL register pair. This is equivalent to a MOV B,M in the 8080A.

3.1 Load and Exchange Group

The instruction set of the Z-80 is divided into 8 groups. The first instruction group contains the load and exchange instructions of the Z-80. The load instructions cause data to be transfered from a source location to a specified destination. All load instructions must specify both a source and a destination. No changes are made to the data source. In every case except loading the accumulator from either the I or the R registers, the status flags are not modified. In addition to the load instructions there are six exchange instructions. Two of these exchange the HL register pair with either the DE register pair or the memory location pointed to by the SP register. These two instructions are common to 8080A instruction set. Two new exchange type instructions have been added to the Z-80 instruction set. One type exchanges either the IX register or the IY register with the memory location specified by the SP register. The second instruction type exchanges either the AF register pair with its alternate or the BC, DE and HL register pairs with their alternates. This last instruction type is very valuable in fast context switch applications such as interrupt processing. A final pair of instruction types are the PUSH and

POP instructions. These instructions allow the contents of any register pair to be copied onto or loaded from a downward growing stack. These instructions are the same as those in the 8080A except that they are expanded to include the IX and IY registers.

3.2 Block Move and Block Search Group

The second instruction group, the block move and block search instructions, make up a totally new set of instructions. This group of instructions provides the Z-80 with the most powerful set of string manipulation instructions available on any currently available microprocessor. All instructions within this group use one or all of the following register pairs during execution. The HL pair is the source location pointer; the DE pair is the destination location pointer; and the BC pair is the byte counter. Four block move instructions are provided in the Z-80 instruction set: LDI, LDIR, LDD, and LDDR. The LDI instruction takes a byte of data from the source location and deposits it in the destination location. The HL and DE register pairs are then incremented and the BC pair is decremented. The LDIR instruction works in exactly the same manner except that instruction execution is repeated until BC is equal to zero. The LDD and LDDR instructions work in analogous manners to the LDI and LDIR instructions except that the HL and DE register pairs are decremented rather than incremented.

The block search instructions use the HL and BC register pairs just as they were used in the block move instructions. The

accumulator is used in the block search instructions to contain the match value. The four instructions (CPI,CPIR,CPD,CPDR) cause the source byte to be compared with the data in the accumulator. The results of the comparison are stored in the zero status flag; the byte count is decremented and the HL register pair is incremented or decremented as the instruction indicates. If the BC register pair contains a zero after decrementing, the parity/overflow flag bit is set. If the instruction is a repeat type instruction, the process is repeated until a match is found or the byte count is equal to zero.

The block move and block search instructions are invaluable when large strings of data must be manipulated such as in a word processing system or an assembler. All of these instructions are interruptable and therefore do not prevent the CPU from responding to interrupts in a timely manner.

3.3 Arithmetic and Logical Group

The third group of instructions, the arithmetic and logical instructions, are divided into three basic subgroups. Subgroup one is the eight bit arithmetic and logical operations. Subgroup two is the general purpose AF operations. Subgroup three is the sixteen bit arithmetic operations.

The eight bit arithmetic and logical operations are essentially the same as those in the 8080A except that they are expanded to

include IX and IY register addressing. All of these instructions except the INC and DEC instructions assume that the accumulator is one of the operands. In all cases except INC, DEC, and CP, the accumulator receives the result of the operation and the appropriate status flags are modified. The parity/overflow flag bit is a special case in that the parity indication is set by a logical operation and the overflow indication is set by an arithmetic operation. The CP instruction modifies all flags as an arithmetic operation but the result is not stored in the accumulator. Both the INC and DEC instructions may use any register or memory location as a source/destination specification. Both effect all flags except the carry flag.

The general purpose AF register pair operations are the same as those in the 8080A except for the addition of the NEG instruction and the modification of the DAA instruction to take into account a decimal adjust after a subtraction operation. The NEG is an instruction not found in the 8080A. It performs a single instruction two's complementing operation on the accumulator. This replaces the complement and increment operations necessary in the 8080A.

The sixteen bit arithmetic operations contain some new and very useful instructions. The sixteen bit INC and DEC instructions operate in the same manner as the 8080A instructions but are expanded to include the IX and IY registers. The ADD instruction with the HL register pair as the destination location is identical to the

equivalent 8080A instruction. The ADD instruction has been expanded to allow the IX and IY registers to act as destination locations. This expansion will allow the BC, DE, SP and either the IX or IY register pairs to be added to either IX or IY respectively. This operation will effect only the carry flag. In addition to the preceding instructions, the Z-80 has a sixteen bit ADC and a sixteen bit SBC instruction. These instructions use the HL register pair as the destination location and use BC, DE, HL and SP as valid source locations. All flags are modified by these instructions. These instructions greatly facilitate extended sixteen bit arithmetic operations.

3.4 Rotate and Shift

A powerful series of instructions are contained in the fourth instruction group. In the 8080A, all rotates occured with the accumulator as operand. The Z-80 uses the same four rotate operations but allows any eight bit register or memory location to be directly manipulated. For memory operations, the location is specified either by HL or by one of the index registers plus a displacement. The Z-80 also contains a shift left operation and two shift right operations. The shift operations use the same operands as the rotate instructions and provide a useful tool for a wide varity of applications. Also unique to the Z-80 are two instructions which allow a BCD digit to be rotated out of or into a memory location to or from the less significant four bits of the accumulator. This is a tremendous aid in BCD arithmetic. The

operand, specified by the HL register pair may be rotated either left or right.

3.5 Bit Manipulation Group

The fifth instruction group, bit manipulation group, contains three instruction types. These instruction types allow any bit located in any general purpose register or memory location to be set, reset or tested. The zero flag records the result of a bit test. No flags are effected by the set and reset operations.

3.6 Jump, Call and Return Group

The sixth instruction group contains the jump, call and return instruction type. All of the instructions within this group manipulate the sixteen bit PC register. The jump instruction type may be either an unconditional or conditional jump. The conditional jump tests the status of the carry, parity/overflow, zero and sign flags within the flag register.

The jump instruction type uses one of three addressing modes. These modes (Absolute, Relative, or Register Indirect) allow for a choice of instruction types to meet any requirement. The Absolute addressing mode of a jump instruction type loads the PC register with the two bytes of data immediately following the Opcode of the jump. This mode exists in the 8080A.

The Relative addressing mode for a jump type instruction is new in the Z-80. This instruction is a two byte instruction in which the second byte is a signed two compliment displacement which

is added to the PC register to form the new execution address. This addressing mode allows the most common types of jumps such as loops and conditional jumps around short blocks of code to be accomplished with two instead of three bytes of code. When using this instruction type, calculate all displacements from the start of the next instruction. The relative addressing range is +129 to -126 bytes as measured from the jump instruction Opcode. This instruction type is not found in the 8080A.

Register Indirect type of jump instruction causes the contents of the PC register to be unconditionally replaced by the contents of the HL register pair, IX or IY. For table driven systems and other software applications in which the final execution address is calculated dynamically, this instruction type is essential. This instruction type is an expansion of the original 8080A instruction equivalent.

A second member of this instruction group is the Call type instruction. A call instruction pushes the memory location of the instruction immediately following the CALL onto the stack and then branches to the specified address. The Z-80 implements two types of Call instructions. The first type is the RST instruction. This one byte instruction allows a very convenient way to call commonly used subroutines such as I/O routines. The RST instruction causes execution control to be transfered to one of eight locations in the

64 byte memory. This instruction functions just as the equivalent instruction operates in the 8080A.

The second type of call instruction is the CALL. CALL is a three byte instruction in which the second and third bytes specify the subroutine start address. The CALL instruction exists as either an unconditional or a conditional call just as in the case of the jump type instruction. These are found in the 8080A.

The last member of this instruction group is the return type instruction. This is a single byte instruction and pops the return address from the top of the stack. Three types of return instructions are implemented on the Z-80. Two of these, RETI and RETN, are defined as a return from maskable interrupt and non-maskable interrupt routines respectively. These returns automatically re-enable interrupt processing so that a separate interrupt enable instruction is unnecessary. These are not found in the 8080A.

The third type of return, RET, is a general purpose subroutine return and exists in both a conditional and unconditional form. This type of instruction is also found in the 8080A.

3.7 Input/Output Group

The Z-80 has a considerably expanded set of I/O type instructions. In addition to the input and output instructions which use the

accumulator as the data destination or source, the Z-80 has two additional I/O modes. The first mode takes the I/O port address from the C register and loads data into or out of any register except the C register. In the case of an input into the C register with the port address contained in the C register, only the flag register is effected. This allows flags to be tested without disturbing any register. The register indirect I/O instructions are not found in the 8080A.

The second I/O mode is a block transfer type instruction. These instructions take the port address from the C register, the byte count from the B register and the destination/source address from the HL register pair. These block transfer instructions allow either incrementing memory addressing or decrementing memory addressing and also allow either repeat until the B register is equal to zero or no repeat. With this mode of instruction up to 256 bytes of data may be transfered with extreme ease. The block transfer instructions are not found in the 8080A.

3.8 CPU Control Group

This instruction group contains those instructions which are used to establish the state of the CPU. The NOP instruction effects no register and is used to delete an instruction or group of instructions without re-assembling the code. It also is used

to provide space for expansion of code. The HALT instruction causes the CPU to begin executing internally generated NOP instructions until the CPU is reset or until an interrupt request is received. This instruction does not effect the memory refresh operations of the CPU. The DI and EI instructions disable and enable respectively the maskable interrupt.

The final group of three instructions set up the interrupt response modes. The Z-80 has three interrupt response modes. The first mode, mode zero, allows the interrupting device to jam any instructions onto the data bus and the CPU will execute it. This mode is the default mode and is the same interrupt responce as the 8080A.

Mode one is a simplified interrupt mode in which the CPU will automatically execute an RST to location 56 in responce to an interrupt request. This mode requires no special interrupt processing hardware external to the CPU.

The third mode, mode two, is the most powerful interrupt processing mode. When an interrupt request is received, the CPU will accept an eight bit address from the interrupting device. These bits form the lower order bits of an interrupt vector table address. The high order bits are taken from the I register. Once the CPU has formed this address, the contents of location pointed to by that address and the next location are loaded into the PC register after the current PC register contents are pushed

onto the stack. This allows up to 128 interrupt processing routines to be directly addressed. This facility is the most powerful interrupt processing scheme currently available on any micro-processor.

4.0 Z-8800 Software Applications

One of the most vexing questions that anyone can ask a computer hobbyist is "what can you do with it?" The hobbyist is bombarded with this question by his wife, friends, business associates and anyone else who finds out about his new found joy--in other words anyone who will stand next to him for two or three seconds. What can he say?

Basically the question can be answered in one of two ways. First of all, his home system is for his own enjoyment. By loading a language processor such as BASIC into his system, the hobbyist has the Universe to choose from. He may be the commander of the USS Enterprise on a mission in deep space. He may be the king of old Babalon and be making the decisions that will affect the lives of all his subjects. He may be observing the growth of "cells" in the game of Life or the rise and fall of the stockmarket in real life. In short, he could be doing anything to amuse himself. To this end, the Z-8800 will support, with little or no modification, any of the BASIC interpreters written for the Altair processor. In particular, the 5K BASIC from Processor Technology will run very well on the Z-8800 with no modification.

The second answer to the question of "what good is it?" can be shown by reviewing, in short form, the history of computing. Initially the principles of modern digital computing were established because a man saw no reason for others to perform the repetitive calculations required to produce a book of logrithms. Babbage saw a need for automation of the process and tried but failed to solve the problem. He did, however lay down the needed theoretical basis for the digital computer. Later, as men needed to calculate the ballistic paths of artillery shells, the same situation was seen, men performing tedious and repetitous solutions to equations. This time technology was equal to the task and the first "computer" was created. In short, computers have been used to perform tasks for men which have been either too tedious or too time consuming. In the past these problems have been of tremendous magnitude. It was too expensive for the computer to be applied to the more mundane problems of life. Not so now. The computer hobbyist may now harness the power of the computer to make his personal life easier. Perhaps he needs some method of writing letters which will allow him to write more frequently and more clearly. A word processing system will help fulfill this need. Maybe he has trouble remembering when to pay the bills or when Aunt Jane is having her birthday. A computerized calendar can aid there. Or his need may be more exotic and he wants to simulate occupancy

in his home during his absence for his vacation. Again a computer system can provide this type of control for his home. Whatever the need, a home system can probably be of service. The uses are limited only by your imagination. The Z-8800 can be a powerful building block in this home system. With the great power of its instruction set most applications can be easily implemented. Because the hobbyist is not usually rich, the system must be as inexpensive as possible. The Z-8800 will allow you to get the most out of your memory space. All told, you will get more with a Z-8800 in your system.

5.0 Hardware Description

5.1 Z-80 features compared to the 8080 and the 6800

Zilog claims that the Z-80 represents the third generation microprocessor. A tabulation of the superior features of the Z-80 compared to the Intel 8080 and the Motorola 6800 is presented in table 5.1.

Table 5.1

Item	Z-80	8080	6800
Number of instructions	158	78	72
Number of internal registers	17	7	6
Number of addressing modes	10	7	8
Memory to memory, memory to I/O block transfers in one instruction	yes	no	no
Block search in a single instruction	yes	no	no
Bit manipulations in a single instruction	yes	no	no
Non-maskable interrupt	yes	no	yes
Fully decoded control signals without external circuitry	yes	no	no
Capability for DMA	yes	yes	yes
Syncing slow devices	yes	yes	no
Separate I/O	yes	yes	no

Table 5.1 (cont.)

Item	Z-80	8080	6800
Clock phases	1	2	2
Clock voltage	4.2v	8.4v	4.8v
Clock frequency	DC-2.5MHZ	0.5-2MHZ	0.1-1MHZ
Memory refresh circuitry on CPU chip	yes	no	no
Voltages needed	+5v	+5,-5,+12	+5
Need external status latches	no	yes	no
TTL compatible	yes	no	yes

5.2 Description of Z-80 Bus

Every attempt was made to create each of the signals on the Altair bus. This was accomplished in all important ways, however, some minor differences occur and are pointed out in the following pin description.

Z-80 Bus for Altair or IMSAI

Pin	Signal Name	Description
1	+8vdc	Unregulated input to +5v regulator
2	+16vdc	Unregulated--not used on Z-8800
3	xrdy	Pulling this line low will cause the CPU to enter WAIT state until this line goes high
4 to 11	VIØ - VI7	Reserved for vectored interrupt inputs. Not required for Z-8800
12 to 17	not defined	For future use

Z-80 Bus for Altair or IMSAI (cont.)

Pin	Signal Name	Description
18	$\overline{\text{STA DSB}}$	Provides the capability to tri-state the SINP, SOUT, SINTA, SMEMR, SWO, SMI, and SHLTA signals.
19	$\overline{\text{c/c DSBL}}$	Provides the capability to tri-state the PWR, PWAIT, PDBIN, PHLDA, and PSYNC signals
20	$\overline{\text{UNPROT}}$	Input to the memory protect flip-flop on a given memory board. Not used for Z8800
21	SS	Single step signal
22	$\overline{\text{ADD DSBL}}$	Provides the capability to tri-state the address lines
23	$\overline{\text{DO DSBL}}$	Provides the capability to tri-state the Data Out lines
24	Ø2	Phase 2 clock
25	Ø1	Phase 1 clock
26	PHLDA	The presence of a "true" here indicates that the Data and address lines have gone tri-state
27	PWAIT	A "true" here indicates that the CPU is in a wait state
28	PINTE	This is the hardware interrupt enable which on the Z-8800 is tied III.
29	A5	Address line #5
30	A4	Address line #4
31	A3	Address line #3
32	A15	Address line #15

Z-80 Bus for Altair or IMSAI (cont.)

Pin	Signal Name	Description
33	A12	Address line #12
34	A9	Address line #9
35	DO1	Data Out line #1
36	DOØ	Data Out line #Ø
37	A1Ø	Address line #1Ø
38	DO4	Data Out line #4
39	DO5	Data Out line #5
40	DO6	Data Out line #6
41	DI2	Data Input line #2
42	DI3	Data Input line #3
43	DI7	Data Input line #7
44	SMI	Status Output signal that indicates that the present machine cycle is an op-code fetch.
45	SOUT	Status Output signal that the address bus contains a valid device address and the data bus will contain the output data when PWR is active
46	SINP	Status Output signal which indicates that the address bus contains the device address and the input data should be put on the data bus when PDBIN is active
47	SMEMR	Status Output which indicates that the data bus will be used for memory read
48	SHLTA	Signal output which acknowledges a software halt instruction

Z-80 Bus for Altair or IMSAI (cont.)

Pin	Signal Name	Description
49	$\overline{\text{CLOCK}}$	2MHZ clock output from the Oscillator
50	GND	Ground
51	+8v	Unregulated voltage +8v
52	-16v	Negative 16v unregulated
53	$\overline{\text{SSW DSBL}}$	Disables the data input buffers so the input from the sense switches may be stroked onto the bidirectional data bus right at the processor
54	$\overline{\text{EXT CLR}}$	Clear signal for I/O devices (front panel switch closure to ground)
55-66		Not used
66	$\overline{\text{RFSH}}$	This output signal indicates when the lower seven bits of the address lines hold the refresh addresses for dynamic memory (unique to Z80)
67	$\overline{\text{NMI}}$	Input signal for the non-maskable interrupt (not on Altair Bus)
68	MWRT	Output signal (from front panel) which indicates that the current data on the Data Out bus is to be written into memory
69	$\overline{\text{PS}}$	Reserved for Protect Status
70	PROT	Reserved for Protect
71	RUN	Indicates that the RUN/STOP flip flop is reset
72	PRDY	Processor command/control input that controls the run state of the processor; if the line is pulled low the processor will enter a wait state until the line is released

Z-80 Bus for Altair or IMSAI (cont.)

Pin	Signal Name	Description
73	$\overline{\text{PINT}}$	The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request
74	$\overline{\text{HOLD}}$	Processor command/control input signal which requests the processor to enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle
75	$\overline{\text{RST}}$	Processor command/control input; while activated the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	Processor command/control output provides a signal to indicate the beginning of each machine cycle
77	$\overline{\text{PWR}}$	Processor command/control output used for memory write or I/O output control: data on the data bus is stable while the $\overline{\text{PWR}}$ is active
78	PDBIN	Processor command/control output signal indicates to external circuits that the data bus is in the input mode
79	AØ	Address line #Ø
80	A1	Address line #1
81	A2	Address line #2
82	A6	Address line #6
83	A7	Address line #7
84	A8	Address line #8
85	A13	Address line #13

Z-80 Bus for Altair or IMSAI (cont.)

Pin	Signal Name	Description
86	A14	Address line #14
87	A11	Address line #11
88	DO2	Data Out line #2
89	DO3	Data Out line #3
90	DO7	Data Out line #7
91	DI4	Data In line #4
92	DI5	Data In line #5
93	DI6	Data In line #6
94	DI1	Data In line #1
95	DIØ	Data In line #Ø
96	SINTA	Status output signal to acknowledge signal for interrupt request
97	SWO	Status output signal indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	$\overline{\text{DEBUG}}$	This input signal replaces the SSTACK signal on the Altair/IMSAI bus and is used to force the A14 and A15 lines high when this signal goes low. This is used for a monitor program which starts at location C000 (unique to Z-8800)
99	$\overline{\text{POC}}$	Power on clear
100	Ground	Ground

Z8800-8080A CPU COMPARISON

The S. D. Z8800 will operate in exactly the same manner as your old 8080 card except as noted below.

You will notice immediately that the "Stack" and "Interrupt Enable" panel lights are continually on. These signals are not provided by the Z-80 (or any Z-80 CPU card), therefore these lights are always lit.

You may notice also that the Address lights do not "flicker" in the same manner as on your 8080A card during a program "RUN". This is due to the slightly different timing that the Z-80 exhibits on the address and data lines. This difference is visual only, and is of no practical concern.

To be assured of proper card operation, the IMSAI recommended front panel mod is a MUST. The specifics of this change are (or should have been made) available from IMSAI or their dealers. The effect of this modification was to insure that a "M WRITE" signal does not occur during an "Output" instruction.

Notes on the Processor Tech VDM

To use the Z8800 with the VDM requires a slight modification on the VDM board.

This mod is necessary because $\overline{WR}$ occurs one "T" state earlier in the Z-80 than on the 8080A. What needs to be done is to disconnect PSYNC from the VDM board. This causes the VDM to strobe the memory and port address comparator once every "T" state as opposed to once every "M" state. This mod will not

affect the normal operation of the VDM when used with the Z8800 or an 8080A CPU.

The mod is as follows: Remove IC 18 (74LS132) from its socket. Bend Pin 5 up and replace IC 18 making sure Pin 5 DOES NOT make contact.

NOTES ON DAZZLER

When DMA devices such as the Cromemco Dazzler is used with our Z8800 CPU, a modification is needed. The trace going to Pin 1 of IC 19 should be cut and Jumpered to Pin 8 of IC 19. This insures the CPU clocks will be on the buss during DMA,

Z8800 CPU CARD

by S D Sales

PARTS LIST

Z80A Model

4	74LS00
2	74LS02
1	7404DC
3	74LS04
1	74LS74
2	74109
1	74LS123
9	8T97, or 74LS367
2	8T98, or 74LS368
1	Z-80 (Z-80A)
1	10pf mica
1	27pf mica
1	108pf mica
16	.01 Mfd disc
1	33 Mfd Tantalum
3	10 Mfd Tantalum
1	367pf mica
2	7805
2	Heatsinks
1	2 MHZ xtal (4 MHz xtal)
2	IN 4148
11	14 pin sockets
15	16 pin sockets
1	40 pin socket
1	Molex connector
2	6-32 screw & nut
22	1K OHMS
13	4.7K OHMS
1	3.9K OHMS
1	680 OHMS
2	270 OHMS
1	330 OHMS
1	10K OHMS
1	PC Board
2	Buss Bars

PARTS LIST BY PACK

PACK #1

11 14 pin sockets ✓✓
15 16 pin sockets ✓
1 40 pin sockets ✓
1 1 Molex connector ✓

PACK #2

16 .01 Mfd disc cap ✓
1 10pf mica ✓
1 27pf mica ✓
1 108pf mica ✓
1 367pf mica ✓ 330pf
3 10 Mfd Tantalum ✓
1 47 Mfd Tantalum ✓
22 1K OHM ¼W Resistors 21
13 4.7K OHM ¼W Resistors 14
1 330 OHM 1/8W Resistors ✓
2 270 OHM REsistors ✓
1 3.9K OHM Resistors ✓
1 10K OHM Resistors ✓
1 680 OHM Resistors ✓
2 IN 4148 Diodes ✓
2 Heatsink W/Hardware ✓ 2screws,nuts
1 2.000 MHZ xtal ✓

extra 2.0K ¼W res
2.2K ¼W res

PACK #3

9 8T97, or 74LS367 ✓
2 8T98, or 74LS368
1 7404DC ✓
4 74LS00 ✓
2 74LS02 ✓
3 74LS04 ✓
1 74LS74 ✓
2 74109 ✓
1 74LS123 ✓
1 Z-80 ✓
2 7805 ✓

1 PC Board ✓
2 Buss Bars ✓

CONSTRUCTION

Double check all parts against the Parts list. If any differences are noted please call us on our toll free line 1-800-527-3460. If all is O.K., procede with the assembly.

1. ✓ Install the IC sockets in their proper locations.

2. Install the Resistors as follows;
   - (✓) R1-1K OHM ¼W Brown, Black, Red
   - (✓) R2,R3-270 OHM ¼W Red, Violet, Brown
   - (✓) R4-4.7K OHM ¼W Yellow, Violet, Red
   - (✓) R5-3.9K OHM ¼W Orange, White, Red
   - (✓) R6-680 OHM ¼W Blue, Gray, Brown
   - (✓) R7-10K OHM ¼W Brown, Black, Orange
   - (✓) R8,R9-4.7K OHM ¼W Yellow, Violet, Red
   - (✓) R10-1K OHM ¼W Brown, Black, Red
   - (✓) R11-4.7K OHM ¼ W Yellow, Violet, Red
   - (✓) R12-1K OHM ¼ W Brown, Black, Red
   - (✓) R13-R15-1K OHM ¼W Brown, Black, Red
   - (✓) R16,R17-1K OHM ¼W Brown, Black, Red
   - (✓) R18-330 OHM 1/8W Orange, Orange, Brown
   - (✓) R19-R21-1K OHM ¼W Brown, Black, Red
   - (✓) R22-4.7K OHM ¼W Yellow, Violet, Red
   - (✓) R23-R25-1K OHM ¼W Brown, Black, Red
   - (✓) R26-R33-1K OHM ¼W Brown, Black, Red R32 from spares
   - (✓) R34-R41-4.7K OHM ¼W Yellow, Violet, Red

3. Install Diodes D1, D2 Banded end (cathode) as shown on the PC Board.

4. Install the capacitors as follows:
   - (✓) C1-C3 10 Mfd Tantalum, note proper polarity
   - (✓) C4-10pf mica
   - (✓) C5-108pf mica
   - (✓) C6-27pf mica
   - (✓) C7-33 Mfd Tantalum 47, note proper polarity
   - ( ) C8-C23 .01 Mfd disc
   - (✓) C24-367pf mica 330

5. Install the two 5 volt regulators with the heat sinks, using the 6-32 hardware supplied.

6. Install the crystal.

7. Install the Board into the computer (extender Board recommended) measure the output of the 5 volt regulators, should be between 4.75 and 5.25 volts.

8. Install the two buss bars into the Board. Note that above the two rows of IC's (IC3 to IC14 and IC 15 to IC26) on the PC Board the component stencil shows a white line with holes spaced 3/4". Also note the buss bars have pins protruding below them with this same spacing. Install the buss bars into the Board from the component side. The buss bars should be purpendicular to the Board and parallel to the two rows of IC's. Solder one pin on the ends of each buss bar. Inspect the Board and verify the buss bars are straight and properly seated. Now carefully solder the remaining pins of the buss bars. Note that the buss bars are made of metal and will require a little longer to solder due to the heatsink action of the metal. The buss bars will also be hot when you finish soldering, so be careful. The buss bars provide a low impedence path for the system Vcc.

9. If you have an Altair, install the white molex connector into the special holes in the upper right hand corner of the Board. A 16 pin socket is provided to the left of the molex connector for IMSAI computers.

10. Install the IC's in their sockets as follows, pin 1 of all IC's (except IC 2) are toward the top of the board.

( ) IC 1 7404DC
( ) IC 3,5 74LS00
( ) IC 4 74LS04
( ) IC 6 74LS02
( ) IC 7 74LS123
( ) IC 8 74109
( ) IC 9 74109
( ) IC 10 74LS74
( ) IC 11 74LS04
( ) IC 12 74LS00
( ) IC 13 8T97,or 74LS367
( ) IC 14 8T97,or 74LS367
( ) IC 15 74LS00
( ) IC 16 8T97,or 74LS367
( ) IC 17 74LS04
( ) IC 18 74LS02
( ) IC 19 8T97,or 74LS367
( ) IC 20 8T98,or 74LS368
( ) IC 21 8T97,or 74LS367
( ) IC 22 8T97,or 74LS367
( ) IC 23 8T97,or 74LS367
( ) IC 24 8T98,or 74LS368
( ) IC 25 8T97,or 74LS367
( ) IC 26 8T97,or 74LS367
( ) IC 2 Z-80 NOTE: Static sensitive, use MOS handling practices.

Remaining – Altair connector
– 4.7K Res - extra
2.0K 2.K Res

SOLDERING TECHNIQUE

THE NEED

THE ASSEMBLY OF ELECTRONIC COMPONENTS IS ESSENTIALLY THE EXERCISE OF THE ART OF SOLDERING. IF THE MANY CONNECTIONS ARE SOLDERED PROPERLY, THE RESULTING ASSEMBLY WILL NORMALLY OPERATE PROPERLY RIGHT FROM THE FIRST APPLICATION OF POWER. A HASTY JOB HERE CAN MEAN ENDLESS HOURS TRYING TO LOCATE SHORT CIRCUITS OR INTERMITTENT CONNECTIONS.

THE SOLDER

USE A #20 GAUGE RESIN OR ROSIN CORE SOLDER WITH A RATIO OF 63% TIN AND 37% LEAD. A 60/40 RATIO IS ACCEPTABLE. "KESTER" AND "ERSIN" ARE TWO DEPENDABLE BRANDS OF SOLDER. ACID CORE SOLDERS OR ACID FLUX MUST NOT BE USED AS THEY WILL CORRODE ELECTRONIC JOINTS AND WILL DAMAGE PRINTED CIRCUIT BOARDS.

THE SOLDERING IRON

USE A SMALL, 30 WATT MAXIMUM IRON WITH A SMALL, CHISEL SHAPED TIP. TOO MUCH HEAT WILL DAMAGE BOTH COMPONENTS AND BOARDS. SOLDERING GUNS ARE TOO HOT AND SHOULD NOT BE USED.

HEAT THE IRON, WIPE ITS TIP QUICKLY ON THE DAMP SPONGE, AND APPLY A TINY AMOUNT OF SOLDER TO THE TIP - JUST ENOUGH TO MAKE IT SILVER IN COLOR BUT NOT SO MUCH THAT IT WILL DRIP OFF. THIS CLEANING PROCEDURE SHOULD BE REPEATED WHENEVER THE SOLDER OF THE TIP OF THE SOLDERING IRON BEGINS TO THICKEN OR TAKE OF A BROWNISH COLOR.

REMOVAL OF MULTI-PIN SOLDERED-IN PARTS

CAUTION

IF FOR ANY REASON, IT BECOMES NECESSARY TO REMOVE A SOLDERED-IN PART HAVING MORE THAN JUST TWO LEADS, DO NOT TRY TO REMOVE THE PART INTACT. IT CAN BE DONE BUT ONLY WITH GREAT RISK OF DAMAGING THE PRINTING CIRCUIT BOARD IN THE PROCESS.

HOLD THE PRINTED CIRCUIT BOARD IN WELL PADDED JAWS OF A BENCH VICE TO AVOID DAMAGE.

REMOVAL OF SOLDERED-IN IC SOCKETS

CRUSH THE PLASTIC BODY WITH A PAIR OF PLIERS TO PULL THE PINS FROM THE BODY. GENTLY REMOVE THE PINS FROM THE TOP OF THE BOARD WITH NEEDLE NOSED PLIERS WHILE TOUCHING THE JOINT ON THE OTHER SIDE OF THE BOARD WITH THE TIP OF THE IRON. DO NOT USE FORCE. THE PIN WILL COME OUT QUITE EASILY ONCE THE SOLDER MELTS.

CLEAR THE HOLES OF ANY EXCESS SOLDER BY RAPIDLY INSERTING ANY REMOVING A PIECE OF WIRE WHILE VERY BRIEFLY HOLDING THE SOLDERING IRON 1O THE HOLE AT THE BACK OF THE BOARD.

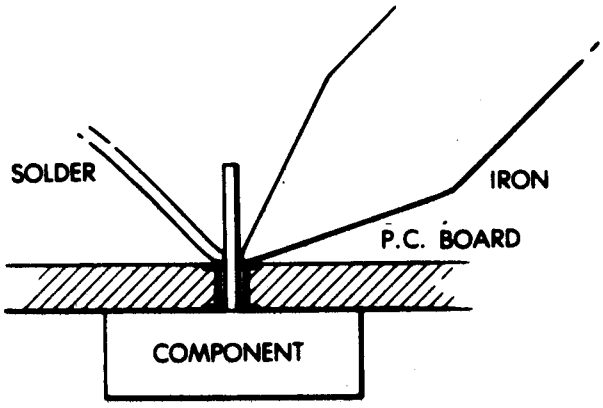
REMOVAL OF SOLDERED-IN INTEGRATED CIRCUIT CHIPS

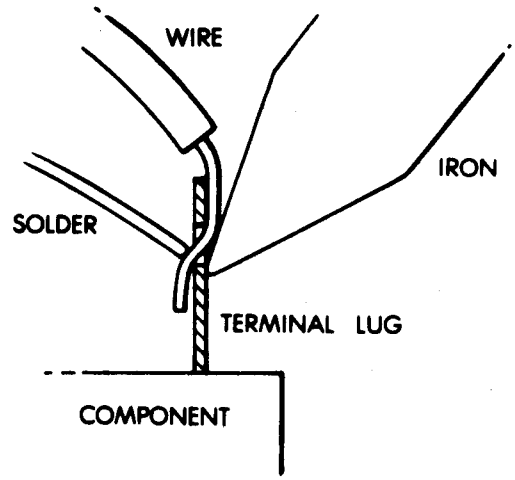
CUT EACH PIN WITH A PAIR OF DIAGONAL CUTTERS AT A POINT BETWEEN THE CHIP AND THE PRINTED CIRCUIT BOARD WHICH IS AS CLOSE TO THE CHIP AS POSSIBLE SO THAT THERE IS ENOUGH OF THE PIN SHOWING ABOVE THE BOARD TO BE GRASPED BY NEEDLE NOSED PLIERS WHILE REMOVING AS DESCRIBED ABOVE.

THE PROCEDURE

THE ENTIRE SOLDERING OPERATION SHOULD TAKE LITTLE MORE THAN TWO SECONDS PER JOINT. THE SEQUENCE IS AS FOLLOWS:

TOUCH THE TIP OF THE SOLDERING IRON TO THE JOINT, AS SHOWN BELOW, SO THAT BOTH THE CONDUCTORS TO BE JOINED ARE SIMULTANEOUSLY HEATED SUFFICIENTLY TO MELT THE SOLDER.





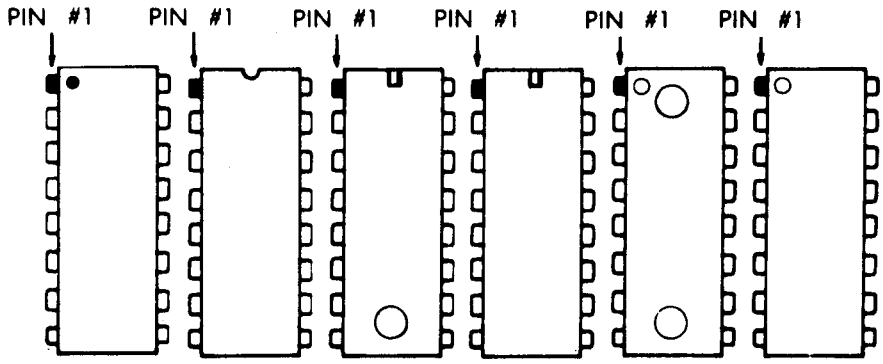
TOUCH THE END OF THE SOLDER ROLL TO THE JOINT, AS SHOWN ABOVE, JUST LONG ENOUGH TO LET NO MORE THAN A 1/8" LENGTH MELT INTO THE JOINT. TOO MUCH SOLDER WILL SHORT CIRCUIT THE BOTTOM OF THE BOARD OR FLOW THROUGH THE HOLES AND SHORT CIRCUIT THE TOP OF THE BOARD. THE MELTED SOLDER WILL APPEAR WET AND SHINY. IT WILL QUICKLY FLOW COMPLETELY AROUND THE WIRE AND OVER THE SURFACE TO WHICH THE WIRE IS ATTACHED.

REMOVE THE SOLDERING IRON AS SOON AS BOTH SURFACES HAVE BEEN COMPLETELY WETTED. REMEMBER, THE TOTAL TIME FROM APPLICATION TO REMOVAL OF THE SOLDERING IRON SHOULD BE ONLY TWO OR THREE SECONDS. REMOVAL OF THE SOLDERING IRON TOO SOON 'L RESULT IN AN INCOMPLETE BOND BETWEEN THE METALS, BUT LEAVING THE SOLDERING IRON AT THE JOINT TOO LONG WILL CAUSE HEAT DAMAGE TO BOTH COMPONENTS AND BOARD.

ORIENTATION OF INTEGRATED CIRCUIT CHIPS

EXTREME CARE MUST BE TAKEN TO INSURE THAT EACH INTEGRATED CIRCUIT CHIP IS SO ORIENTED, PRIOR TO INSERTION IN ITS SOCKET, THAT PIN #1 IS AT THE LOCATION SO DESIGNATED ON THE PRINTED CIRCUIT BOARD OR IN THE INDIVIDUAL ASSEMBLY INSTRUCTIONS FOR THE KIT.

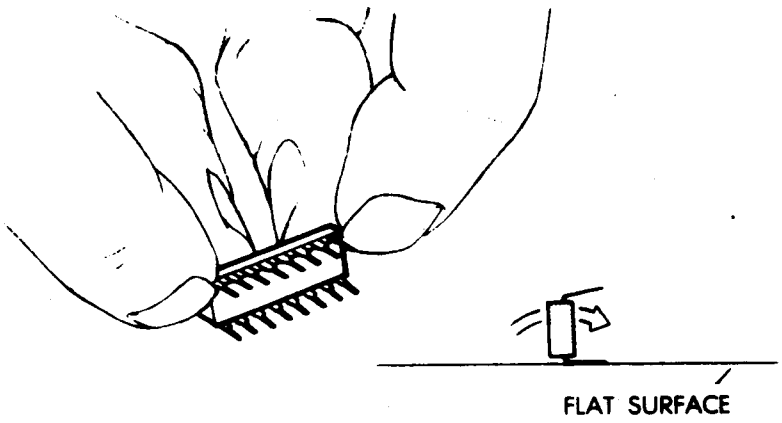
PIN #1 IS, UNFORTUNATELY, DESIGNATED IN A VARIETY OF WAYS DEPENDING UPON THE INTEGRATED CIRCUIT MANUFACTURER. SEVERAL METHODS ARE INDICATED IN THE CHART BELOW. WITH THE LEADS OF THE CHIP POINTING AWAY FROM THE VIEWER, PIN #1 IS IN THE POSITION INDICATED WITH RESPECT TO THE VARIOUS END NOTCHES OR TINY CIRCULAR MARKINGS OR DEPRESSIONS IN ONE CORNER.



INSERTION OF INTEGRATED CIRCUIT CHIPS

BE SURE ALL LEADS ARE STRAIGHT AND PARALLEL. IF NOT, GENTLY STRAIGHTEN AND ALIGN THE BENT PINS WITH NEEDLE NOSED PLIERS.

INTEGRATED CIRCUIT CHIPS USUALLY COME FROM THE MANUFACURER WITH THEIR ROWS OF LEADS SPREAD WIDER THAN THE DISTANCE BETWEEN ROWS OF HOLES IN THE SOCKET INTO WHICH THEY ARE TO BE INSERTED. TO SLIGHTLY CLOSE THE ROWS OF PINS IN A UNIFORM MANNER SO THEY ARE ALIGNED WITH THE SOCKET HOLES, PLACE THE CHIP ON ITS SIDE ON A FLAT SURFACE SO THAT ONE ROW OF PINS IS FLAT AGAINST THE SURFACE AS SHOWN ON THE FOLLOWING PAGE.



HOLDING THE SIDE OF THE CHIP FIRMLY AGAINST THE FLAT SURFACE WITH BOTH HANDS, ROTATE IT A SHORT DISTANCE TOWARD ITS PINS UNTIL IT IS IN A FULL VERTICAL POSITION. THIS WILL PUT ITS BODY AT A RIGHT ANGLE TO THAT ROW OF PINS. PLACE THE OTHER ROW OF PINS ON THE FLAT SURFACE AND REPEAT THE PROCESS AS ABOVE.

PARTIALLY INSERT ALL ICS WITH THE PIN #1 ORIENTED AS SHOWN ON THE ASSEMBLY LAYOUT WHICH IS SILK SCREENED ON THE FRONT OF THE BOARD. THE LAYOUT SYMBOL FOR IC PIN #1 IS DESIGNATED BY A WHITE DOT ADJACENT TO THE UPPER LEFT HAND CORNER OF EACH RECTANGULAR IC CHIP LOCATION SYMBOL. RECHECK TO INSURE THAT EACH PIN IS IN ITS HOLE AND HAS NOT BEEN FOLDED UNDER THE CHIP OR BENT OUTSIDE THE SOCKET. COMPLETE INSERTION EVENLY AND FIRMLY.

UNPLUGGING INTEGRATED CIRCUIT CHIPS

UNPLUGGING AND INTEGRATED CIRCUIT CHIP MUST BE DONE EVENLY FROM BOTH ENDS SIMULTANEOUSLY SO THAT THE PINS WILL NOT BE BENT DURING REMOVAL. GENTLY PRYING WITH A SCREWDRIVER A LITTLE BIT AT A TIME FIRST AT ONE END, THEN AT THE OTHER IS RECOMMENDED. IF ACCESS IS POSSIBLE ONLY FROM ONE END, BE SURE THE SCREWDRIVER IS PUSHED AS FAR IN AS POSSIBLE SO AS TO GIVE A UNIFORM LIFTING ACTION OVER THE FULL LENGTH OF THE CHIP.

POWER ON

PLUG THE BOARD INTO YOUR COMPUTER AND CHECK IT OUT IN ACCORDANCE WITH THE USERS MANUAL PRECEDING THESE ASSEMBLY INSTRUCTION.

S. D. SALES
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