ARE SOCKETS SUPPLIED WITH YOUR VDM-1?

Not if you purchased your kit before May 1, 1976*. Kits purchased before this date are shipped with one socket only, and that socket is for the character generator (IC4).

A set of sockets for the VDM-1 is available from Processor Technology for $19.00, postpaid to U.S. and Canada if full payment accompanies your order. The added convenience in assembly and IC replacement is well worth the added investment in your VDM-1.

If you purchased your kit before May 1 and intend to install sockets for all ICs, follow the assembly procedure given in this manual.

If you do not intend to install sockets for all ICs, replace Step 1 in the procedure with the following.

( ) Step 1. Install 24-pin socket in Area A-6,7 for IC4. Avoid creating solder bridges between pins and traces.

Also, refer to "Loading DIP Devices" in Appendix III of this manual when performing Step 16, 18, 20 and 22.

*Sockets are included in all VDM-1 kits purchased after May 1, 1976 at the new kit price of $179.00.
VDM - 1 ENGINEERING MODIFICATION (PC board rev. A through D)

A modification has been made to the circuit of the VDM-1 which will improve the timing margins in the vertical scrolling circuit. In order to incorporate these design changes in your unit, please carry out the following step before starting step 1 of the assembly instructions:

1. On top side of board cut trace connecting pin 1 of IC 13 with pin 15 of IC 13.

Now proceed with assembly until you reach step 15. After completing step 15, carry out the following steps before continuing with step 16:

2. Cut trace from pin 2 of IC 19 to R 18.
3. Connect a jumper wire from R 18 to pin 7 of IC 13.
5. Connect a jumper wire from pin 1 of IC 13 to pin 10 of IC 15.
6. Connect a jumper wire from pin 15 of IC 13 to pin 5 of IC 13.

PROCESSOR TECHNOLOGY CORPORATION  6200 HOLLIS STREET  EMERYVILLE CA 94608  (415)652-8080  CABLE ADDRESS "PROTECT"
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<td>3.1.5 Cursor Circuit</td>
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<tr>
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<td>3.1.6 Video Circuit</td>
<td>III-5</td>
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<tr>
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<td>3.1.7 Scroll Circuit</td>
<td>III-6</td>
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SECTION I

INTRODUCTION and

GENERAL INFORMATION

VDM-1 VIDEO DISPLAY MODULE
1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the VDM-1 Video Display Module. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components listed in the "Parts List" (Table 2-1) in Section II. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from backward installed components and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 VDM-1 Description

The VDM-1 Video Display Module is not a limited "TV Type-writer". It is an ultra-high speed computer terminal designed to operate within your Altair.

This display module generates sixteen 64 character lines from data stored in a 1024 8-bit byte on-card RAM memory (random access memory). Alphanumeric and control characters (the full 128 upper and lower case plus control ASCII character set) are displayed in a 7 x 9 dot matrix. With its EIA video output, the VDM-1 can be used with any standard video monitor. (A TV set can also be easily modified for use with the VDM-1. See Appendix VI.)

A two-port memory permits random read-write access to the screen memory from the memory bus of the CPU. Other features include:

1. Normal (white-on-black background) video display or inverted (black-on-white background) video display, switch-selectable for entire screen or program-controlled for each character.

2. Video inversion block cursor, switch-selectable blink capability, programmable for each character location.

3. Continuously adjustable display position, both vertical and horizontal.

4. Text blanking (switch selectable) from CR control character to end of line and from VT control character to end of screen, excluding CR or VT character.
5. Optional blanking of all control characters (switch selectable).

6. Program-controlled scrolling of display in increments of one to 16 lines without rewriting memory.

7. "Window shade" blanking of text above desired starting location, program controllable.

8. Scroll timer on board available for test by processor.

1.2.2 Receiving Inspection

When your module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology should it become necessary to do so.) If your VDM-1 kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, the parts supplied with the module, as well as the assembled module, are warranted against defects in materials and workmanship for a period of 6 months after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (e.g. DM8131) and/or a complete description (e.g., 6.8 ohm, ½ watt, 5% resistor).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the module to Processor Technology, first obtain authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the module, proceed as follows:

1. Write a description of the problem.

2. Pack the module with the description in a container suitable to the method of shipment.

3. Ship prepaid to Processor Technology, 6200 Hollis Street, Emeryville, CA 94608.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.
SECTION II

ASSEMBLY
and
TEST

VDM-1 VIDEO DISPLAY MODULE
2.1 ASSEMBLY TIPS

1. Scan Section II in its entirety before you start to assemble the VDM-1.

2. In assembling your VDM-1, you will be following an integrated assembly-test procedure. Such a procedure is designed to progressively insure that individual sections of the module are operating correctly. IT IS IMPORTANT THAT YOU FOLLOW THE STEP-BY-STEP INSTRUCTIONS IN THE ORDER GIVEN.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. When installing components, make use of the assembly aids that are incorporated on the VDM-1 PC board and the assembly drawing: (These aids are designed to assist you in correctly installing the components.)

   a. The circuit reference (R3, C10 and IC20, for example) for each component is silk screened on the PC board near the location of its installation.

   b. An alphanumeric "grid", that divides the board into 90 areas, is also silk screened on the PC board. (In the assembly instructions, grid coordinates are used to define the areas in which specific components are located.)

   c. Both the circuit reference and value or nomenclature (1.5K and 7406, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that the color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5).

6. Install disc capacitors as close to the board as possible.

7. Should you encounter any problem during assembly, call on us for help if needed.

2.2 ASSEMBLY PRECAUTIONS

2.2.1 Handling MOS Integrated Circuits

Several MOS integrated circuits are used in the VDM-1, and they can be damaged by static electricity discharge. Always handle
MOS ICs so that no discharge will flow through the IC. Also, avoid unnecessary handling and wear cotton--rather than synthetic--clothing when handling these ICs.

2.2.2 Soldering

1. Use a low-wattage iron, 25 watts maximum.

2. Solder neatly and quickly as possible.

3. DO NOT press top of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

4. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

5. The VDM-1 uses a circuit board with plated-through holes. Solder flow through to the component side of the board can produce solder bridges. Check for such bridges after each installation.

6. The VDM-1 circuit board has an integral solder mask (green lacquer) that shields selected areas on the board. This mask minimizes the chances of creating solder shorts during assembly.

7. Additional pointers on soldering are provided in Appendix III of this manual.

2.2.3 Installing and Removing VDM-1

NEVER install the VDM-1 in, or remove it from, the computer with the power on. To do otherwise can damage the board.

2.2.4 Installing and Removing Integrated Circuits

NEVER install or remove integrated circuits with power applied to the VDM-1.

2.3 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the VDM-1:

1. Needle nose pliers
2. Diagonal cutters
3. Controlled heat soldering iron, 25 watts
4. Sharp knife
5. 60-40 rosin-core solder (supplied)
Revision C Boards: Ignore Step 2, section 2.6 (page II-3), and instead follow these instructions when installing C 34 on page II-8:

1. Scrape solder mask (green lacquer) from +5V trace at C 34 (F2 coordinate)

2. Bend leads of Q1 (2N2907) as indicated

3. Attach C and E leads of Q1 to C 34 as shown.

4. Install C34 and Q1 as shown. Solder B lead of Q1 to +5V trace.

Schematic:
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

SECTION II

6. Volt-ohm meter
7. Oscilloscope (optional)
8. IC test clip (optional)

2.4 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1). If you have difficulty in identifying any parts by sight, refer to Figure 2-1.

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper righthand corner of the board when the edge connector is positioned at the bottom of the board. In this position, the component (front) side of the board is facing up. Subsequent position references assume this orientation.

2.6 ASSEMBLY-TEST PROCEDURE

Refer to assembly drawing in Section IV.

CAUTION

THIS DEVICE USES SEVERAL MOS INTEGRATED CIRCUITS WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE MOS IC SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN HANDLING THESE ICs.

( ) Step 1. Install sockets in locations IC1 through IC48. Each socket should be installed with its end notch oriented as indicated on the assembly drawing. Avoid creating solder bridges between pins and traces.

( ) Step 2. Install Q1 (2N2907) in Area G-2. The emitter lead (closest to tab on can) is oriented toward top of board and the base lead to the left. Push straight down on transistor until it is stopped by the leads. Solder and trim.

( ) Step 3. Install all resistors in numerical order in the indicated locations. Bend leads to fit distance between mounting holes, insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

Refer to footnotes at the end of this step before installing flagged (*, **, #, ##, @ or @@) resistors.

II-3
## Table 2-1. VDM-1 Video Display Module Parts List.

<table>
<thead>
<tr>
<th>INTEGRATED CIRCUITS</th>
<th>TRANSISTORS</th>
<th>DIODES</th>
<th>CRYSTALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 4001 (IC30) 1 7406 (IC1) 4 74LS163 (IC2,20,21,22)</td>
<td>1 2N2907 (Q1)</td>
<td>1 IN5225B (D1)</td>
<td>1 HC-18/U (Y1), 13.478 MHz</td>
</tr>
<tr>
<td>2 4029 (IC26,27) 2 74LS08 (IC33,34) 1 74166 (IC3)</td>
<td></td>
<td>1 IN4148 (D2,3)</td>
<td></td>
</tr>
<tr>
<td>2 4042 (IC31,32) 2 74LS10 (IC9,40) 3 74LS175 (IC5,6,17)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 4049 (IC25) 1 74LS20 (IC7) 2 8097 or 8T97 (IC38,39)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 MC6574,6575 or 1 74LS86 (IC12) 1 8131 (IC29)</td>
<td>3 74LS109 (IC10,13,16) 1 8836 or 8T380 (IC37)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 74LS00 (IC15,35)</td>
<td>1 74LS132 (IC18) 8 91L02 or 21L02 (IC41 through IC48)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 74LS02 (IC14) 1 74LS138 (IC11)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 74LS04 (IC19,36) 3 74LS157 (IC23,24,28) 1 93L16 (IC8)</td>
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<td></td>
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<table>
<thead>
<tr>
<th>RESISTORS</th>
<th>CAPACITORS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 75 ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 10 pfd, disc</td>
<td></td>
</tr>
<tr>
<td>2 200 ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 680 pfd, disc</td>
<td></td>
</tr>
<tr>
<td>2 330 ohm, (\frac{1}{2}) watt, 5%</td>
<td>3 .001 ufd, disc</td>
<td></td>
</tr>
<tr>
<td>1 330 ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 .001 ufd, mylar</td>
<td></td>
</tr>
<tr>
<td>1 680 ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 .01 ufd, mylar</td>
<td></td>
</tr>
<tr>
<td>5 8.2K ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 .1 ufd, mylar</td>
<td></td>
</tr>
<tr>
<td>3 39K ohm, (\frac{1}{2}) watt, 5%</td>
<td>31 .1 ufd, disc</td>
<td></td>
</tr>
<tr>
<td>2 50K ohm potentiometers</td>
<td>4 1 ufd, tantalum</td>
<td></td>
</tr>
<tr>
<td>1 100K ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 15 ufd, tantalum</td>
<td></td>
</tr>
<tr>
<td>31 1.5K ohm, (\frac{1}{2}) watt, 5%</td>
<td>1 100 ufd, 15V, electrolytic</td>
<td></td>
</tr>
<tr>
<td>2 3.3M ohm, (\frac{1}{2}) watt, 5%</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>MISCELLANEOUS</th>
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<tbody>
<tr>
<td>1 VDM-1 PC Board</td>
<td>1 Tie Wrap</td>
</tr>
<tr>
<td>1 Heat Sink</td>
<td>1 Length Spaghetti</td>
</tr>
<tr>
<td>48 DIP Sockets</td>
<td>3 6-32 Screws</td>
</tr>
<tr>
<td>1 DIP Switch, 6 or 7 position</td>
<td>3 6-32 Lockwashers</td>
</tr>
<tr>
<td>1 Length #24 Bare Wire</td>
<td>3 6-32 Nuts</td>
</tr>
<tr>
<td>9&quot; 8-conductor Ribbon Cable</td>
<td>1 Length Solder</td>
</tr>
<tr>
<td>1 Length 72-ohm Coaxial Cable</td>
<td>1 Manual</td>
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</table>
Figure 2-1. Identification of components.
<table>
<thead>
<tr>
<th>LOCATION</th>
<th>AREA</th>
<th>VALUE (OHMS)</th>
<th>COLOR CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ) R1*</td>
<td>A-1</td>
<td>75</td>
<td>violet-green-black</td>
</tr>
<tr>
<td>( ) R2*</td>
<td>A-1</td>
<td>330 ½ watt</td>
<td>orange-orange-brown</td>
</tr>
<tr>
<td>( ) R3*</td>
<td>A-2</td>
<td>200</td>
<td>red-black-brown</td>
</tr>
<tr>
<td>( ) R4**</td>
<td>A-3</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R5+</td>
<td>A-4</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R6</td>
<td>A-10</td>
<td>680 ½ watt</td>
<td>blue-grey-brown</td>
</tr>
<tr>
<td>( ) R7+</td>
<td>B-2</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R8</td>
<td>B-2</td>
<td>39 K</td>
<td>orange-white-orange</td>
</tr>
<tr>
<td>( ) R9</td>
<td>B-4</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R10</td>
<td>B-4</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R11</td>
<td>B-5.6</td>
<td>200</td>
<td>red-black-brown</td>
</tr>
<tr>
<td>( ) R12</td>
<td>B-10</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R13</td>
<td>C-3.4</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R14</td>
<td>C-4</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R15</td>
<td>C-6.7</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R16*</td>
<td>D-3</td>
<td>330</td>
<td>orange-orange-brown</td>
</tr>
<tr>
<td>( ) R17*</td>
<td>D-3</td>
<td>330</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R18</td>
<td>D-3.4</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R19+</td>
<td>D-4</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R20</td>
<td>D-6</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R21</td>
<td>E-1.2</td>
<td>3.3 M</td>
<td>orange-orange-green</td>
</tr>
<tr>
<td>( ) R22</td>
<td>E-1.2</td>
<td>8.2 K</td>
<td>grey-red-red</td>
</tr>
<tr>
<td>( ) R23</td>
<td>E-1.2</td>
<td>100 K</td>
<td>brown-black-yellow</td>
</tr>
<tr>
<td>( ) R24</td>
<td>E-3</td>
<td>3.3 M</td>
<td>orange-orange-green</td>
</tr>
<tr>
<td>( ) R25</td>
<td>E-4</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R26+</td>
<td>E-5</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R27-32#</td>
<td>E-7.8</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R33#</td>
<td>F-1</td>
<td>50 K</td>
<td>Potentiometer</td>
</tr>
<tr>
<td>( ) R34*</td>
<td>F-2</td>
<td>8.2 K</td>
<td>grey-red-red</td>
</tr>
<tr>
<td>( ) R35</td>
<td>F-2</td>
<td>8.2 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R36@</td>
<td>F-1.2</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R37</td>
<td>F-2</td>
<td>39 K</td>
<td>orange-white-orange</td>
</tr>
<tr>
<td>( ) R38</td>
<td>F-2.3</td>
<td>8.2 K</td>
<td>grey-red-red</td>
</tr>
<tr>
<td>( ) R39+</td>
<td>F-3</td>
<td>39 K</td>
<td>orange-white-orange</td>
</tr>
<tr>
<td>( ) R40+</td>
<td>F-5</td>
<td>1.5 K</td>
<td>brown-green-red</td>
</tr>
<tr>
<td>( ) R41-48@@</td>
<td>F-7</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R49</td>
<td>F-9</td>
<td>1.5 K</td>
<td>&quot;</td>
</tr>
<tr>
<td>( ) R50##</td>
<td>G-1</td>
<td>50 K</td>
<td>Potentiometer</td>
</tr>
<tr>
<td>( ) R51*</td>
<td>G-2</td>
<td>8.2 K</td>
<td>grey-red-red</td>
</tr>
</tbody>
</table>

**NOTE**

Unless noted otherwise, all resistors are ½ watt, 5%.

* Check for solder bridges to ground plane.

** Move R4 away from IC1 (Area A-2,3) toward IC2 (Area A-3,4) before soldering.

+ Be sure leads do not short traces beneath them.
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

SECTION II

# Leads at bottom of board (toward edge connector) must not short to one another.

## Install parallel to board with thumb wheels at top edge of board. Check for solder bridges to ground plane after installation.

@ Take care that R35 and R36 leads do not short.

@@ Check for solder bridges after installation.

( ) **Step 4.** Install all capacitors in numerical order. Insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

**NOTE**

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through the mounting holes, remove the capacitor and clear the holes of any wax. Reinsert and install.

Refer to footnotes at the end of this step before installing flagged (*, **, @, @@, # or ##) capacitors.

<table>
<thead>
<tr>
<th>LOCATION</th>
<th>AREA</th>
<th>VALUE (UFD)</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ) C1*</td>
<td>A-1,2</td>
<td>100</td>
<td>Electrolytic</td>
</tr>
<tr>
<td>( ) C2</td>
<td>A-2,3</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C3</td>
<td>A-2</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C4</td>
<td>A-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C5</td>
<td>A-7</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C6</td>
<td>A-8</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C7*</td>
<td>A-8</td>
<td>1</td>
<td>Tantalum, dipped</td>
</tr>
<tr>
<td>( ) C8*</td>
<td>A-9</td>
<td>1</td>
<td>Tantalum, dipped</td>
</tr>
<tr>
<td>( ) C9*</td>
<td>A-9,10</td>
<td>1</td>
<td>Tantalum, dipped</td>
</tr>
<tr>
<td>( ) C10</td>
<td>B-1</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C11</td>
<td>B-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C12</td>
<td>B-8</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C13</td>
<td>B-10</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C14</td>
<td>C-2</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C15</td>
<td>C-4</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C16</td>
<td>C-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C17</td>
<td>C-9</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C18</td>
<td>D-1</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C19</td>
<td>D-2</td>
<td>10</td>
<td>pfda</td>
</tr>
<tr>
<td>( ) C20</td>
<td>D-2</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C21*</td>
<td>D-3</td>
<td>.001</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C22*</td>
<td>D-4</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C23</td>
<td>D-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C24</td>
<td>D-9</td>
<td>.1</td>
<td>Disc</td>
</tr>
</tbody>
</table>

II-7
<table>
<thead>
<tr>
<th>LOCATION</th>
<th>AREA</th>
<th>VALUE</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ) C25@</td>
<td>E-1.2</td>
<td>.01</td>
<td>Mylar tubular</td>
</tr>
<tr>
<td>( ) C26</td>
<td>E-7</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C27#</td>
<td>F-2</td>
<td>.001</td>
<td>Mylar tubular</td>
</tr>
<tr>
<td>( ) C28##</td>
<td>F-2</td>
<td>.001</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C29##</td>
<td>F-3</td>
<td>680</td>
<td>pfd</td>
</tr>
<tr>
<td>( ) C30</td>
<td>F-3.4</td>
<td>.001</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C31</td>
<td>F-4</td>
<td>.1</td>
<td>Mylar tubular</td>
</tr>
<tr>
<td>( ) C32</td>
<td>F-6</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C33</td>
<td>F-9</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C34</td>
<td>G-2</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C35</td>
<td>G-4</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C36</td>
<td>G-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C37</td>
<td>G-9</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C38</td>
<td>G-10</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C39*, **</td>
<td>H-1</td>
<td>15</td>
<td>Tantalum, dipped</td>
</tr>
<tr>
<td>( ) C40</td>
<td>H-1</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C41*, **</td>
<td>H-2</td>
<td>1</td>
<td>Tantalum, dipped</td>
</tr>
<tr>
<td>( ) C42</td>
<td>J-5</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C43</td>
<td>J-7</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C44</td>
<td>J-8</td>
<td>.1</td>
<td>Disc</td>
</tr>
<tr>
<td>( ) C45</td>
<td>J-9</td>
<td>.1</td>
<td>Disc</td>
</tr>
</tbody>
</table>

* Take care to observe polarity.
** Check for solder bridges to ground plane.
@ Check that C22 lead doesn't short to R19 (Area D-4). Move R19 lead as required.
@@ Do not center C25 between mounting holes. Position it so the capacitor is closer to the top mounting hole and the resulting longer lead at the bottom end.
# Check that C27 lead doesn't short to R36 (Area F-1.2). Move R36 lead as required.
## Be careful not to interchange C28 and C29.

( ) **Step 5.** Install diode D1 (IN5225B) in Area A-10. Position D1 so that its band mark (cathode) is on the righthand side. Solder and trim leads.

( ) **Step 6.** Install diodes D2 and D3 (IN4148) in Area E-1.2. Position these diodes with the band mark (cathode) at top of board. Solder and trim leads.

( ) **Step 7.** Install heat sink in Area H,J-1,2,3,4. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the triangle of holes is under one of the triangular cut-outs in the sink. Using two 6-32 screws, nuts, and lockwashers, attach the heat sink to the board. Insert screws from back (solder) side of board. (See Figure 2-2.)

II-8
( ) **Step 8.** Install IC49 (340T-5.0V or 7805UC) in Area J-1,2,3. Position IC49 on heat sink and observe how the leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent downwards at a point approximately 0.2 inches further from the body than the other leads. Bend the leads so that no contact is made with the heat sink when IC49 is flat against the sink and its mounting hole is aligned with the hole in the sink. Fasten IC49 to sink using 6-32 screw, lockwasher and nut. Insert screw from back (solder) side of board. Solder and trim leads. (See Figure 2-2.)

![Figure 2-2. Heat sink and IC49 installation.](image)

( ) **Step 9.** Install IC50 in Area A-9. (See detail drawing on component location diagram.) Install IC50 with flat facing left. Bend center lead back to fit into mounting hole. Push straight down until the IC is stopped by its leads. Solder and trim leads.

( ) **Step 10.** Install crystal Y1 in Area D-1,2. (See detail drawing on component location diagram.)

( ) Install Y1 so that it lies flat against board as shown (case at top of board), solder leads and trim. Using a piece of excess crystal lead, ground the crystal case as indicated in the detail drawing. First solder on the back side of board. Then solder the lead to the crystal case. (See CAUTIONS on Page II-10.)

II-9
CAUTION 1

SOLDER QUICKLY SO THAT EXCESSIVE HEAT
WILL NOT BE APPLIED TO CRYSTAL.

CAUTION 2

THE CRYSTAL GROUND LEAD MUST NOT SHORT
TO TOP TRACE ON BACK (SOLDER) SIDE OF
BOARD. IF THIS SHORT DOES EXIST, THE
COMPUTER FUSE WILL BLOW.

( ) Step 11. Check that crystal Y1 ground is not shorted to top
trace on back (solder) side of board. Use an ohmmeter to
measure the resistance between the top trace on the back side
of the board and the crystal case. You should measure some
resistance. Zero resistance indicates a solder bridge. Cor-
rect the condition.

Proceed to Step 12 if you measure some top trace-to-crystal
case resistance.

( ) Step 12. Check regulator operation. This check is made to
prevent potential subsequent damage to the ICs from incorrect
voltages.

( ) Install VDM-1 in computer. (The use of a Processor Tech-
nology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD
WITH POWER ON. TO DO OTHERWISE CAN
DAMAGE THE BOARD.

( ) Turn power on and make the following voltage measurements:

<table>
<thead>
<tr>
<th>MEASUREMENT POINT</th>
<th>AREA</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 3 of IC50</td>
<td>A-8,9</td>
<td>12 vdc ± 5%</td>
</tr>
<tr>
<td>Anode of D1</td>
<td>A-10</td>
<td>-3 vdc ±10%</td>
</tr>
<tr>
<td>Pin 14 of IC1</td>
<td>A-2</td>
<td>5 vdc ± 5%</td>
</tr>
</tbody>
</table>

( ) If any voltages are incorrect, determine and correct the
cause before proceeding. Especially check for solder
shorts.

If voltages are correct, go on to Step 13.

( ) Step 13. Install jumper in Area D,E-9. Cover a piece of ex-
cess resistor lead with ¼" spaghetti, bend to fit holes,
insert, solder and trim.
Step 14. Install coaxial cable in Area A,B-1. (See Figure 2-3 for details on how to prepare cable.)

Strip away approximately 1/4" of the outer insulation to expose the shield. Unbraid shield, gather and twist into a single lead. Then strip away the inner conductor insulation, leaving about 1/4" at the shield end.

CAUTION

WHEN PREPARING AND INSTALLING SHIELD, BE SURE BITS OF BRAID DO NOT FALL ON-TO BOARD. SUCH DEBRIS CAN CREATE HARD-TO-FIND SHORT CIRCUITS.

Insert inner conductor in indicated mounting hole, solder and trim. Solder shield to ground plane and trim. Install tie wrap as shown.

CAUTION

AFTER INSTALLATION, FINE BITS OF THE BRAID FROM THE SHIELD MAY WORK LOOSE AND FALL ONTO THE BOARD AND CREATE HARD-TO-FIND SHORT CIRCUITS. TO PREVENT THIS, COAT ALL EXPOSED BRAID WITH AN ADHESIVE AFTER SOLDERING AND BEFORE TIEING. USE AN ADHESIVE SUCH AS SILICONE, CONTACT CEMENT OR FINGER- NAIL POLISH. DO NOT USE WATER BASE ADHESIVES.

Step 15. Install DIP Switch in Area B-1,2. Position it so Switch No. 1 is at left end of pad. As you will note, the DIP Switch pad is designed to accomodate a 7-position switch. If a 6-position (12 pin) switch is supplied, position it as far to the left as possible. (The two holes to the right will be unused in this case.) If a 7-position (14 pin) switch is supplied, remember that Switch No. 7 is not used.

NOTE

The function of the DIP switches is defined in Section III of this manual.

II-11
( ) Step 16. Install the following ICs in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

<table>
<thead>
<tr>
<th>IC NO.</th>
<th>AREA</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>A-2,3</td>
<td>7406</td>
</tr>
<tr>
<td>IC2</td>
<td>A-3,4</td>
<td>74LS163</td>
</tr>
<tr>
<td>IC7</td>
<td>B-3</td>
<td>74LS20</td>
</tr>
<tr>
<td>IC8</td>
<td>B-4,5</td>
<td>93L16</td>
</tr>
<tr>
<td>IC9</td>
<td>B-6,7</td>
<td>74LS10</td>
</tr>
<tr>
<td>IC14</td>
<td>C-4,5</td>
<td>74LS02</td>
</tr>
<tr>
<td>IC15</td>
<td>C-6</td>
<td>74LS00</td>
</tr>
<tr>
<td>IC16</td>
<td>C-7</td>
<td>74LS109</td>
</tr>
<tr>
<td>IC19</td>
<td>D-3,4</td>
<td>74LS04</td>
</tr>
<tr>
<td>IC20</td>
<td>D-5</td>
<td>74LS163</td>
</tr>
<tr>
<td>IC21</td>
<td>D-6</td>
<td>74LS163</td>
</tr>
<tr>
<td>IC22</td>
<td>D-7</td>
<td>74LS163</td>
</tr>
</tbody>
</table>

( ) Step 17. Check timing chain operation. If you do not have an oscilloscope, proceed to Step 18.

( ) Install VDM-1 in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON.

( ) Turn power on. Using an oscilloscope, check for the waveforms given in Figure 2-4 at the indicated observation points and in the order given. The waveforms shown in Figure 2-4 approximate actual waveforms. If any waveforms are incorrect, determine and correct the cause. Especially check for solder bridges and incorrectly installed ICs.

NOTE

Irregularities up to 1 volt are acceptable on positive portions of waveforms. Negative portions, however, should be relatively flat.

If all waveforms are correct, proceed to Step 18.

II-12
## PROCESSOR TECHNOLOGY CORPORATION
### VDM-1 VIDEO DISPLAY MODULE

<table>
<thead>
<tr>
<th>CHECK POINT</th>
<th>AREA</th>
<th>WAVEFORM</th>
</tr>
</thead>
<tbody>
<tr>
<td>( ) IC19, pin 3</td>
<td>D-3,4</td>
<td>13.5 MHz square wave. (This is not a perfect square wave. It in fact more resembles a poor sine wave.)</td>
</tr>
<tr>
<td>( ) IC19, pin 11</td>
<td>D-3,4</td>
<td>300 nsec 375 nsec</td>
</tr>
<tr>
<td>( ) IC19, pin 13</td>
<td>D-3,4</td>
<td>75 nsec 600 nsec</td>
</tr>
<tr>
<td>( ) IC22, pin 11</td>
<td>D-7</td>
<td>5 usec 5 usec</td>
</tr>
<tr>
<td>( ) IC21, pin 11</td>
<td>D-6</td>
<td>50 usec 12 usec</td>
</tr>
<tr>
<td>( ) IC2, pin 11</td>
<td>A-3,4</td>
<td>350 usec 520 usec</td>
</tr>
<tr>
<td>( ) IC8, pin 11</td>
<td>B-4,5</td>
<td>10 msec 6.7 msec</td>
</tr>
<tr>
<td>( ) IC16, pin 10</td>
<td>C-7</td>
<td>13.5 msec 3.3 msec</td>
</tr>
</tbody>
</table>

Figure 2-4. Timing Waveforms

II-13
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

SECTION II

( ) Step 18. Install the following ICs in the indicated locations. Observe the same general instructions given in Step 16.

<table>
<thead>
<tr>
<th>IC NO.</th>
<th>AREA</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC12</td>
<td>C-2</td>
<td>74LS86</td>
</tr>
<tr>
<td>IC25*</td>
<td>E-3</td>
<td>4049</td>
</tr>
<tr>
<td>IC30*</td>
<td>F-3</td>
<td>4001</td>
</tr>
</tbody>
</table>

*MOS devices. Refer to CAUTION on Page II-3.

( ) Step 19. Check synchronization circuits.

( ) Set DIP Switch as follows:

Switch No. 1: ON
All other switches: OFF

( ) Install VDM-1 in computer. Observe CAUTION given in Step 17. Then connect VDM-1 to video monitor.

( ) Set R33 (VERT) and R50 (HORIZ) on the VDM-1 to their mid-range settings. Turn computer and monitor on.

NOTE

In making this check, the Horizontal Hold Control on monitor may always be readjusted to center display.

( ) The display raster will be pulled in. Using the monitor vertical hold, you should be able to obtain a slow roll (black horizontal bar moves slowly down the screen) and a stationary raster. Using the monitor horizontal hold, you should be able to adjust for an out of sync raster (numerous black lines cutting across the raster) and a stable raster. If you do not observe these conditions, try adjusting R33 and R50 on the VDM-1. If you are still unable to obtain the indicated conditions, determine and correct the cause before proceeding.

NOTE

For a stable presentation, a few monitors--especially modified TV sets---may require a higher sync amplitude than that supplied by the VDM-1. In such cases, increase sync amplitude by reducing value of R2 (Area A-1). DO NOT DECREASE R2 BELOW 225 OHMS.
If the aforementioned vertical and horizontal conditions are realized, turn Switch No. 1 OFF and Switch No. 2 ON. The monitor screen should darken, and you should be able to obtain the previously described vertical and horizontal conditions. If operation is not as described after turning Switch No. 1 OFF and Switch No. 2 ON, determine and correct the cause.

If the synchronization circuits are operating correctly, proceed to Step 20.

Step 20. Install the following ICs in the indicated locations. Observe the same general instructions given in Step 16.

<table>
<thead>
<tr>
<th>IC NO.</th>
<th>AREA</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC3</td>
<td>A-4,5</td>
<td>74166</td>
</tr>
<tr>
<td>IC4*</td>
<td>A-6,7</td>
<td>MCM6575,6576 or 6574</td>
</tr>
<tr>
<td>IC5</td>
<td>A-8</td>
<td>74LS175</td>
</tr>
<tr>
<td>IC6</td>
<td>A-9</td>
<td>74LS175</td>
</tr>
<tr>
<td>IC17</td>
<td>C-8</td>
<td>74LS175</td>
</tr>
</tbody>
</table>

*MOS devices. Refer to CAUTION on Page II-3.

CAUTION 1

TO INSURE THAT IC4 WILL NOT BE DAMAGED BY STATIC DISCHARGE, GROUND YOURSELF TO COMPUTER CHASSIS, REMOVE IC4 FROM PACKAGE AND INSTALL ON VDM-1 BOARD.

CAUTION 2

IC4 IS A CERAMIC PACKAGE AND FRAGILE. USE AN EVENLY DISTRIBUTED, EASY PRESSURE WHEN LOADING IC4.

CAUTION 3

PIN 1 ON IC4 IS INDICATED BY A RAISED BUMP ON TOP OF THE IC. TAKE CARE TO LOAD IT CORRECTLY.

Step 21. Check video circuits and character generator (IC4).

Using wire jumpers and tack soldering technique, make the following TEMPORARY connections:

IC15 (Area C-6): Pin 2 to 7
IC17 (Area C-8): Pin 5 to 8
Pin 4 of IC7 (Area B-3) to pin 1 of IC8 (Area B-4,5)
( ) Set up DIP Switch as follows:

Switches No. 2 and 5: ON
All other switches: OFF

( ) Install VDM-1 in computer. Observe CAUTION in Step 17. Then connect VDM-1 to video monitor.

( ) Adjust R33 and R50, and monitor Horizontal Hold Control if required, to center pattern on screen. Check for 16 lines of 64 white dashes (actually ASCII underscores) on black background. (See Figure 2-4.)

( ) Set Switch No. 1 to ON and Switch No. 2 to OFF. Check for 16 lines of 64 black dashes (ASCII underscores) on white background. (See Figure 2-5.)

( ) Set Switch No. 3 to ON. Check for 16 lines of 64 black dashes (ASCII underscores) on white background surrounded by black frame. (See Figure 2-6 on Page II-18.)

( ) Set Switch No. 3 to OFF and Switch No. 4 to ON. Black frame in preceding presentation should disappear and entire display should blink.

( ) Set Switch No. 1 and No. 4 to OFF and Switch No. 2 and No. 3 to ON. Check for 16 lines of 64 white dashes (ASCII underscores) on black background surrounded by white frame. (See Figure 2-7 on Page II-18.)

( ) Set Switch No. 3 to OFF and Switch No. 4 to ON. White frame in preceding presentation should disappear and entire display should blink.

( ) If your VDM-1 fails to pass any of the preceding tests, DO NOT PROCEED BEYOND THIS STEP without determining and correcting the problem.

( ) If your VDM-1 passes all of the preceding tests, REMOVE TEMPORARY JUMPERS installed at beginning of this step and go on to Step 22.

( ) Step 22. Install remaining ICs in the indicated locations. Observe the same general instructions given in Step 16.

<table>
<thead>
<tr>
<th>IC NO.</th>
<th>AREA</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( )</td>
<td>IC10</td>
<td>B-7,8</td>
</tr>
<tr>
<td>( )</td>
<td>IC11</td>
<td>B-9</td>
</tr>
<tr>
<td>( )</td>
<td>IC13</td>
<td>C-3</td>
</tr>
<tr>
<td>( )</td>
<td>IC18</td>
<td>C-9,10</td>
</tr>
<tr>
<td>( )</td>
<td>IC23 &amp; 24</td>
<td>D-8,9,10</td>
</tr>
</tbody>
</table>

74LS109
74LS138
74LS109
74LS132
74LS157

II-16
Figure 2-4. Video circuit check: SW2 & 5 ON, SW1,3,4 & 6 OFF.

Figure 2-5. Video circuit check: SW1 ON, SW2 OFF.
Figure 2-6. Video circuit check: SW1 & 3 ON, SW2 OFF.

Figure 2-7. Video circuit check: SW1 & 4 OFF, SW2 & 3 ON.
VDM-1 VIDEO DISPLAY MODULE

SECTION II

<table>
<thead>
<tr>
<th>IC NO.</th>
<th>AREA</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC26 &amp; 27*</td>
<td>E-4,5</td>
<td>4029</td>
</tr>
<tr>
<td>IC28</td>
<td>E-6</td>
<td>74L8157</td>
</tr>
<tr>
<td>IC29</td>
<td>E-9</td>
<td>8131</td>
</tr>
<tr>
<td>IC31 &amp; 32*</td>
<td>F-4,5,6</td>
<td>4042</td>
</tr>
<tr>
<td>IC33 &amp; 34</td>
<td>F-8,9,10</td>
<td>74L808</td>
</tr>
<tr>
<td>IC35</td>
<td>G-3</td>
<td>74L800</td>
</tr>
<tr>
<td>IC36</td>
<td>G-4,5</td>
<td>74L804</td>
</tr>
<tr>
<td>IC37</td>
<td>G-5,6</td>
<td>8836 or 87380</td>
</tr>
<tr>
<td>IC38 &amp; 39</td>
<td>G-8,9,10</td>
<td>8097 or 8797</td>
</tr>
<tr>
<td>IC40</td>
<td>H-1,2,3</td>
<td>74L810</td>
</tr>
<tr>
<td>IC41 thru 48*</td>
<td>H,J-5,6,7,8,9</td>
<td>91L02 or 21L02</td>
</tr>
</tbody>
</table>

*MOS device. Refer to CAUTION on Page II-3.

( ) Step 23. Set VDM-1 address. The Software included with the VDM-1, as well as future releases, requires setting the VDM memory address to CCØØ (hex) and the I/O control port to C8 (hex). To connect the VDM for these "standard" address assignments, wire jumpers as shown in Figure 2-8.

![Diagram of VDM-1 Address Jumpers](image)

Figure 2-8. VDM-1 address jumpers, "standard" address assignments.

Should you wish to set your VDM-1 for other than the "standard" address assignments, proceed as follows: (Refer to Figure 2-9.)

( ) 1. Write down port address in binary form (ADRØ-7), ADRØ and 1 must always be zero.

( ) 2. Write down six-bit memory page address in binary form (ADRØ-15) directly below port address. Place bit 15 below bit 7, bit 14 below bit 6 and so forth.

( ) 3. Connect address selection jumpers in Area E-8,9 according to the following rules:

   a. If both bits in a column (bits 6 and 14, for example) are "1", no jumper is installed.

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b. If both bits in a column (bits 4 and 12, for example) are "0", install a jumper between the corresponding output of IC29 and ground (GND).

c. If the port and memory page address bits in a column are "1" and "0" respectively (bits 7 and 15, for example), install a jumper between the corresponding output of IC29 and the Y row.

d. If the port and memory address bits in a column are "0" and "1" respectively (bits 5 and 13, for example), install a jumper between the corresponding output of IC29 and the X row.

Figure 2-9 illustrates the preceding procedure assuming a port address of C4 (hex) and a memory page address of 6400 (hex).

ADR BIT NO.       7 6 5 4 3 2 1 0
(1) PORT ADDRESS (C4 Hex)   1 1 0 0 0 0 0 0
(2) MEMORY PAGE ADDRESS (6400 Hex)       0 1 0 0 0 0 0 0
ADR BIT NO.       1 5 1 4 1 3 1 2 1 1 0

(3) ADDRESS SELECTION JUMPERS

ADR 15
0 0 0 0 0 0 0 0 Y
0 0 0 0 0 0 0 X
0 0 0 0 0 0 0 GND

Area E-8,9  IC29

Figure 2-9. Procedure for setting VDM-1 for other than "standard" address assignments.

( ) Step 24. Install ready jumper (J2) in Area C-10.

( ) If your Altair has been modified so that the ready driver on the display board is connected to Bus Pin 3, install a jumper between J2 and PRDY.

( ) If this modification has not been made, jumper J2 to XRDY.

II-20
( ) Step 25. Install 9-inch length of 8-conductor ribbon cable on front (component) side of board between J1 in Area A-10 and J1 in Area J,H-10.

( ) To insure correct terminal-to-terminal interconnection, make a fold midway between the cable ends to form an inverted V. Figure 2-10 clearly illustrates this technique.

![Diagram of cable installation](image)

Figure 2-10. 8-conductor ribbon cable installation.

2.7 FINAL TEST PROCEDURES

2.7.1 VDM-1 DIP Switch Settings

( ) Set Switches 2, 3, 5 and 6 to ON.

( ) Set Switches 1 and 4 to OFF.

NOTE

With above settings, the VDM-1 is configured for normal video display (white on black background), non-blinking cursor, and unblanked control characters.

2.7.2 VDM-1 Installation

( ) Install VDM-1 in computer and connect VDM-1 to video monitor. Turn monitor on. Hold STOP Switch on and turn computer on. (This keeps computer from coming on in run mode and insures a random display for scroll test.

CAUTION

NEVER INSTALL OR REMOVE VDM-1 WITH COMPUTER POWER ON.

II-21
2.7.3 VDM-1 Status Initialization

( ) Enter following program into computer memory beginning at address zero.

<table>
<thead>
<tr>
<th>HEX ADDRESS</th>
<th>OP CODE</th>
<th>LINE NO.</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>3E 00</td>
<td>0005</td>
<td>MVI A, $0H</td>
</tr>
<tr>
<td>0002</td>
<td>D1 08</td>
<td>0010</td>
<td>OUT CSH</td>
</tr>
<tr>
<td>0004</td>
<td>C3 00 00</td>
<td>0015</td>
<td>JMP $0</td>
</tr>
</tbody>
</table>

( ) Execute this program by turning on the RUN Switch and then flipping it quickly back to STOP. This program initializes the VDM-1 to display all sixteen lines.

2.7.4 Scroll and Status Change Test

The purpose of this test is twofold: 1) it checks scrolling operation, and 2) it allows you to become familiar with the operation of the VDM-1 status control port.

( ) Change first two bytes of program in Paragraph 2.7.3 to DB and FF hexadecimal. Also set the eight Sense Switches on your Altair or IMSAI front panel to OFF (zero). The program, if run continuously, will now output the Sense Switch data to the VDM-1 status control port.

( ) With all eight Sense Switches OFF, a full 16 line by 64 character display (1024 characters) should appear on the screen. Note contents of first line in display. Call this line A.

( ) As shown in Figure 2-11, Sense Switches $ through 3 define the first display line in memory. Set Sense Switch $ to ON (one). First line (A) in preceding display should shift to bottom of screen and the others should move up one line. Try various combinations of Sense Switches $ through 3 and note where first line (A) appears in display. Once you are familiar with how Sense Switches $ through 3 affect the display, set them to OFF.

( ) As shown in Figure 2-11, Sense Switches 4 through 7 determine the first displayed screen position. Set these four switches to ON. Only the bottom line on the screen

II-22
should be displayed. Try various combinations of Sense Switches 4 through 7. As each switch is changed, the display should appear to move up and down the screen with a black area above it. The first line on display, regardless of its vertical position on the screen, should remain the same.

( ) After becoming familiar with how Sense Switches 4 through 7 affect the display, try different combinations of all the Sense Switches. Do this until you are familiar with the various ways in which "scrolling" can be performed.

<table>
<thead>
<tr>
<th>VDM-1 Status Port Bit Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR BIT NO.</td>
</tr>
<tr>
<td>First Displayed Screen Position</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VDM-1 Address Allocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR BIT NO.</td>
</tr>
<tr>
<td>VDM-1 Card Address (C8 Hex &quot;Standard&quot;)</td>
</tr>
<tr>
<td>Display Line Address</td>
</tr>
</tbody>
</table>

NOTE: Character addresses always correspond to actual screen display position. Depending on status port control word, the line address may or may not correspond to the screen position.

Figure 2-11. VDM-1 status port bit functions and address allocation.

2.7.5 Hardware-Software Function Test

This test checks all VDM-1 hardware-software functions.

( ) Enter following program into computer memory beginning at address zero.
### VDM-1 VIDEO DISPLAY MODULE

#### SECTION II

<table>
<thead>
<tr>
<th>HEX ADDRESS</th>
<th>OP CODE</th>
<th>LINE NO.</th>
<th>MNEMONIC</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>3E 00</td>
<td>0010</td>
<td>MVI A,$0</td>
<td>INIT. SCREEN TO SHOW ALL 1024 CHARACTERS</td>
</tr>
<tr>
<td>0002</td>
<td>D3 C8</td>
<td>0020</td>
<td>OUT $C8H</td>
<td></td>
</tr>
<tr>
<td>0004</td>
<td>21 00</td>
<td>0030</td>
<td>LXI H,$CC0H</td>
<td>INIT. SCREEN POINTER</td>
</tr>
<tr>
<td>0007</td>
<td>06 00</td>
<td>0040</td>
<td>MVI B,$0</td>
<td></td>
</tr>
<tr>
<td>0009</td>
<td>05</td>
<td>0050</td>
<td>LOOP DCR B</td>
<td>COUNT DOWN</td>
</tr>
<tr>
<td>000A</td>
<td>70</td>
<td>0060</td>
<td>MOV M,B</td>
<td>PUT (B) ON SCREEN</td>
</tr>
<tr>
<td>000B</td>
<td>23</td>
<td>0070</td>
<td>INX H</td>
<td>INCREMENT SCREEN POINTER</td>
</tr>
<tr>
<td>000C</td>
<td>7C</td>
<td>0080</td>
<td>MOV A,H</td>
<td>END OF SCREEN</td>
</tr>
<tr>
<td>000D</td>
<td>FE 00</td>
<td>0090</td>
<td>CPI $D0H</td>
<td>COMPARE POINTER WITH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>END OF SCREEN</td>
</tr>
<tr>
<td>000F</td>
<td>C2 09</td>
<td>0100</td>
<td>JNZ LOOP</td>
<td></td>
</tr>
<tr>
<td>0012</td>
<td>3E 20</td>
<td>0110</td>
<td>MVI A,$20H</td>
<td>PUT &quot;SPACE&quot; IN (A)</td>
</tr>
<tr>
<td>0014</td>
<td>32 00</td>
<td>0120</td>
<td>STA $CC0H</td>
<td>MOVE (A) TO SCREEN</td>
</tr>
<tr>
<td>0017</td>
<td>32 74</td>
<td>0130</td>
<td>STA $CC74H</td>
<td>MOVE (A) TO SCREEN</td>
</tr>
<tr>
<td>001A</td>
<td>32 F2</td>
<td>0140</td>
<td>STA $CCF2H</td>
<td>MOVE (A) TO SCREEN</td>
</tr>
<tr>
<td>001D</td>
<td>76</td>
<td>0150</td>
<td>HLT</td>
<td>WE'RE DONE!</td>
</tr>
</tbody>
</table>

( ) Set all eight Sense Switches on your Altair or IMSAI to OFF (zero) and turn RUN Switch on. The display shown in Figure 2-12 should appear on the screen. Three character positions in this display are blanked to provide reference points. They are as follows:

![Figure 2-12. VDM-1 hardware-software test pattern (6574 character generator).](image-url)

II-24
1. The first character in the first display line is blanked to identify the first line in the display.

2. The VT control character (character position 53) in the second display line is blanked to permit a CR blanking test.

3. The CR control character (character position 51) in the fourth display line is blanked to permit a VT blanking test.

( ) Set DIP Switches 1 to ON and 2 to OFF. You should have the same display as shown in Figure 2-12.

( ) Set DIP Switch 2 on VDM-1 to OFF and Switch 1 to ON in that order. A reversed video equivalent of the display shown in Figure 2-12 should appear on the screen. That is, the first two display lines will be white on black, the third and fourth lines will be black on white, etc.

NOTE
DIP Switches 1 and 2 should never be on at the same time.

( ) Return DIP Switch 1 to OFF and Switch 2 to ON in that order.

( ) Set DIP Switch 3 to OFF and Switch 4 to ON in that order. The entire display shown in Figure 2-12 should blink.

NOTE
DIP Switches 3 and 4 should never be on at the same time.

( ) Return DIP Switch 4 to OFF and Switch 3 to ON in that order.

( ) Set DIP Switch 5 to OFF. The VDM-1 is now configured to to blank all control characters. Text blanking from CR to end of line and VT to end of screen is also enabled. The display shown in Figure 2-13 should appear on the screen.

As can be seen, the control characters (character positions 33 through 51) in the second display line are blanked out. Text blanking from, but not including, the CR control character (character position 51) to the end of line accounts for the remaining blanked portion of the line. VT blanking begins with the 54th character position in the fourth display line and blanks out the remainder of the screen.
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VDM-1 VIDEO DISPLAY MODULE

SECTION II

( ) Return DIP Switch 5 to ON and set Switch 6 to OFF. The VDM-1 is now configured to display control characters. Text blanking from CR to end of line and VT to end of screen is also enabled. The display shown in Figure 2-14 should appear on the screen.

As can be seen, the second line is blanked from, but not including, the CR control character to the end of the line. The CR control character as well as the other control characters preceding it are displayed. Again, VT blanking acts on the last 11 character positions in the fourth line as well as on all the following lines. The VT control character and the control characters preceding it in the fourth line are displayed.

( ) Return DIP Switch 6 to ON.

( ) At this point, if desired, you can put the VDM-1 through its scrolling paces by using the Sense Switches.

2.7.6 Character Generator Test

This test is provided for two purposes: 1) it allows you to check the character generator in the VDM-1 by displaying each character individually, and 2) it gives you an opportunity to become familiar with the ASCII code.

( ) Set DIP Switches on VDM-1 as follows:

Switch No. 1 and 4: OFF
All other switches: ON

( ) Enter following program into computer memory beginning at address zero.

<table>
<thead>
<tr>
<th>HEX ADDRESS</th>
<th>OP CODE</th>
<th>LINE NO</th>
<th>MNEMONIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>3E 00</td>
<td>0000</td>
<td>0010</td>
<td>MVI A, 0</td>
</tr>
<tr>
<td>D3 C8</td>
<td>0020</td>
<td>0030</td>
<td>OUT $CH</td>
</tr>
<tr>
<td>DB FF</td>
<td>0044</td>
<td>0050</td>
<td>IN $FFH</td>
</tr>
<tr>
<td>47 00</td>
<td>0060</td>
<td>0070</td>
<td>LXI H,$CH</td>
</tr>
<tr>
<td>3E 00</td>
<td>0080</td>
<td>0090</td>
<td>MVI A,$CH</td>
</tr>
<tr>
<td>21 00 CC</td>
<td>00A0</td>
<td>00B0</td>
<td>LXI H,$CH</td>
</tr>
<tr>
<td>70 00</td>
<td>00C0</td>
<td>00D0</td>
<td>MOV M,B</td>
</tr>
<tr>
<td>23 00</td>
<td>00E0</td>
<td>00F0</td>
<td>INX H</td>
</tr>
<tr>
<td>BC 00</td>
<td>0100</td>
<td></td>
<td>CMP H</td>
</tr>
</tbody>
</table>

(Program continued on Page II-28.)

II-26
Figure 2-13. Control character and text (VT-CR) blanking (6574 character generator).

Figure 2-14. Text (VT-CR) blanking (6574 character generator).

II-27
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VDM-1 VIDEO DISPLAY MODULE

SECTION II

<table>
<thead>
<tr>
<th>HEX ADDRESS</th>
<th>OP CODE</th>
<th>LINE NO.</th>
<th>MNEMONIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>000F</td>
<td>C2 0C</td>
<td>0100</td>
<td>JNZ MOVE</td>
</tr>
<tr>
<td>0012</td>
<td>DB FF</td>
<td>0110</td>
<td>INPUT IN $FFH *INPUT SENSE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SWITCHES</td>
</tr>
<tr>
<td>0014</td>
<td>B8</td>
<td>0120</td>
<td>CMP B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>*COMPARE TO B</td>
</tr>
<tr>
<td>0015</td>
<td>CA 12</td>
<td>0130</td>
<td>JZ INPUT</td>
</tr>
<tr>
<td>0018</td>
<td>C3 06</td>
<td>0140</td>
<td>JMP REDO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>*LOOP</td>
</tr>
</tbody>
</table>

( ) Turn RUN Switch on. The first seven Sense Switches (Ø through 6) on your Altair or IMSAI may now be used to address each character in the VDM-1 character generator, for their setting is the binary representation of the addressed ASCII character.

**NOTE**

The position of the eighth Sense Switch (7) determines whether the cursor is on or off.

( ) Using Sense Switches Ø through 6, individually address each of the 128 ASCII characters. (Refer to Figures 3-1A, B and C in Section III for ASCII code.)

For example, setting Sense Switches Ø and 6 to "1" and Sense Switches 1 through 5 to "Q" will address the character "A" (ASCII code 10000001). A full screen (16 lines by 64 characters) of A's should appear on the screen.

Setting Sense Switches Ø, 2, 4 and 5 to "1" and Sense Switches 1, 3 and 6 to "Q" will cause a 5 (ASCII code 01110101) to be displayed.

II-28
SECTION III

THEORY OF OPERATION

VDM-1 VIDEO DISPLAY MODULE
3.1 THEORY OF OPERATION

The VDM-1 can be broken down into eight functional sections: timing, synchronization and blanking, memory, character generation, cursor, video, scroll and computer interface. For the following discussions, refer to the VDM-1 schematic diagram in Section IV.

3.1.1 Timing

Two inverter gates (IC19)--connected as a high-gain non-inverting amplifier--and crystal Y1 form a crystal-controlled 13.5 MHz DOT CLOCK. This frequency defines the period of one dot in a character display matrix. DOT CLOCK is applied to a binary counter (IC20) which is preset to count seven to divide DOT CLOCK by nine. Two 1.5 MHz outputs are supplied by IC20: LOAD CLOCK and CHARACTER CLOCK. The former is a low-active signal of one DOT CLOCK duration; the latter is a square wave that is high and low for four and five DOT CLOCK periods respectively. Both the LOAD and CHARACTER CLOCK low-to-high transitions occur synchronously to the same DOT CLOCK transition.

CHARACTER CLOCK, which defines the period for one character, is counted down in IC22 and 21, both of which are 4-bit binary counters. IC22 counts from 0 to 15 and provides a carry output to enable IC21. IC21 is preset to count 3 and reset at count 9 by the output of NAND gate IC15. Thus IC21 cycles through six counts, with each count representing 16 CHARACTER CLOCK pulses.

Reset of IC21 defines the lefthand margin of the display, counts 4 through 7 define successive groups of 16 character positions, count 8 defines the righthand display margin, and count 9 defines the first CHARACTER CLOCK in the lefthand margin of the display.

The outputs of IC22 provide the four lower address bits of the character position on display. The two least significant outputs from IC21 supply the two high order address bits. Qn (pin 11) and Qn (pin 12) of IC21 are SCAN ADVANCE and HDISP (horizontal display) respectively. The former is used to generate horizontal synchronization signals, and the latter defines the start of a horizontal scan line.

On count 9 of IC21, the output of NAND gate IC15 also enables IC2, the scan divider. IC2 counts the horizontal scan lines that make up a row of characters and supplies the line number to the character generator ROM, IC4. IC2 is preset to count 15 for the first scan line in the row. With this line count, the character generator provides a blank spacer line between the preceding and current character rows. IC2 then counts from 0 to 11 lines. At the end of the 11th count, a decoder comprised of IC14 and 7 supplies a load pulse to IC2 which resets it to count 15.
This load pulse, after inversion, becomes the OVERFLOW LINE signal. OVERFLOW LINE enables the character row divider, IC8. IC8 resets itself with its carry output through IC9, with the reset count being determined by the state of IC16, the vertical display (VDISP) flip-flop. If IC16 is cleared, IC8 is reset to count 0; if IC16 is set, IC8 is reset to count 12. Thus IC8 counts four or 16 character rows when IC16 is set or cleared respectively during load. The total of 20 character rows (260 scan lines) represents a full field on the display raster.

3.1.2 Synchronization and Blanking

Horizontal and vertical synchronization signals are generated by two one-shot multivibrators consisting of three two-input NOR gates in IC30 and two inverters in IC25. Horizontal sync is triggered by SCAN ADVANCE and vertical sync by VDISP. Both circuits generate fixed-length sync pulses with adjustable starting times. C27 and C25 determine the length of the horizontal and vertical sync pulses respectively. The starting times with respect to triggering, are variable with R50 (HORIZ) and R33 (VERT) to provide continuous adjustment of the display position on the raster. An exclusive OR-gate in IC12 combines the two sync pulses into a composite sync (COMP SYNC) signal. Note that the use of the exclusive OR inverts the horizontal sync pulses when the vertical sync pulse appears. Since vertical sync information is extracted in the monitor by an integrating, or averaging, process, this technique maintains horizontal synchronization during the vertical sync period.

Two types of blanking are available in the VDM-1: control character blanking and video blanking. The former blanks control characters and causes cursor information to be displayed in their place. Video blanking forces portions of the video display to a white or black level, depending on whether normal or reverse video is selected with SW1 and SW2. (See Paragraph 3.2.)

Control character blanking, switch selectable with SW5 and SW6, is accomplished with one gate in IC14 and one gate in IC15. When a control character is present in the data latch (IC5 and 6), IC14 is satisfied. Assuming the blanking option is selected, the output of IC14 is gated with LOAD CLOCK in IC15 to clear the video parallel-to-serial converter, IC3. IC3 then loads all zeros instead of the character.

Video blanking is initiated by the PRE BLANK, POST BLANK, or BLANK inputs to IC7, a four-input NAND gate. The fourth input, the video output of the cursor circuit, is blanked when any of the three blanking inputs is active.

The PRE BLANK input provides "window shade" blanking which is analogous to pulling a window shade down from the top of the display. PRE BLANK is generated in one half of IC13. IC13 is reset active during V SYNC and set inactive during START DISPLAY. The
latter is generated by the scrolling circuitry and defines the character row for which the window shade ends. START DISPLAY may begin with any character row from zero through 14.

POST BLANK blanks all character rows following the row in which a VT control character appears if the CR/VT option is selected by SW5 or SW6 (see Paragraph 3.2). POST BLANK is generated in one flip-flop in IC16. This flip-flop is set inactive during V SYNC and reset active during OVERFLOW LINE if the VT flip-flop is set to indicate a VT control character.

The remaining video blanking function concerns the BLANK output from one section of IC17. This signal is a composite of HDISP, VDISP and the two control characters VT and CR. Since the blanking effects of these signals are character-position critical, timing is also critical. Thus, two D-type flip-flops in IC17 are used to insure synchronization.

The first flip-flop is active (low) only when HDISP and VDISP are high at IC15. Thus, the output of this flip-flop is active during the time a displayable character is latched into the data latch (IC5 and 6). The output of the first flip-flop is applied to one input of a three-input gate in IC9. IC9 is active (low) only when all of its inputs are high. A low input to IC9 will therefore override any other high inputs.

Outputs from the VT and CR flip-flops (IC10) are the other two inputs to IC9. VT and CR are active (low) from the first LOAD CLOCK during which either character is present in the data latch. This assumes the CR/VT option is enabled. Both the VT and CR flip-flops are set inactive during SCAN ENABLE. Thus, the blanking effect of VT and CR lasts from the character following VT or CR to the end of the character row.

The VT and CR blanking signals are generated by IC11, IC10, IC16 and their associated circuitry. In order to enable an output from IC11, the inputs to pins 6, 4 and 5 must be active. If pin 6 is grounded with SW5 and 6, the output of IC14 is disabled to deselect the VT/CR option. Otherwise pin 6 will be active (high) when IC14 decodes a control character in the output of the data latch (bits 5 and 6 are zero). Pin 4 is active (low) when IC9 decodes a control character (bit 3 zero and bit 4 high) when PRE BLANK is inactive (high). Pin 5 is active when DISPLAY is active (low). DISPLAY is low during all video display times. With IC11 enabled, it supplies outputs when the three low-order bits from the data latch reflect the VT or CR ASCII code, 0001011 and 0001101 respectively.

The CR output of IC11 (Pin 10) resets the CR flip-flop (IC10) active at the end of the CR control character. VT flip-flop (IC10) is likewise set active by the VT output of IC11 (pin 12). Both sections in IC10 are set inactive by LOAD CLOCK during SCAN ENABLE.
CR and VT blanking are consequently effective from the start of the character position following the control character to the end of the character row. When the VT flip-flop is set inactive at the end of the last scan line in the row, the POST BLANK flip-flop (IC16) is also reset active since OVERFLOW LINE becomes active. Thus, VT initiated blanking continues to the end of the screen.

3.1.3 Screen Memory

Screen memory in the VDM-1 consists of eight 1 x 1024 bit RAM (random access memory) chips, IC41 through IC48. All chips are held enabled. Memory addressing is provided through a two-to-one multiplexer (IC23, 24 and 28) which selects one of two address sources: external address from the computer or internal character address from IC21, 22, 26 and 27. The last two ICs make up the scrolling counter. Normally the internal address is multiplexed to memory. When the computer requests access, the multiplexer switches to the external address lines, ADR# through 9. The write enable (WE) input to IC41 through 48 are active only during external addressing when WRITE at pin 8 of IC18 is low.

3.1.4 Character Generation

Two latches, IC5 and 6, latch data from the screen memory. The output from IC46 is inverted before being applied to pin 12 of IC5, and the complement (pin 11) of the Q, output is used in addressing the character generator ROM, IC4. This enables the data latch to present a SPACE code to the ROM when it is cleared. Bit 8 from the latch is used for the cursor and does not enter the ROM.

IC4 has seven character address inputs, four row select inputs and seven data outputs. It is programmed to generate seven bits (dots) of character information for the selected scan line of the character row. The complete pattern of IC4 is shown in Figure 3-1A, B and C.

The ROM output is converted from parallel to serial form in IC3, a shift register, and applied to one gate in IC12. This gate is the first component in the video circuitry.

3.1.5 Cursor Circuit

A blink oscillator (two inverter sections in IC25), a latch (one section in IC17) and their associated components comprise the cursor circuit. The blink oscillator runs continuously at a rate set by R21 and C20. Its output has a nominal 0.5 sec period. If the blink option is selected with SW4 (see Paragraph 3.2), the blink signal is applied to one input of a gate in IC14. The other input to this gate is provided by the cursor latch, one section in IC17. If bit 7 out of the data latch is high, IC17 sets for the time the ROM is active on the character and remains set during the period when video data is shifted out of IC3. The output of IC17
is gated high through IC14 when BLINK is low. (BLINK is held low when the blink option is not selected.) The output of IC14 is in turn gated with the video output of IC3 in IC12, an exclusive OR gate. IC12 thus inverts the video if the output of IC14 is high, and no inversion takes place if the output of IC14 is low.

3.1.6 Video Circuit

The video signal, including the cursor, is gated to SW1 and 2 by IC7 in the absence of any blanking signals at the other three inputs to IC7. With SW2 closed, video and COMP SYNC are applied through two inverters in IC1 to a resistive mixer, R1 through R3. This mixer has a 75-ohm output impedance. The two signals are mixed to meet EIA composite video signal requirements and coupled to the output by C1. If only SW1 is closed, another inverter in IC1 inverts the video signal to produce a reverse (black on white) display.
Figure 3-1B. MCM6575 pattern.

3.1.7 Scroll Circuit

The scroll circuit is made up of IC26, 27, 31 and 32 and their associated circuitry. IC26 and 27 are up/down counters that are preset by the outputs of latches IC31 and 32. IC31 and 32 latch the character row information specified on DIS through 7. IC26 is preset during VDISP, the time from the bottom of the displayed text to the top of the next vertical display period. IC26 is held at the preset number during this period, and counting is disabled by OVERFLOW LINE. When the character row divider (IC8) advances at the end of the first character row in the display, IC26 is enabled to count down. IC26 provides a low on its TC output whenever the counter is at count zero. This TC active output is inverted in IC19 to supply the START DISPLAY signal (active high). PRE BLANK blanks the display until START DISPLAY goes active. START DISPLAY goes inactive when IC26 counts below zero during OVERFLOW LINE at the end of the character row.

During the active time of START DISPLAY, IC27 is loaded with the contents of IC32. IC27 is enabled, when OVERFLOW LINE is low, to count up from the start of the end of the first displayed character row. IC27 continues to count with the end of each following character row.
Figure 3-1C. MCM6576 pattern.

Since IC27 reloads to its preset value at the line for which the window shade ends, the display may be scrolled up or down by incrementing or decrementing the row number. Incrementing or decrementing the number in IC32 varies the window shade duration. Doing the same thing to the number in IC31, in the absence of window shade blanking, causes the display to scroll.

3.1.8 Computer Interface

IC29 compares the address bits, ADR16 through ADR15 with two possible binary comparison numbers. These numbers are set with the X, Y and GND (ground) jumper arrangement (ADDRESS SELECT). One comparison number, which relates to the page number to which the screen memory responds, is generated when there is no input on SIMP or SOUT. The other is generated when either of these inputs is present and represents the six high-order bits of the I/O port address to which the status port responds. Note that the circuit requires that the two low-order bits of the I/O port address always be zero.

During PSYNC, when $ \emptyset $ is low, IC29 compares its inputs and the two comparison numbers. An internal latch in IC29 retains the
state of the comparison when its enable input goes high. The output from IC29 drives several circuits.

1. It enables the XRDY driver, IC38.

2. It enables a section in IC37 (low) and IC40 (high).

If S1NP and SOUT are low, the other input to IC37 satisfies the gate to generate MEM SELECT (memory select). Should either be high and the two low-order I/O address bits (ADR8 and 9) are low, IC40 generates I/O SELECT.

An active I/O SELECT enables another gate in IC37 and a gate in IC35 to respond to PWR and PDRBIN respectively. PWR supplies LOAD STATUS to IC31 and 32. These two latches will thus retain the state of the DO bus as the scrolling parameters. PDRBIN generates STATUS OUT to enable IC39 (pin 15) to place the status bit on D10.

MEM SELECT performs three functions: 1) it immediately switches the address multiplexer (IC23, 24 and 28) to supply external addressing to the screen memory, 2) it enables one section of IC13, and 3) it enables one section in IC17.

The input to, and Q output of, IC13 are gated during the time preceding the next Ø2 high-to-low transition to IC38, the XRDY driver. Transmission through IC38 causes a wait state in the computer. This wait period allows the screen memory addresses to settle and allows adequate time for the memory to come ready for data input or output.

A MEM GO (memory go) signal from IC13, which occurs with the second Ø2 in the instruction cycle, indicates enough time has elapsed since addressing for the screen memory to transfer data. During the wait period, PDRBIN or MWRITE hold in their active state (high). Hence, either WRITE is given to the screen memory or DATA OUT enables the DI bus drivers as appropriate.

The output of IC17 prevents any possible interference with the display when the screen memory address is changed. When the address is changed, the display is overridden, and spurious data at the memory outputs can interfere with the display. When IC17 is set, it causes the data latch to reset to a SPACE code. The SPACE code remains until the next character clock following removal of MEM SELECT. As a result, a short (but not critical) line segment in the display is lost.

LOAD STATUS from IC37 also triggers a one-shot timer consisting of one section in IC30, one in IC25, and Q1. The buffered output of this one-shot is STATUS. STATUS goes high when the one-shot is triggered and remains high for 0.25 to 0.5 second. The computer, when performing an output instruction from the VDM-1 port,
can thus test the timer status by looking for a high on DI9. This allows a slow scroll rate without requiring complex timing routines in the CPU.

STATUS is also connected to an unused 7406 inverter section in IC1. The output of this inverter can be jumpered to any of the vector interrupt (VI) pins. In future systems with vectored interrupt, this output will eliminate the need to continuously test the timer status.

3.2 SWITCH SELECTABLE OPTIONS

The VDM-1 has several switch-selectable operating features. These are: normal and reverse video display, blinking and non-blinking cursor, text blanking, and control character blanking. These options are selected by SW1 through SW6 in the DIP Switch located in Area B-1,2 on the circuit board.

SW1 and 2 control the video display, SW3 and 4 control cursor, and SW5 and 6 control the text and control character blanking features. The role that each switch serves in configuring the VDM-1 circuitry for the various options can be readily determined by reviewing the schematic diagram in Section IV of this manual. Table 3-1 defines the options that are available with SW1 through 6. (Table 3-1 will be found on Page III-10.)
Table 3-1. DIP Switch States vs Options.

<table>
<thead>
<tr>
<th>SWITCHES</th>
<th>OPTION</th>
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<tr>
<td>No.</td>
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<td>---------</td>
<td>-------</td>
</tr>
<tr>
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<tr>
<td>5</td>
<td>ON</td>
</tr>
<tr>
<td>5</td>
<td>ON</td>
</tr>
</tbody>
</table>
SECTION IV

DRAWINGS

VDM-1 VIDEO DISPLAY MODULE

Processor Technology
APPENDICES

VDM-1 VIDEO DISPLAY MODULE
APPENDIX I

STATEMENT OF WARRANTY
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX I

STATEMENT of WARRANTY

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by Processor Technology Corporation are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 6 months following the date of purchase. The defective part must be returned postpaid to Processor Technology Corporation within the warranty period.

Any malfunctioning module, purchased as a kit and returned to Processor Technology within the warranty period, which in the judgement of P.T. Corp. has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, with a minimal charge to cover postage and handling.

Any modules purchased as a kit and returned to P.T. Corp. which in the judgement of P.T. Corp. are not covered by the above conditions will be repaired and returned at a cost commensurate with the work required. In no case will this charge exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least 6 months following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same 6 month period. All warranted factory assembled units returned to P.T. Corp. postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.
APPENDIX II

8080 OPERATING CODE
### Hex ASCII Table

<table>
<thead>
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<th>Hex</th>
<th>ASCII</th>
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<tr>
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<td></td>
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<tr>
<td>0x1F</td>
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</tr>
</tbody>
</table>
APPENDIX III

LOADING DIP DEVICES

and

SOLDERING TIPS
LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

1. Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

2. Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

3. Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

4. Press the device straight down until it seats on the points where the pins widen.

5. Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

1. Use a low-wattage iron — 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

2. Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

3. Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

   NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

4. In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).

5. Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

6. Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

7. To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.
APPENDIX IV

INTEGRATED CIRCUIT PIN CONFIGURATIONS
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX IV

MCM6574, 6575 or 6576

See Section III for complete patterns of these generators.

74LS00

positive logic:
\( Y = A \bar{B} \)

74LS02

positive logic:
\( Y = AB \)
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX IV

74LS04

7406

positive logic:
\[ Y = \overline{X} \]

74LS08

74LS10

positive logic:
\[ Y = AB \]

74LS20

74LS86

AIV-3
PROCessor TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX IV

74LS175

8836 or 8T380

DM8131

78L12A

93L16

See 74LS163

AIV-7
APPENDIX V

VDM-1 TERMINAL SOFTWARE
The VDM DRIVER SOFTWARE allows the display of printable data onto a television monitor or a modified regular television. The rate at which the data is displayed is controlled from the keyboard used as the input to the computer. The rate may be set from completely stopped to over 2000 characters per second! The entire display may be cleared from the keyboard and the cursor may be turned on or off as desired. The display format is 16 lines of 64 characters. If the line being displayed exceeds 64 characters the screen is scrolled up and continued on the next screen line. Control characters are not displayed.

The VDM DRIVER program is called by a user output routine or by BASIC depending upon which version is used.

In the BASIC version, a sense switch is used to send the data to either the screen or to a printer.

If you wish to use the VDM with MITS BASIC, use the BASIC-VDM DRIVER program which automatically loads the VDM DRIVER SOFTWARE and links itself to BASIC'S output routines.

For use with other programs the machine language VDM DRIVER should be loaded into memory and called by a users program with the data to be displayed in register B.

BASIC-VDM DRIVER

The BASIC version of the VDM DRIVER operates with the same commands as the machine language version. The display speed may be changed during an active screen, (data being presented). The display and program may also be stopped by typing a 'space bar', and then resumed by typing any key except another space. If an entire line is typed, the display is resumed at the new speed. Changing speed when the display is not active is not possible when running BASIC. The BASIC-VDM DRIVER is also RELOCATABLE and the STATUS BITS and I/O PORTS are AUTOMATICALLY SET to the values your BASIC is running with.

MACHINE LANGUAGE VDM DRIVER

The software requires 512 bytes of memory and may be located anywhere in memory except the first 512 bytes that are used for the relocating hex loader. A simple BINARY loader is used to bootstrap in an Intel format checksum loader that allows the VDM DRIVER software to be placed anywhere in memory. It is usually best to put it in the last 512 bytes of available memory. A users program should CALL to the first location of the VDM DRIVER program with the data in register B. The driver will save the calling programs stack and all of its registers. The data is displayed on the screen and screen operations are performed by the VDM DRIVER, then the calling program's stack and registers are restored and a RETURN is executed.
VDM DRIVER OPERATION

1.) INITIALIZING THE SCREEN AND CURSOR
The first time the VDM software is accessed the cursor position
must be set. Type a SHIFT K or LEFT BRACKET "[". The screen
is cleared and the cursor is set to the bottom left.

SCREEN CONTROL COMMANDS FOR BASIC
CONTROL Z: CLEAR SCREEN AND INITIALIZE CURSOR
CONTROL A: TURN CURSOR ON/OFF

SCREEN CONTROL COMMANDS FOR MACHINE LANGUAGE SOFTWARE
SHIFT K or LEFT BRACKET ([: CLEAR SCREEN & INITIALIZE CURSOR
SHIFT M or RIGHT BRACKET (]): TURN CURSOR OFF/ON
SHIFT L or BACKSLASH (\): SET SPEED [not in BASIC program]
   This command will allow the display speed to be changed
   when there is no active display movement. " NEW SPEED (1-9)? "
   will appear on the screen. A number 1 thru 9 may then be typed
   and the display speed will be adjusted accordingly. Any other
   character typed will cause no change in the speed.

   1 = NO DELAY   [ about 2000 CPS or 2000 60 char lines per min ]
   9 = GREATEST DELAY  [ about 1.5 characters per second ]

SPEED CONTROL:
   During active display, (driver program being accessed),
   the speed may be changed or the display stopped.
   Type a number 1-9 and the speed will change and remain set at
   that speed until changed again. If the SPACE BAR is typed
during display action, the screen will freeze until any key
   other than the space bar is typed. If a number is typed,
   the display will resume at the new speed, otherwise the display
   will resume at the last set speed. The SPACE BAR may be used
to 'SINGLE STEP' the display.

NOTE: IN PROGRAMS SUCH AS "BASIC" THAT ALTER THE DATA
AVAILABLE FLAG, IT MAY BE NECESSARY TO HIT A SPEED CONTROL
VALUE TWICE. THE SAME IS TRUE FOR "BREAK" OR CONTROL "C"
IN "BASIC".

MACHINE LANGUAGE VDM DRIVER LOADING INSTRUCTIONS

1.) SET THE BINARY BOOTSTRAP LOADER LISTED HEREIN INTO MEMORY
STARTING AT LOCATION ZERO (0).

AV-2
2.) SET THE SENSE SWITCHES TO THE DESIRED MEMORY LOCATION WHERE THE DRIVER SOFTWARE IS TO RESIDE.

THE 8 SENSE SWITCHES ARE USED BY THE LOADER AS THE STARTING HIGH ORDER BYTE OF MEMORY ADDRESS TO LOAD THE SOFTWARE INTO THE CORRECT LOCATION AND TO ADJUST THE HIGH ORDER ADDRESSES REFERENCED BY THE VDM DRIVER PROGRAM INTERNALLY.

Example:
TO LOAD THE DRIVER STARTING AT 4E00 (HEX); (047000 octal)
THE SENSE SWITCHES SHOULD BE SET TO READ 4E (HEX).

A15-down A14-up A13-down A12-down : A11-up A10-up A9-up A8-down

THE DRIVER WILL THEN LOAD INTO LOCATIONS 4E00H TO 4FFFH.
470000 TO 474000

!!! MAKE SURE YOU SET THE SENSE SWITCHES PRIOR TO LOADING !!!!!!!
Note: The driver will not load into locations 0-1FF as the loading routine resides there during load time.

3.) READ IN THE VDM DRIVER PAPER TAPE STARTING ON THE BLANK LEADER AT THE BEGINNING OF THE TAPE.
Note: There are two sections of the paper tape. The first is the hex loader that is bootstrapped into locations 25H-138H.
The second part starts at the blank area on the tape about 3 feet from the beginning, and is the VDM DRIVER software in hexadecimal checksum relocate format.
The binary load routine first loads the hex loading routine and then jumps to that routine and reads in the hexadecimal format VDM DRIVER software. The jump may be noted by a change in the front panel lights. The 'input' light should be on during the reading of the tape by the load routine.

4.) WHEN THE PAPER TAPE HAS BEEN READ THE PROGRAM OUTPUTS "LOAD COMPLETE" TO THE LOAD DEVICE PORT AND ENTERS A HOLD LOOP. THE VDM DRIVER MAY THEN BE CALLED BY ANY PROGRAM. THE DATA IN REGISTER "B" WILL BE DISPLAYED ON THE SCREEN. THE CALLING POINT WILL BE THE FIRST LOCATION USED BY THE DRIVER.

THE SCREEN MUST BE INITIALIZED THE FIRST TIME IT IS ACCESSED. TYPE 'SHIFT K' TO CLEAR SCREEN AND INITIALIZE CURSOR.

5.) ERRORS DURING LOADING
A. IF THE SENSE Switches INDICATE 0 OR 1, THE PROGRAM WILL PRINT "SET SENSE SWITCHES" TO THE LOAD DEVICE PORT.
The Switches SHOULD BE SET TO THE DESIRED ADDRESS AND THE PAPER TAPE REPOSITIONED TO ITS SECOND BLANK AREA. EXAMINE LOCATION 25H (0450) AND HIT "RUN", AND TURN ON THE TAPE READER.
B. IF THE LOADER CANNOT VERIFY THAT THE DATA LOADED IS CORRECT, "MEMORY ERROR" WILL BE OUTPUT TO THE LOAD DEVICE PORT. CHECK TO SEE THAT THE SENSE SWITCHES ARE SET TO THE CORRECT ADDRESS AND THAT MEMORY IS UNPROTECTED.

C. IF THE CHECKSUM VALUE EACH 26 BYTES IS NOT CORRECT, "CHECKSUM ERROR" WILL BE OUTPUT. TRY READING THE TAPE AGAIN FROM THE SECOND BLANK AREA. RESTART THE LOADER PROGRAM FROM LOCATION 25H. IF CHECKSUM ERRORS STILL OCCUR, EITHER THE PAPER TAPE IS BAD OR IS NOT BEING READ PROPERLY.

6.) PORT ADDRESS AND STATUS BITS

THE PAPER TAPE AND LISTING ARE SET UP WITH THE FOLLOWING:

STATUS PORT = 0
DATA PORT = 1
DATA AVAILABLE FLAG BIT = 40H { 1000 } ACTIVE HIGH
TRANSMITTER BUFFER EMPTY BIT = 80H { 2000 } ACTIVE HIGH

ALL REFERENCE TO THIS SET UP IS INDICATED ON THE LISTINGS BY AN ARROW " <------<<< ".
IF YOUR STATUS IS ACTIVE LOW, CHANGE THE BYTES INDICATED BY AN ARROW " <--[ J(N)Z ]--<<< " TO "JNZ" OR "JZ" AS NEEDED. IF YOUR STATUS IS ACTIVE LOW, THE INSTRUCTIONS WILL BE THE OPPOSITE OF THOSE IN THE LISTING.

BASIC-VDM DRIVER LOADING INSTRUCTIONS

1.) LOAD BASIC

!!! IMPORTANT !!!

2.) LEAVE AT LEAST 512 BYTES OF MEMORY FREE ABOVE YOUR RESPONSE TO THE QUESTION "MEMORY SIZE?" DURING THE INITIALIZATION OF BASIC. THERE MUST BE ROOM FOR THE DRIVER ABOVE BASIC! EXAMPLE: IF YOU HAVE 20K OF MEMORY THEN THE DECIMAL EQUIVALENT IS 20480. 20480-512 = 19968 WHICH IS THE MAXIMUM VALUE YOU SHOULD TYPE FOR "MEMORY SIZE".

AV-4
IT IS A GOOD IDEA TO SET THE "TERMIAL WIDTH" TO 63 FOR USE WITH THE VDM.

3.) AFTER BASIC INITIALIZED AND PRINTS "OK", TYPE "NEW", TYPE "NULL 0", AND LOAD IN THE BASIC-VDM DRIVER PROGRAM.

4.) PUT SENSE SWITCH A8 UP AND TYPE 'RUN'.
THE PROGRAM WILL ASK FOR INFORMATION REGARDING DESTINATION LOCATION, VDM MEMORY ADDRESS, VDM PORT ASSIGNMENT, ETC..

"WAIT A MOMENT....." !!! IMPORTANT !!!
WHEN THE PROGRAM TYPES "WAIT A MOMENT....", IT IS PEEKING THROUGH ITSELF TO DETERMINE STATUS AND I/O VALUES, PATCH POINTS, AND LOADING THE VDM DRIVER SOFTWARE INTO MEMORY. THIS MAY TAKE 30 TO 60 SECONDS. ALL THE FRONT PANEL LIGHTS GO ON AND THEY LOOK VERY STILL; BUT DON'T START TO WORRY THAT THE PROGRAM HAS CRASHED...UNTIL ABOUT 2 MINUTES.......THEN WORRY.

5.) SENSE SWITCH A8 WILL NOW CONTROL THE DESTINATION OF OUTPUT.
WHEN THE SWITCH IS UP, DATA WILL GO TO THE DEVICE BASIC WAS SET UP FOR SUCH AS A TELETYP. WITH THE SWITCH DOWN, THE DATA WILL BE DISPLAYED ON THE TV SCREEN. THE SWITCH MAY BE CHANGED AT ANY TIME, INCLUDING DURING OUTPUT.

6.) TYPE CONTROL Z
THE FIRST TIME THE SCREEN IS ACCESSED IT MUST BE INITIALIZED.

.....you won't use so much paper now
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0000 0002
0000 0003
0000 0004 <<< VDM DRIVER BOOTSTRAP LOADER >>>
0000 0005 BINARY
0000 0006
0000 0007 THIS PROGRAM IS USED TO ROOTSTRAP IN THE
0000 0008 VDM DRIVER SOFTWARE, THE FIRST PART OF
0000 0009 THE VDM TAPE IS AN INTEL HEX CHECKSUM
0000 0010 LOADER THAT IS USED TO RELOCATE THE VDM
0000 0011 DRIVER CODE ACCORDING TO THE SETTING OF
0000 0012 THE SENSE SWITCHES ON THE FRONT PANEL.
0000 0013 PLEASE REFER TO LOADING INSTRUCTIONS
0000 0014 FOR FURTHER INFORMATION ON THE LOADING
0000 0015 PROCEDURE.
0000 0016
0000 0017 LOAD THIS PROGRAM STARTING AT LOCATION ZERO (0)
0000 0018
0000 0019
0000 21 25 00 0020 BEGIN LXI H,STACK SET MEMORY ADDRESS
0003 F9 0021 SPH L, SET STACK POINTER
0004 4C 0022 MOV C,H CLEAR REG C
0005 CD 19 00 0023 CALL IN GET BINARY BYTE
0008 FE 7F 0024 CPI 7FH WAIT FOR START BYTE
000A C2 00 00 0025 JNZ BEGIN
000D 0026
000D 0D 0027 CHRN DCR C DECREMENT BYTE COUNT
000E CA 25 00 0028 JZ STACK JUMP TO HEX LOADER IF DONE
0011 CD 19 00 0029 CALL IN GET BYTE
0014 77 0030 MOV M,A PUT IT IN MEMORY
0015 23 0031 INX H NEXT MEMORY ADDRESS
0016 C3 OD 00 0032 JMP CHRN GET ANOTHER BYTE
0019 0033
0019 DB 00 0034 IN IN STAT GET CHR <<<<<<
001A E6 80 0035 ANI DAY DATA AVAILABLE? <<<<<<
001D CA 19 00 0036 JZ IN NO- WAIT
0020 DB 01 0037 IN IN DATA GET DATA <<<<<<
0022 C9 0038 RET
0023 0039
0023 0040 DS 2
0025 0041 STACK EQU 8 STACK ADDRESS
0026 0042
0026 0043
0026 0044 DATA EQU 1 DATA PORT <<<<<<
0026 0045 STAT EQU 0 STATUS PORT <<<<<<
0026 0046 DAV EQU 40H DATA AVAILABLE <<<<<<
0026 0047
0026 0048
0026 0049

BEGIN 0000 0025
CHRN 000D 0032
DATA 0001 0037
DAV 0040 0038
IN 0019 0023 0029 0036
STACK 0025 0026 0028
STAT 0000 0034

AV-6
PROCESSOR TECHNOLOGY CORPORATION  
VDM-1 VIDEO DISPLAY MODULE  
APPENDIX V

0025 0001 *  
0025 0002 *  
0025 0003 *  "INTEL CHECKSUM HEX LOADER FOR VDM-DRIVER >>"  
0025 0004 *  
0025 0005 *  
0025 0006 *  "VERSION 2.0 APRIL 11, 1976 S. DOMPIER"  
0025 0007 *  
0025 0008 *  "THIS IS A MODIFICATION OF AN INTEL HEX CHECKSUM"  
0025 0009 *  "LOADER TO ALLOW RE-LOCATABLE LOADING OF THE"  
0025 0010 *  "VDM-DRIVER SOFTWARE. THE HIGH ADDRESS IS RCVD"  
0025 0011 *  "FROM THE SENSE SWITCHES, ZERO OR ONE NOT ALLOWED."  
0025 0012 *  
0025 0013 *  
0025 0014 FIRST LXI SP,STACK STACK ADDRESS  
0026 06 3A 0015 START MVI B,'1': START OF RECORD  
0026 CD 18 01 0016 CALL INB GET CHARACTER  
0026 90 0017 SUB B RECORD MARK?  
0026 C2 28 00 0018 JNZ START NO-WAIT FOR RECORD MARK  
0031 57 0019 MOV D,A CLEAR CHECKSUM  
0032 CD C0 00 0020 CALL READ GET RECORD LENGTH  
0035 CA 7D 00 0021 JZ DONE IF RECORD.O THEN DONE  
0038 5F 0022 MOV E,A RECORD LENGTH IN REG E  
0039 CD E6 00 0023 CALL OFFSET GET MSB FROM DATA  
003C 61 0024 MOV H,C GET MSR FROM DATA  
003D CD C0 00 0025 CALL READ GET LSB OF ADDRESS  
0040 6F 0026 MOV L,A LSB IN REG L  
0041 CD C0 00 0027 CALL READ SKIP RECORD TYPE  
0044 0028 *  
0044 CD E6 00 0029 GETCH CALL OFFSET GET CHARACTER  
0047 71 0030 MOV H,C PUT CHR IN MEMORY  
004B BE 0031 CMP M CHECK IF MEMORY IS OK  
0049 C2 71 00 0032 JNZ MERR NO MEMORY ERROR  
004C 23 0033 INX H NEXT ADDRESS  
004D 1D 0034 DCR E RECORD LENGTH -1  
004E C2 44 00 0035 JNZ GETCH GET MORE  
0051 CD C0 00 0036 CALL READ' GET CHECKSUM  
0054 CA 28 00 0037 JZ START OK- GET NEXT RECORD  
0057 0038 *  
0057 21 83 00 0039 CERR LXI H,CHKER CHECKSUM ERROR  
005A CD FE 00 0040 MSG CALL CPLF  
005D 76 0041 MSG2 MOV A,M  
005E FE 56 0042 CPI 'X'  
0060 CA 69 00 0043 JZ HOLD  
0063 47 0044 MOV B,A  
0064 CD 00 01 0045 CALL OUTR PRINT CHR  
0067 23 0046 INX H  
0068 C3 50 00 0047 JMP MSG2  
006B 0048 *  
006B CD FE 00 0049 HOLD CALL CRLF  
006E C3 60 00 0050 HOLD2 JMP HOLD2  
0071 0051 *  
0071 21 92 00 0052 MERR LXI H,ERR MEMORY ERROR  
0074 C3 5A 00 0053 JMP MSG  
0077 21 9F 00 0054 WHAT LXI H,SENSW SET SENSE SWITCHES  
007A C3 5A 00 0055 JMP MSG  
007D 21 B2 00 0056 DONE LXI H,LCMP LOAD COMPLETE  
0080 C3 5A 00 0057 JMP MSG  
0083 0058 *  
0083 H 48 45 43 0059 CHKER ASC "CHECKSUM ERROR"  
4B 53 55 4D 20 45 52 52 4F 52 58  

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<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction</th>
<th>Description</th>
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<tbody>
<tr>
<td>0009h</td>
<td>4D 45 4D 4F</td>
<td>MOV EAX, 0x45</td>
</tr>
<tr>
<td>000FH</td>
<td>3F 45 54 20</td>
<td>MOV EBX, 0x54</td>
</tr>
<tr>
<td>0012h</td>
<td>3F 45 4E 53</td>
<td>MOV EDX, 0x4E</td>
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<td>0015h</td>
<td>20 53 57</td>
<td>MOV ESI, 0x53</td>
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<td>0018h</td>
<td>45 53 48</td>
<td>MOV ESP, 0x53</td>
</tr>
<tr>
<td>001Bh</td>
<td>45 53 5B</td>
<td>MOV EBP, 0x53</td>
</tr>
<tr>
<td>001Eh</td>
<td>4C 4F 42</td>
<td>MOV ECX, 0x42</td>
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<tr>
<td>0021h</td>
<td>4F 41 44</td>
<td>MOV EDI, 0x41</td>
</tr>
<tr>
<td>0024h</td>
<td>20 43 4F 4D</td>
<td>MOV EBX, 0x4D</td>
</tr>
<tr>
<td>0027h</td>
<td>50 4C 45 54</td>
<td>MOV ESI, 0x54</td>
</tr>
<tr>
<td>002Ah</td>
<td>45 58</td>
<td>MOV ESP, 0x58</td>
</tr>
<tr>
<td>0000h</td>
<td>006A READ</td>
<td>CALL NIBBLE GET BYTE</td>
</tr>
<tr>
<td>0003h</td>
<td>0055 RLC</td>
<td>MOV LSB 8 BITS TO MSB 8 BITS</td>
</tr>
<tr>
<td>0006h</td>
<td>0066 RLC</td>
<td></td>
</tr>
<tr>
<td>0009h</td>
<td>0067 RLC</td>
<td></td>
</tr>
<tr>
<td>000Ch</td>
<td>0068 RLC</td>
<td></td>
</tr>
<tr>
<td>000Fh</td>
<td>0069 MOV</td>
<td>C,A SAVE NIBBLE</td>
</tr>
<tr>
<td>0012h</td>
<td>0070 CALL</td>
<td>NIBBLE</td>
</tr>
<tr>
<td>0015h</td>
<td>0071 ORA</td>
<td>C</td>
</tr>
<tr>
<td>0018h</td>
<td>0072 MOV</td>
<td>C,A CHARACTER IN REG C</td>
</tr>
<tr>
<td>001Bh</td>
<td>0073 ADD</td>
<td>D</td>
</tr>
<tr>
<td>001Eh</td>
<td>0074 MOV</td>
<td>D,A CHECKSUM IN REG D</td>
</tr>
<tr>
<td>0021h</td>
<td>0075 NO</td>
<td>MOV A,C</td>
</tr>
<tr>
<td>0024h</td>
<td>0076 NO</td>
<td>RET</td>
</tr>
<tr>
<td>0027h</td>
<td>0077 NIBBLE CALL INR GET CHR</td>
<td></td>
</tr>
<tr>
<td>002Ah</td>
<td>0079 SUI</td>
<td>'0' REMOVE ASCII Bias</td>
</tr>
<tr>
<td>002Dh</td>
<td>0080 RC</td>
<td>DONE IF 0-2PH</td>
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<td>002Fh</td>
<td>0081 ADI</td>
<td>'O'-'G'</td>
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<td>0033h</td>
<td>0082 RC</td>
<td>DONE IF 47H-50FH</td>
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<td>0035h</td>
<td>0083 ADI</td>
<td>6</td>
</tr>
<tr>
<td>0037h</td>
<td>0084 JP</td>
<td>NIB2 ADD 10 IF A-F</td>
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<td>0039h</td>
<td>0085 ADI</td>
<td>7</td>
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<tr>
<td>003Bh</td>
<td>0086 RC</td>
<td>DONE IF 3AH-40H</td>
</tr>
<tr>
<td>003Dh</td>
<td>0087 NIB2</td>
<td>ADI 10</td>
</tr>
<tr>
<td>003Fh</td>
<td>0088 ORA</td>
<td>A SET ZERO FLAG</td>
</tr>
<tr>
<td>0041h</td>
<td>0089 RET</td>
<td></td>
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<td>0043h</td>
<td>0090 NIBBLE CALL INR GET CHR</td>
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</tr>
<tr>
<td>0046h</td>
<td>0091 OFFSET CALL READ GET CHR</td>
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</tr>
<tr>
<td>0049h</td>
<td>0092 SUI</td>
<td>8 CHECK IF 8 OR 9</td>
</tr>
<tr>
<td>004Bh</td>
<td>0093 JZ</td>
<td>YES</td>
</tr>
<tr>
<td>004Fh</td>
<td>0094 CPI</td>
<td>1</td>
</tr>
<tr>
<td>0053h</td>
<td>0095 JNZ</td>
<td>NO</td>
</tr>
<tr>
<td>0055h</td>
<td>0096 YES</td>
<td>MOV C,A</td>
</tr>
<tr>
<td>0057h</td>
<td>0097 IN</td>
<td>OFFH READ SENSE SWITCHES</td>
</tr>
<tr>
<td>0059h</td>
<td>0098 CPI</td>
<td>2 MUST BE &gt; 1</td>
</tr>
<tr>
<td>005Bh</td>
<td>0099 JC</td>
<td>WHAT NO- ERROR</td>
</tr>
<tr>
<td>005Dh</td>
<td>0100 ADD</td>
<td>C ADD OFFSET</td>
</tr>
<tr>
<td>005Fh</td>
<td>0101 MOV</td>
<td>C,A</td>
</tr>
<tr>
<td>0061h</td>
<td>0102 RET</td>
<td></td>
</tr>
<tr>
<td>0063h</td>
<td>0103 NIBBLE CALL INR GET CHR</td>
<td></td>
</tr>
<tr>
<td>0066h</td>
<td>0104 CRLF</td>
<td>MVI B,ODH CARRIAGE RETURN</td>
</tr>
<tr>
<td>0069h</td>
<td>0105 CALL</td>
<td>OUTB</td>
</tr>
<tr>
<td>006Ch</td>
<td>0106 MVI</td>
<td>B,ODH LINE FEED</td>
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<tr>
<td>006Fh</td>
<td>0107 CALL</td>
<td>OUTB</td>
</tr>
<tr>
<td>0072h</td>
<td>0108 MVI</td>
<td>B,7FH FILL</td>
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<tr>
<td>0075h</td>
<td>0109 CALL</td>
<td>OUTB</td>
</tr>
<tr>
<td>0078h</td>
<td>0110 RET</td>
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</tr>
<tr>
<td>007Bh</td>
<td>0111 OUTB</td>
<td>IN STAT</td>
</tr>
</tbody>
</table>

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

010F E6 80 0112 ANI THR <-----
0111 CA 0D 01 0113 JZ OUTB
0114 78 0114 MOV A,B
0115 D3 01 0115 OUT DATA <-----
0117 C9 0116 RET
0118 0117*
0118 DB 00 0118 INB IN STAT CHECK STATUS PORT <-----
011A E6 40 0119 ANI DAV DATA AVAILABLE? <-----
011C CA 18 01 0120 JZ INR NO WAIT <-(J(N)Z)-><-----
011F DB 01 0121 IN DATA GET CHR FROM DATA PORT <-----
0121 E6 7F 0122 ANI 7FH
0123 C9 0123 RET
0124 0124 0124*
0124 0125 STAT EQU 0 STATUS PORT <-----
0124 0127 DATA EQU 1 DATA PORT <-----
0124 0128 DAV EQU 40H DATA AVAILABLE <-----
0124 0129 THR EQU 80H TRANSMITTER BUFFER EMPTY <-----
0124 0130*
0124 0131 DS 20 STACK AREA
0138 0132 STACK EQU *
0138 0133*
0138 0134*

CERR 0057
CHKEF 0083 0039
CRLF 00FE 0040 0040
DATA 0001 0115 0121
DAV 0040 0119
DONE 007D 0021
ERN 0092 0052
FIRST 0025
GETCH 0044 0035
HOLD 0068 0043
HOLD2 006E 0050
INB 0118 0016 0078 0120
LCMP 0082 0056
MERR 0071 0032
MSG 005A 0053 0055 0057
MSG2 005D 0047
NIB2 0062 0084
NIBBL 0081 0064 0070
NO 00CF 0095
OFFSE 0086 0023 0029
OUTB 010D 0045 0105 0107 0109 0113
READ 00C0 0020 0025 0027 0036 0091
SENSW 009F 0054
STACK 0138 0014
START 0028 0018 0037
STAT 0000 0111 0116
TBE 0080 0112
WHAT 0077 0099
YES 00F3 0093

AV-9
0800 0001 •
0800 0002 •
0800 0003 •
0800 0004 •
0800 0005 • VERSION 3.0 APRIL 12, 1976 S. DOMPIER
0800 0006 •
0800 0007 •
0800 0008 •
0800 0009 •
0800 0010 •
0800 0011 • THIS ROUTINE SAVES THE CALLING STACK,
0800 0012 • PERFORMS SCREEN OPERATIONS AND RETURNS
0800 0013 • TO THE CALLING PROGRAM AFTER RESTORING
0800 0014 • THE SYSTEM STACK. IT MAY BE USED WITH
0800 0015 • PTCO. "SOFTWARE PACKAGE #1" WITH
0800 0016 • EXCELLENT RESULTS. THE CHARACTER TO BE
0800 0017 • DISPLAYED SHOULD BE IN REGISTER B.
0800 0018 •
0800 0019 •
0800 3333 • VDM MEMORY ADDRESS = CC000
0800 3333 • VDM PORT = C8
0800 3333 • DATA PORT = 1
0800 3333 • STATUS PORT = 0
0800 3333 • DAY = 40H
0800 3333 • TBC = 80H
0800 3333 •
0800 3333 • CALL HERE WITH CHARACTER IN REG R
0800 0020 •
0800 0021 •
0800 0022 •
0800 0023 • VDM SHLD HLSAY SAVE NL
0800 22 B7 09 0024 LXI H, D
0800 31 00 00 0025 DAD SP GET SYSTEM STACK POINTER
0800 31 F0 09 0026 LXI SP, STACK SET NEW STACK
0800 0E 05 0027 PUSH H SAVE SYSTEM STACK POINTER
0800 0D 05 0028 PUSH D SAVE ALL REGISTERS
0800 0C 05 0029 PUSH B
0800 0D F6 0030 PUSH PSW
0800 CD 1A 08 0031 CALL SCREEN DO SCREEN OPERATIONS
0801 F1 0032 POP PSW RESTORE REGISTERS
0801 C1 0033 POP B
0801 D1 0034 POP D
0801 04 0035 POP H
0801 F9 0036 SPHL RESTORE SYSTEM STACK
0801 2A B7 09 0037 LHLD HLSAY RESTORE NL
0810 C9 0038 RET . BACK TO CALLING PROGRAM
081A 0039 •
081A 0040 •
081A 78 0041 • SCREEN MOV A,B GET CHR
081B E6 7F 0042 ANI TPFH STRIP MSB
081D FE 7F 0043 CPI TPF DON'T WANT DELETE
081F C8 0044 RZ
0820 FE 5F 0045 CPI SPPH BACKSPACE? (shift 0)
0822 CA 20 09 0046 JZ BKSPA
0825 FE 5B 0047 CPI "(' CLEAR SCREEN? (shift K)
0827 CA CE 08 0048 JZ CLE
082A FE 5D 0050 CPI "}" CURSOR OFF/ON? (shift L)
082C CA 41 08 0051 JZ CURTO
082F FE 5C 0052 CPI "\" SPEED CONTROL? (shift L)
0831 CA 81 08 0053 JZ SETSP
0834 FE 0D 0054 CPI ODH CARRIAGE RETURN?

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VDM-1 VIDEO DISPLAY MODULE  

0836 CA 15 09  0055  JZ  CHOT2
0839 FE 20  0056  CPI  20H
083B D8  0057  RC .  DON'T DISPLAY CONTROL CHR
083C 0058 *  083C 0059 *  OUTPUT TIMER
083C 0060 *  083C 0061 *  083C 0062 *  083C 0063 *  083C 0064 *
083C F5  0065  MOV  H.A  SET COUNTER IN HL
083D 3A B6 09  0066  LOD  SPEED  GET DELAY TIME
083E 67  0067  JNC  77  TO BIG
083F 2E 80  0068  CPI '1'
0840 DA 77 08  0069  JC  WAIT TO SMALL
0841 E6 00  0070  CPI  0H  JUST RIGHT REMOVE ASCII PRIAS
0842 0F  0071  ANI  OFH  INITIALIZE DELAY BIT IN CARRY
0843 CF  0072  JMP  NEXT
0844 C3 60 08  0073  JMP  LESS NEXT ROUND
0845 00 00  0074  CMP  ASCII NUMBER 1-9
0846 FE 3A  0075  MOV  NUM CK  '0'-1  NO CHECK IF ASCII NUMBER 1-9
0847 D2 77 08  0076  MOV  JNC  WAIT TO BIG
0848 31  0077  CPI  1'
0849 DA 77 08  0078  JC  WAIT TO SMALL
084A E6 00  0079  ANI  OFH  JUST RIGHT REMOVE ASCII PRIAS
084B 4F  0080  MOV  C,A  SAVE DELAY NUMBER
084C AF  0081  MOV  A,A  CLEAR ACCUMULATOR
084D 37  0082  XRA  A  CLEAR ACCUMULATOR
084E 77  0083  STC .  INITIALIZE DELAY BIT IN CARRY
084F 0D  0084  CMP  LESS DCR C DECREMENT DELAY NUMBER
0850 C9 60 08  0085  MOV  JZ  POUND STOP ROTATING DELAY BIT
0851 17  0086  MOV  RAL .  SHIFT DELAY BIT LEFT
0852 C3 61 08  0087  JMP  LESS NEXT ROUND
0853 32 B6 09  0088  MOV  STA SPEED STORE DELAY TIME
0854 C9  0089  JMP  RET
0855 28  0090 *  0856 7C  0091 *  0857 87  0092 *
0858 0D  0093  MOV  A,H  GET HIGH BYTE OF DELAY COUNT
0859 E6 00  0094  CMP  ORA A IS IT ZERO?
085A CF  0095  CMP  JNZ NEXT NO DELAY SOME MORE
085B C9 00 09  0096  CMP  JMP CHOUT TO THE SCREEN!
085C 00 00  0097 *  085D 00 00  0098 *
085E FE 20  0099 WAIT CPI  20H SPACE BAR?
085F C9 00 09  0100 *  085E 7C  0092 NEXT2 MOV A,H GET HIGH BYTE OF DELAY COUNT
0860 87  0093  ORA A IS IT ZERO?
0861 C2 6D 08  0094  CMP  JNZ NEXT NO DELAY SOME MORE
0862 F1  0095  CMP  POP PSW GET CHR
0863 C3 00 09  0096  JMP  JMP CHOUT TO THE SCREEN!
0864 00 00  0097 *  0865 28  0098 *
0866 FF 20  0099 WAIT CPI  20H SPACE BAR?
0867 C9 00 09  0100 *  0866 7C  0092 NEXT2 MOV A,H GET HIGH BYTE OF DELAY COUNT
0868 87  0093  ORA A IS IT ZERO?
0869 C2 6D 08  0094  CMP  JNZ NEXT NO DELAY SOME MORE
086A 00 00  0095  JMP  JMP CHOUT TO THE SCREEN!
086B 00 00  0096 *
086C FF 20  0097 WAIT CPI  20H SPACE BAR?
086D C9 00 09  0100 *  086E 7C  0092 NEXT2 MOV A,H GET HIGH BYTE OF DELAY COUNT
086F 87  0093  ORA A IS IT ZERO?
0870 C2 6D 08  0094  CMP  JNZ NEXT NO DELAY SOME MORE
0871 F1  0095  CMP  POP PSW GET CHR
0872 C3 00 09  0096  JMP  JMP CHOUT TO THE SCREEN!
0873 00 00  0097 *
0874 FF 20  0098 *
0875 C9 00 09  0100 *  0876 7C  0092 NEXT2 MOV A,H GET HIGH BYTE OF DELAY COUNT
0877 00 00  0093 *
0878 C3 00 09  0094  JMP  JMP CHOUT TO THE SCREEN!
0879 00 00  0095 *
087A FF 20  0096 WAIT CPI  20H SPACE BAR?
087B 00 00  0097 *
087C FF 20  0098 *  087D 00 00  0099 *  087E 00 00  009A *  087F 00 00  009B *
0880 7C 00 00  009C *
0881 00 00  009D *
0882 00 00  009E *
0883 00 00  009F *
0884 FF 20  00A0 SETSP CALL CHOT2
0885 C9 00 09  00A1 SET1 MOV A,M SPEED MESSAGE
0886 FF 58  00A2 CALL CHOT2
0887 00 00  00A3 SET1 MOV A,M SPEED MESSAGE
0888 FE 58  00A4 CALL CHOT2
0889 C9 00 09  00A5 RET  SET DISPLAY SPEED
088A FF 20  00A6 *  088B FF 20  00A7 *  088C FF 20  00A8 *  088D FF 20  00A9 *
088E FF 20  00A0 *  088F FF 20  00A1 *  0890 FF 20  00A2 *  0891 FF 20  00A3 *
0892 23  00A4 *  0893 00 00  00A5 *

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0891 C3 87 08 0117 JMP SET1
0896 CD 17 09 0118 SET2 CALL STATUS GET NEW SPEED
0899 CA 96 08 0119 JZ SET2 WAIT FOR IT <------ [J(N)Z] ------><<
089C CD AC 09 0120 CALL INPUT GET NUMBER
089F FE 3A 0121 CPI "*" +1
08A1 D2 B4 08 0122 JNC OPPS TO BIG
08A4 FE 31 0123 CPI "!" OPPS TO SMALL
08A6 DA B4 08 0124 JC OPPS TO SMALL
08A9 F5 0125 PUSH PSW SAVE IT
08AA CD 00 09 0126 CALL CHOT DISPLAY IT
08AB CD 15 09 0127 CALL CHOT2
08B0 F1 0128 POP PSW
08B1 C3 52 08 0129 JMP NUMCK
08B4 21 CC 08 0130 OPPS LXI H, MSG + 18 PRINT "?"
08B7 C3 87 08 0131 JMP SET1
08BA 20 4E 55 57 0132 MSG ASC " NEW SPEED (1-9)? X"
 20 53 50 45
 45 44 20 28
 31 2D 39 29
 3F 20 20 56
08CE 0133 "
08CE 0134 "
08CE 0135 "CLEAR SCREEN & INITIALIZE CURSOR"
08CE 0136 "
08CE 21 00 CC 0137 CLR LXI H, VDMBASE VDM MEMORY ADDRESS <------<<
08D1 TC 0138 MOV A, H
08D2 C6 04 0139 ADI 4 VDM MEMORY TOP
08D4 36 20 0140 CLR2 MVI M, 1 CLEAR SCREEN
08D6 23 0141 INX H
08D7 BC 0142 CMP H
08DB C2 D4 08 0143 JNZ CLR2
08DB AF 0144 XRA A
08DC 32 B4 09 0145 STA BOSL BEGINNING SCREEN LINE
08DF 32 B5 09 0146 STA BOTL BEGINNING TEXT LINE
08E2 32 B2 09 0147 STA CCP CURRENT CURSOR POINTER
08E5 2F 0148 CMA
08E6 32 B3 09 0149 STA CURF CURSOR FLAG
08E9 36 0F 0150 MVI A, 15 SET CURSOR AT SCREEN BOTTOM
08EB 32 B1 09 0151 STA CLW CURRENT LINE NUMBER
08EB CD F2 08 0152 CALL VDMOT SET VDM
08F1 C9 0153 RET
08F2 0154 "
08F2 0155 "
08F2 0156 "OUTPUT BOSL AND BOTL TO VDM"
08F2 0157 "
08F2 3A B4 09 0158 VDMOT LDA BOSL INITIALIZE VDM
08F5 07 0159 RLC
08F6 07 0160 RLC
08F7 07 0161 RLC
08F8 07 0162 RLC
08F9 21 B5 09 0163 LXI H, BOSL
08FC B6 0164 GRA M
08FD D3 C8 0165 OUT VDMDEV VDM PORT ADDRESS <------<<
08FF C9 0166 RET
0900 0167 "
0900 0168 "
0900 0169 "STORE CHARACTER IN VDM MEMORY"
0900 0170 "
0900 0171 "
0900 4F 0172 CHOUT MOV C, A SAVE CHR
0901 3A B2 09 0173 LDA CCP GET CURRENT CURSOR POINTER
0904 47 0174 MOV B, A

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094b 3a b1 09 0175  lda cln  get line number
0908 cd 70 09 0176  call clna  convert to address
090b 71 09 0177  mov m,c  put character on screen
090c 3a b2 09 0178  lda ccp  advance cursor
090f 3c 09 0179  inr a
0910 ff 40 09 0180  cfi 64 wrap around?
0912 c2 23 09 0181  jnz chot1
0915 3a b2 09 0182  chot2 lda ccp
0918 47 09 0183  mov b,a
0919 3a b1 09 0184  lda cln
091c cd 9f 09 0185  call ccur  clear cursor
091f cd 52 09 0186  call scrl  scroll up
0922 97 09 0187  sub a  set cursor to left margin
0923 32 b2 09 0188  chot1 sta ccp
0926 47 09 0189  mov b,a
0927 3a b1 09 0190  lda cln
092a 3c 83 09 0191  jmp scun  set cursor on/off
092d 092d 09 0192  b
092d 092d 09 0193  b
092d 092d 09 0194  b space and erase last chr
092d 092d 09 0195  b
092d 3a b2 09 0196  bkspa lda ccp  get cursor pointer
0930 47 09 0197  mov b,a
0931 3a b1 09 0198  lda cln
0934 cd 9f 09 0199  call ccur  clear cursor
0937 2b 09 0200  dcx h
0938 36 20 09 0201  mvi h,0 clear chr
093b 3a b1 09 0202  lda cln
093e 3c 83 09 0203  jmp scun  set cursor
0941 0941 09 0205  b
0941 0941 09 0206  b
0941 0941 09 0207  cursor display (off-on)
0941 0941 09 0208  b
0941 3a b3 09 0209  curtg lda curf  get cursor flag
0944 2f 09 0210  cma
0945 32 b3 09 0211  sta curf  switch it
0948 3a b2 09 0212  lda ccp  get cursor pointer
094a 47 09 0213  mov b,a
094c 3a b1 09 0214  lda cln  get line number
094f 3c 83 09 0215  jmp scun  cursor on/off
0952 0952 09 0216  b
0952 0952 09 0217  b
0952 0952 09 0218  scroll screen up
0952 0952 09 0219  b
0952 21 b5 09 0220  scrl lxi h,botl
0955 b5 09 0221  push m
0956 7e 09 0222  mov a,m
0957 34 09 0223  inr m
0958 96 09 0224  sub m
0959 01 00 00 09 0225  lxi b,0
095c cd 70 09 0226  call clna
095f 01 40 20 09 0227  lxi b,2040h
0962 70 09 0228  scrl2 mov m,b clear bottom line
0963 3c 09 0229  inr l
0964 0d 09 0230  dcn c
0966 c2 62 09 0231  jnz scrl2
0968 81 09 0232  pop h
0969 7e 09 0233  mov a,m
096a e6 0f 09 0234  ani mph
096c 77 09 0235  mov m,a
096d 3c f2 08 0236  jmp vdmot

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PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0970  0237 *
0970  0238 *
0970  0239 * CONVERT LINE NUMBER IN REG A AND CHR
0970  0240 * POSITION IN REG B TO ADDRESS IN HL
0970  0241 *
0970 6F  0242 CLNA MOV L,A
0971 3A B5 09  0243 LDA BOLT LOAD THE OFFSET FOR LINE 0
0974 85  0244 ADD L REG A LOW 4 BITS IS LINE NUMBER
0975 0F  0245 RRC
0976 0F  0246 RRC
0977 6F  0247 MOV L,A
0978 E6 03  0248 ANI 3
097A C6 CC  0249 ADI VDMPAGE <------>
097C 67  0250 MOV H,A
097D 7D  0251 MOV A,L
097E E6 C0  0252 ANI OCR
0980 80  0253 ADD B
0981 6F  0254 MOV L,A
0982 C9  0255 RET
0983  0256 *
0983  0257 *
0983  0258 * SET CURSOR TO LINE IN REG A AND
0983  0259 * CHARACTER POSITION IN REG B
0983  0260 *
0983 E6 0F  0261 SCUR ANI 0FH
0986 32 B1 09  0262 STA CLN
0988 CD 70 09  0263 CALL CLNA
0988 7B  0264 MOV A,B
098C 32 B2 09  0265 STA CCP
098F 3A B3 09  0266 LDA CURP
0992 B7  0267 ORA A
0993 7E  0268 MOV A,M
0994 CA 9B 09  0269 JZ CCUR2
0997 FE 80  0270 ORI 80H
0999 77  0271 MOV M,A
099A C9  0272 RET
099B E6 7F  0273 CCUR2 ANI 7FH
099D 77  0274 MOV M,A
099E C9  0275 RET
099F  0276 *
099F  0277 * CLEAR CURSOR FROM LINE IN REG A
099F  0278 * AND POSITION IN REG B
099F  0279 *
099F CD 70 09  0280 CCUR CALL CLNA
09A2 7E  0281 MOV A,M
09A3 E6 7F  0282 ANI 7FH
09A5 77  0283 MOV M,A
09A6 C9  0284 RET
09A7  0285 *
09A7  0286 *
09A7  0287 * SPEED CONTROL INPUT ROUTINE
09A7  0288 *
09A7 DB 00  0289 STATUS IN STAT STATUS PORT <------>
09A9 E6 40  0290 ANI DAV DATA AVAILABLE? <------
09AB C9  0291 RET
09AC  0292 *
09AC DB 01  0293 INPUT IN DATA DATA PORT <------
09AD E6 7F  0294 ANI 7FH STRIP MSR
09B0 C9  0295 RET
09B1  0296 *
09B1  0297 *
09B1 0298 * RAM STORAGE

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PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0981 0299 *
0981 00 0300 CLN DB 0 CURRENT LINE NUMBER
0982 00 0301 CCP DB 0 CURRENT CURSOR POSITION
0983 01 0302 CURF DB 1 CURSOR DISPLAY FLAG
0984 00 0303 BOSL DB 0 BEGINNING OF SCREEN LINE
0985 00 0304 BOTL DB 0 BEGINNING OF TEXT LINE
0986 06 0305 SPEED DB 6 DELAY BYTE
0987 0306 HLSAV DS 2 USER HL
0989 0307 *
0989 0308 *
0989 0309 SP EQU 6
0989 0310 PSW EQU 6
0989 0311 VMDXEN EQU 0C8H VDM OUTPUT PORT <---<---
0989 0312 VDMستان EQU 0CC0H VDM MEMORY ADDRESS <---<---
0989 0313 VDMPAGE EQU VDMستان/256 <---<---
0989 0314 *
0989 0315 *
0989 0316 STAT EQU 0 STATUS PORT <---<---
0989 0317 DATA EQU 1 DATA PORT <---<---
0989 0318 TRE EQU 80H TRANSMITTER BUFFER EMPTY <---<---
0989 0319 DAV EQU 40H DATA AVAILABLE <---<---
0989 0320 *
0989 0321 *
0989 0322 STACK EQU 09FOH STACK AREA
0989 0323 *
0989 0324 *

BKSPA 092D 0047
Bosl 0984 0149 015B
BOTL 0985 0146 0163 0220 0283
CCF 0982 0147 0173 0178 0182 0188 0196 0212 0265
CCUR 098F 0185 0199
CCURZ 0998 0269
CGO71 0923 0181
CGRST 0915 0055 0108 0127
CMOUT 0900 0096 0114 0126
CLN 0981 0151 0175 0184 0190 0198 0203 0214 0262
CLNA 0970 0176 0226 0263 0280
CLR 08CE 0049
CLR2 08D4 0143
CLRF 0983 0149 0209 0211 0266
CMR7C 0911 0051
DATA 0001 0293
DAV 0040 0290
FOUNO 0869 0085
HLSAV 0987 0023 0037
INPUT 09AC 0069 0120
LUSS 0861 0087
MOS 088A 0109 0130
MEXT 086D 0071 0094
MEXTZ 086E 0068
NUMCK 0852 0070 0129
OPPS 0884 0122 0124
PSW 0006 0030 0032 0063 0095 0125 0128
SCRE 081A 0051
SCLR 0912 0186
SCRL2 0962 0237
SCUR 0983 0191 0204 0215
SET1 0887 0117 0131
SET2 0866 0112 0119
SETSP 0881 0053
SP 0006 0025 0026

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<th>09B6</th>
<th>0064 0088</th>
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<td>0026</td>
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<tr>
<td>Stat</td>
<td>0000</td>
<td>0289</td>
</tr>
<tr>
<td>Status</td>
<td>09A7</td>
<td>0067 0101 0118</td>
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<tr>
<td>TBE</td>
<td>0080</td>
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<tr>
<td>Timer</td>
<td>083C</td>
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<td>00CB</td>
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<td>08F2</td>
<td>0152 0236</td>
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<tr>
<td>VDMFA</td>
<td>00CC</td>
<td>0249</td>
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<tr>
<td>Wait</td>
<td>0877</td>
<td>0077 0079</td>
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<tr>
<td>Wait2</td>
<td>087A</td>
<td>0102</td>
</tr>
</tbody>
</table>
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

0000 REM
0002 REM << BASIC TO VDM-1 LINK PROGRAM >>>
0004 REM
0006 REM PROCESSOR TECHNOLOGY CORP.
0008 REM 6200 HOLLIS STREET
0010 REM EMERYVILLE, CALIFORNIA 94608
0012 PRINT
0014 A$="(HEX) IS YOUR LAST ADDRESS, INPUT:"
0016 B$="GIVE ME YOUR VDM":C$="ADDRESS IN DECIMAL"
0018 PRINT"<< VDM TO BASIC LOADING AND LINKING PROGRAM >>>
0020 PRINT." WRITTEN IN BASIC LANGUAGE BY GORDON FRENCH":PRINT
0022 PRINT"REMEMBER, IF YOU DID NOT LEAVE THE LAST 512 BYTES"
0024 PRINT"OF YOUR LAST 4K OF MEMORY FREE WHEN RESPONDING"
0026 PRINT"TO ' MEMORY SIZE? ' WHEN THIS BASIC WAS"
0028 PRINT"LOADED, YOU MUST RELOAD BASIC WITH THE CORRECTED"
0030 PRINT"MEMORY SIZE!":PRINT:PRINT
0032 PRINT"INPUT DECIMAL NUMBER OF YOUR LAST 4K BOUNDARY"
0034 PRINT"EXAMPLE: IF 4FFF "A$" 4(RETURN)"
0036 PRINTTAB(10)"IF 5FFF "A$" 5(RETURN)
0037 PRINTTAB(10)"IF AFFF "A$"10(RETURN) ETC."
0038 INPUT L:IF L<7 THEN S=0:GOTO 46
0040 PRINT"IS THIS 12K EXTENDED BASIC? (Y/N)":INPUT D$
0042 IF D$="Y" THEN S=65536:GOTO 46
0044 IF D$="N" THEN 40
0046 GOTO 84
0048 IF L>15 OR L=0 THEN 32
0050 PRINT"IS YOUR VDM MEMORY ADDRESS CC00(HEX)"
0052 PRINT" WITH PORT=CB? (Y/N)"
0054 INPUT D$:IF D$="Y"GOTO 64
0056 PRINT$" MEMORY STARTING "C$:INPUT V2
0058 V1=INT(V2/256):V2=(V2/256)-INT(V2/256)*256
0060 PRINT$: PORT "C$:INPUT V3:IF V3>255 GOTO 60
0062 GOTO 68
0064 V1=20H:V2=0:V3=200:V4=192
0066 PRINT"A MOMENT PLEASE..."
0070 S=0
0072 FOR K=0 TO 4096
0074 A=PEEK(K+)
0076 B=PEEK(K+1)
0078 IF A = 219 AND B = 0 GOTO 92
0080 IF A = 219 AND B = 1 THEN I=K:GOTO 106
0082 NEXT K
0084 PRINT"IT IS NOT POSSIBLE TO LINK VDM-1";
0086 PRINT" TO THIS BASIC BY MEANS"
0088 PRINT"OF THIS PROGRAM. SORRY!"
0090 GOTO 146
0092 IF S>0 THEN GOTO 100
0094 =PEEK(K+2):D=PEEK(K+3):E=PEEK(K+4):F=K+4
0096 IF C<230 THEN GOTO 82
0098 S=S+1:G=K:GOTO 82

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0100 H=PEEK(K+3):J=0
0102 F=F-256:J=J+1:IF F>256 GOTO 102
0104 GOTO 82
0106 FOR Y=1 TO L+409
0108 READ Z
0110 IF Z<300 GOTO 138
0112 IF Z=300 THEN Z=V3: GOTO 138
0114 IF Z=400 THEN Z=V2: GOTO 138
0116 IF Z=500 THEN Z=V1: GOTO 138
0118 IF Z=1001 THEN Z=P+1: GOTO 138
0120 IF Z=1000 THEN Z=P: GOTO 138
0122 IF Z=2000 THEN Z=D: GOTO 138
0124 IF Z=3000 THEN Z=E: GOTO 138
0126 IF Z=4000 THEN Z=F: GOTO 138
0128 IF Z=5000 THEN Z=J: GOTO 138
0130 IF Z=6000 THEN Z=H: GOTO 138
0132 PRINT"THIS PROGRAM LOAD IS BAD."
0134 PRINT"PLEASE RELOAD THIS PROGRAM."
0136 GOTO 146
0138 POKE Y,Z: NEXT Y
0140 POKE G,195:POKE G+1,0:POKE G+2,P
0142 POKE I,205:POKE I+1,110:POKE I+2,P+1:POKE I+3,0
0144 PRINT"VDM-1 IS NOW LINKED TO BASIC":PRINT
0145 PRINT"DO NOT ATTEMPT TO RE-RUN THIS PROGRAM !":PRINT
0146 RESTORE
0148 NULL 0
0150 END
0152 DATA 219, 255, 31, 210, 13, 1000, 219, 0, 230, 2000
0154 DATA 195, 4000, 5000, 241, 230, 127, 254, 32, 210, 43
0156 DATA 1000, 254, 7, 194, 30, 1000, 245, 195, 6, 1000
0158 DATA 254, 13, 202, 46, 1000, 254, 1, 202, 46, 1000
0160 DATA 254, 26, 192, 254, 127, 200, 245, 229, 213, 197
0162 DATA 205, 58, 1000, 193, 209, 225, 241, 201, 246, 58
0164 DATA 146, 1001, 103, 46, 128, 205, 105, 1001, 300, 104
0166 DATA 1000, 205, 110, 1001, 50, 140, 1001, 254, 58, 210
0168 DATA 112, 1000, 254, 49, 218, 112, 1000, 230, 15, 79
0170 DATA 175, 55, 13, 202, 100, 1000, 23, 195, 92, 1000
0172 DATA 146, 1001, 43, 124, 183, 194, 103, 1000, 195
0174 DATA 181, 1000, 254, 32, 194, 103, 1000, 205, 105, 1001
0176 DATA 1000, 177, 1000, 195, 103, 1000, 33, 400, 500, 124
0178 DATA 198, 4, 54, 32, 35, 188, 194, 132, 1000, 175
0180 DATA 146, 1001, 50, 145, 1001, 50, 142, 1001, 47
0182 DATA 146, 1001, 50, 145, 1001, 50, 142, 1001, 47
0184 DATA 1000, 62, 13, 245, 195, 181, 1000, 58, 144, 1001
0186 DATA 7, 7, 7, 33, 145, 1001, 182, 211, 300
0188 DATA 201, 58, 142, 1001, 71, 241, 254, 13, 202, 223
0190 DATA 1000, 254, 95, 202, 243, 1000, 254, 1, 202, 3
0192 DATA 1000, 254, 26, 202, 126, 1000, 79, 58, 141, 1001
0194 DATA 205, 50, 1001, 113, 58, 142, 1001, 60, 254, 64
0196 DATA 194, 233, 1000, 58, 141, 1001, 205, 97, 1001, 205
0198 DATA 20, 1001, 151, 50, 142, 1001, 71, 58, 141, 1001
0200 DATA 195, 69, 1001, 58, 141, 1001, 205, 97, 1001, 43
PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

| 0202  | DATA54, 32, 5, 58, 141, 1001, 195, 69, 1001, 58  |
| 0204  | DATA143, 1001, 47, 50, 143, 1001, 58, 142, 1001, 71  |
| 0206  | DATA58, 141, 1001, 195, 69, 1001, 33, 145, 1001, 229  |
| 0208  | DATA126, 52, 150, 3, 120, 0, 205, 50, 1001, 1  |
| 0210  | DATA54, 32, 112, 144, 13, 194, 36, 1001, 225, 126  |
| 0212  | DATA230, 15, 119, 195, 167, 1000, 111, 58, 145, 1001  |
| 0214  | DATA133, 15, 15, 111, 230, 3, 198, 600, 103, 125  |
| 0216  | DATA230, 192, 128, 111, 201, 230, 15, 50, 141, 1001  |
| 0218  | DATA205, 50, 1001, 120, 50, 142, 1001, 58, 143, 1001  |
| 0220  | DATA183, 126, 202, 93, 1001, 246, 128, 119, 201, 230  |
| 0222  | DATA127, 119, 201, 205, 50, 1001, 126, 230, 127, 119  |
| 0224  | DATA201, 219, 0, 230, 6000, 201, 58, 140, 1001, 254  |
| 0226  | DATA31, 194, 125, 1001, 245, 175, 50, 140, 1001, 241  |
| 0228  | DATA201, 219, 1, 230, 127, 254, 1, 202, 46, 1000  |
| 0230  | DATA254, 26, 202, 46, 1000, 201, 0, 0, 0, 1  |
| 0232  | DATA0, 0, 0, 0, 0, 0, 0, 0, 0, 0  |

AV-19
Television Interface

Anyone with a bunch of memory circuits, control logic and a wire wrap gun can whip up a digital video generator with TTL output levels. The problem as I see it is to get that digital video signal into a form that the TV set can digest. The care and feeding of digital inputs to the TV set is the subject of Don Lancaster's contribution to BYTE 2 — an excerpt from his forthcoming book, TV Typewriter Cookbook, to be published by Howard W. Sams, Indianapolis, Indiana.

... CARL

We can get between a TV typewriter and a television style display system either by an rf modulator or a direct video method.

In the rf modulator method, we build a miniature, low power, direct wired TV transmitter that clips onto the antenna terminals of the TV set. This has the big advantage of letting you use any old TV set and ending up with an essentially free display that can be used just about anywhere. No set modifications are needed, and you have the additional advantage of automatic safety isolation and freedom from shock problems.

There are two major restrictions to the rf modulator method. The first of these is that transmitters of this type must meet certain exactly spelled out FCC regulations and that system type approval is required. The second limitation is one of bandwidth. The best you can possibly hope for is 3.5 MHz for black and white and only 3 MHz for color, and many economy sets will provide far less. Thus, long character line lengths, sharp characters, and premium (lots of dots) character generators simply aren't compatible with clip-on rf entry.

In the direct video method, we enter the TV set immediately following its video detector but before sync is picked off. A few premium TV sets and all monitors already have a video input directly available, but these are still expensive and rare. Thus, you usually have to modify your TV set, either adding a video input and a selector switch or else dedicating the set to exclusive TV typewriter use. Direct video eliminates the bandwidth restrictions provided by the tuner, if strip, and video detector filter. Response can be further extended by removing or shorting the 4.5 MHz sound trap and by other modifications to provide us with longer line lengths and premium characters. No FCC approval is needed, and several sets or monitors are easily driven at once without complicated distribution problems.

There are two limitations to the direct video technique. One is that the set has to be modified to provide direct video entry. A second and far more severe, restriction is that many television sets are "hot chassis" or ac0 sets with one side of their chassis connected to the power line. These sets introduce a severe shock hazard and cannot be used as TV typewriter video entry displays unless some isolation technique is used with them. If the TV set has a power transformer, there is usually no shock problem. Transistor television sets and IC sets using no vacuum tubes tend to have power transformers, as do older premium tube type sets. All others (around half the sets around today) do not.

Direct Video Methods

With either interface approach, we usually start by getting the dot matrix data, blanking, cursor, and sync signals together into one composite video signal whose
form is useful to monitors and TV sets. A good set of standards is shown in Fig. 1. The signal is dc coupled and always positive going. Sync tips are grounded and blacker than black. The normal open circuit black level is positive by one-half a volt, and the white level is two volts positive. In most TV camera systems, intermediate levels between the half volt black level and the two volt white level will be some shade of gray, proportionately brighter with increasing positive voltage. With most TV typewriter systems, only the three states of zero volts (sync), half a volt (black), and two volts (white dot) would be used. One possible exception would be an additional one volt dot level for a dim but still visible portion of a message or a single word.

The usual video source impedance is either 72 or 100 Ohms. Regardless of how far we travel with a composite video output, some sort of shielding is absolutely essential.

For short runs from board to board or inside equipment, tightly twisted conductors should be OK, as should properly guarded PC runs. Fully shielded cables should be used for interconnections between the TVI and the monitor or TV set, along with other long runs. As long as the total cable capacitance is less than 500 pF or so (this is around 18 feet of RG178-U miniature coax), the receiving end of the cable need not be terminated in a 72 or 100 Ohm resistor. When terminated cable systems are in use for long line runs or multiple outputs, they should be arranged to deliver the signal levels of Fig. 1 at their output under termination. Generally, terminated cable systems should be avoided as they need extra in the way of drivers and supply power.

The exact width of the horizontal and vertical sync pulses isn't usually too important, so long as the shape and risetime of these pulses are independent of position control settings and power supply variations. One exception to this is when you're using a color receiver and a color display. Here, the horizontal sync pulse should be held closely to 5.1 microseconds, so the receiver's color burst sampling does in fact intercept a valid color burst. More on this later.

Intentional Smear

Fig. 2 shows a typical composite video driver using a 4066 quad analog switch. It gives us a 100 Ohm output impedance and the proper signal levels. Capacitor C1 is used to purposely reduce the video rise and fall times. It is called a smearing capacitor.

Why would we want to further reduce the bandwidth and response of a TV system that's already hurting to begin with? In the case of a quality video monitor, we wouldn't. But if we're using an ordinary run-of-the-mill TV set, particularly one using rf entry, this capacitor can very much improve the display legibility and contrast. Why?

Because we are interested in getting the most legible character of the highest contrast we can. This is not necessarily the one having the sharpest dot rise and fall times. Many things interact to determine the upper video response of a TV display. These include the tuner settings and the rf response and alignment, the video detector response, video peaking, the sound trap setting, rf cable reflections, and a host of other responses. Many of these stages are underdamped and will ring if fed too sharp a risetime input, giving us a ghosted, shabby, or washed out character. By reducing the video bandwidth going into the system, we can move the dot matrix energy lower in frequency, resulting in cleaner characters of higher contrast.

For most TV displays, intentional smearing will help the contrast, legibility, and overall appearance. The ultimate limit to this occurs when the dots overlap and become illegible. The
Fig. 3. Block diagram of typical B and W television.

The optimum amount of intentional smear is usually the value of capacitance that is needed to just close the inside of a "W" presented to the display.

Adding a Video Input

Video inputs are easy to add to the average television set, provided you follow some reasonable cautions. First and foremost, you must have an accurate and complete schematic of the set to be modified, preferably a Sams Photofact or something similar. The first thing to check is the power supply on the set. If it has a power transformer and has the chassis properly safety isolated from the power line, it's a good choice for a TVT monitor. This is particularly true of recent small screen, solid state portable TV sets. On the other hand, if you have a hot chassis type with one side of the power line connected to the chassis, you should avoid its use if at all possible. If you must use this type of set, be absolutely certain to use one of the safety techniques outlined later in Fig. 8.

A block diagram of a typical TV set appears in Fig. 3. UHF or VHF signals picked up by the tuner are downconverted in frequency to a video i-f frequency of 44 MHz and then filtered and amplified. The output of the video i-f is transformer coupled to a video detector, most often a small signal germanium diode. The video detector output is filtered to remove the carrier and then routed to a video amplifier made up of one or more tubes or transistors.

At some point in the video amplification, the black and white signal is split three ways. First, a reduced bandwidth output routes sync pulses to the sync separator stage to lock the set's horizontal and vertical scanning to the video. A second bandsplit output sharply filtered to 4.5 MHz extracts the FM sound subcarrier and routes this to a sound i-f amplifier for further processing. The third output is video, which is strongly amplified and then capacitively coupled to the cathode of the picture tube.

The gain of the video amplifier sets the contrast of the display, while the bias setting on the cathode of the picture tube (with respect to its grounded control grid) sets the display brightness. Somewhere in the video amplifier, further rejection of the 4.5 MHz sound subcarrier is usually picked up to minimize picture interference. This is called a sound trap. Sound traps can be a series resonant circuit to ground, a parallel resonant circuit in the video signal path, or simply part of the transformer that is picking off the sound for more processing.

The video detector output is usually around 2 volts peak to peak and usually subtracts from a white level bias setting. The stronger the signal, the more negative the swing, and the blacker the picture. Sync tips are blacker than black, helping to blank the display during retrace times.
Fig. 4 shows the typical video circuitry of a transistor black and white television. Our basic circuit consists of a diode detector, a unity gain emitter follower, and a variable gain video output stage that is capacitively coupled to the picture tube. The cathode bias sets the brightness, while the video gain sets the contrast. Amplified signals for sync and sound are removed from the collector of the video driver by way of a 4.5 MHz resonant transformer for the sound and a low pass filter for the sync. A parallel resonant trap set to 4.5 MHz eliminates sound interference. Peaking calls on each stage extend the bandwidth by providing higher impedances and thus higher gain to high frequency video signals.

Note particularly the biasing of the video driver. A bias network provides us with a stable source of 3 volts. In the absence of input video, this 3 volts sets the white level of the display, as well as establishing proper bias for both stages. As an increasing signal appears at the last video output transformer, it is negatively rectified by the video detector, thus lowering the 3 volts proportionately. The stronger the signal, the blacker the picture. Sync will be the strongest of all, giving us a blacker than black bias level of only one volt.

The base of our video driver has the right sensitivity we need for video entry, accepting a maximum of a 2 volt peak to peak signal. It also has the right polarity, for a positive going bias level means a whiter picture. But, an unmodified set is already biased to the white level, and if we want to enter our own video, this bias must be shifted to the black level.

We have a choice in any TV of direct or ac coupling of our input video. Direct coupling is almost always better as it eliminates any
shading effects or any change of background level as additional characters are added to the screen. Fig. 5 shows how we can direct couple our video into a transistor black and white set. We provide a video input, usually a BNC or a phono jack, and route this to a PNP Darlington transistor or transistor pair, borrowing about 5 mH from the set’s +12 volt supply. This output is routed to the existing video driver stage through a SPDT switch that either picks the video input or the existing video detector and bias network.

The two base-emitter diode drops in our Darlington transistor add up to a 1.2 volt positive going offset, so, in the absence of a video input or at the base of a sync tip, the video driver is biased to a blacker than black sync level of 1.2 volts. With a white video input of 2 volts, the video driver gets biased to its usual 3.2 volts of white level. Thus, our input transistor provides just the amount of offset we need to match the white and black bias levels of our video driver. Note that the old bias network is on the other side of the switch and does nothing in the video position.

Two other ways to offset our video input are to use two ordinary transistors connected in the Darlington configuration, or to use one transistor and a series diode to pick up the same amount of offset, as shown in Fig. 5. If more or less offset is needed, diodes or transistors can be stacked up further to pick up the right amount of offset.

The important thing is that the video driver ends up with the same level for white bias and for black bias in either position of the switch.

As or capacitively coupled video inputs should be avoided. Fig. 6 shows a typical circuit. The TV’s existing bias network is lowered in voltage by adding a new parallel resistor to ground to give us a voltage that is 0.6 volts more positive than the blacker than black sync tip voltage. For instance, with a 3 volt white level, and 2 volt peak to peak video, the sync tip voltage would be 1 volt; the optimum bias is then 1.6 volts. Input video is capacitively coupled by a fairly large electrolytic capacitor in parallel with a good high frequency capacitor. This provides for a minimum of screen shading and still couples high frequency signals properly. A clamping diode constantly clamps the sync tips to their bias value, with the 0.6 volt drop of this diode being taken out by the extra 0.6 volts provided for in the bias network. This clamping diode automatically holds the sync tips to their proper value, regardless of the number of white dots in the picture. Additional bypassing of the bias network by a large electrolytic may be needed for proper operation of the clamping diode, as shown in Fig. 6. Note that our bias network is used in both switch positions – its level is shifted as needed for the direct video input.

Tube type sets present about the same interface problems as the solid state versions do. Fig. 7 shows a typical direct coupled tube interface. In the unmodified
circuit, the white level is zero volts and the sync tip black level is minus two volts. If we can find a negative supply (scarce in tube type circuits), we could offset our video in the negative direction by two volts to meet these bias levels.

Instead of this, it is usually possible to self bias the video amplifier to a cathode voltage of +2 volts. This is done by breaking the cathode to ground connection and adding a small resistor (50 to 100 Ohms) between cathode and ground to get a cathode voltage of +2 volts. Once this value is found, a heavy electrolytic bypass of 100 microfarads or more is placed in parallel with the resistor. Switching then grounds the cathode in the normal rf mode and makes it +2 volts in the video entry mode.

In the direct video mode, a sync tip grounded input presents zero volts to the grid, which is self biased minus two volts with respect to the cathode. A white level presents +2 volts to the grid, which equals zero volts grid to cathode.

Should there already be a self bias network on the cathode, it is increased in value as needed to get the black rather than white level bias in the direct video mode.

Hot Chassis Problems

There is usually no shock hazard when we use clip-on rf entry or when we use a direct video jack on a transformer-powered TV. A very severe shock hazard can exist if we use direct video entry with a TV set having one side of the power line connected to the chassis. Depending on which way the line cord is plugged in, there is a 50-50 chance of the hot side of the power line being connected directly to the chassis.

Hot chassis sets, particularly older, power hungry tube versions, should be avoided entirely for direct video entry. If one absolutely must be used, some of the suggestions of Fig. 8 may ease the hazard. These include using an isolation transformer, husky back-to-back filament transformers, three wire power systems, optical coupling of the video input,
and total package isolation. Far and away the best route is simply never to attempt direct video entry onto a hot chassis TV.

Making the Conversion

Fig. 9 sums up how we modify a TV for direct video entry. Always have a complete schematic on hand, and use a transformer style TV set if at all possible. Late models, small screen, medium to high quality solid state sets are often the best display choice. Avoid using junk sets, particularly very old ones. Direct coupling of video is far preferable to ac capacitor coupling. Either method has to maintain the black and white bias levels on the first video amplifier stage. A shift of the first stage quiescent bias from normally white to normally black is also a must. Use short, shielded leads between the video input jack and the rest of the circuit. If a changeover switch is used, keep it as close to the rest of the video circuitry as you possibly can.

Extending Video and Display Bandwidth

By using the direct video input route, we eliminate any bandwidth and response restrictions of an rf modulator, the tuner, video i-f strip, and the video detector filter. Direct video entry should bring us to a 3 MHz bandwidth for a color set and perhaps 3.5 MHz for a black and white model, unless we are using an extremely bad set. The resultant 6 to 7 million dot per second rate is adequate for short character lines of 32, 40, and possibly 48 characters per line. But the characters will smear and be illegible if we try to use longer line lengths and premium (lots of dots) character generators on an ordinary TV. Is there anything we can do to the set to extend the video bandwidth and display response for these longer line lengths?

In the case of a color TV, the answer is probably no. The video response of a color set is limited by an essential delay line and an essential 3.58 MHz trap. Even if we were willing to totally separate the chrominance and luminance channels, we'd still be faced with an absolute limit set by the number of holes per horizontal line in the shadow mask of the tube. This explains why video color displays are so expensive and so rare. Later on, we'll look at what's involved in adding color to the shorter line lengths.

With a black and white TV, there is often quite a bit

Fig. 8. Getting Around a Hot Chassis Problem.

Hot chassis problems can be avoided entirely by using only transformer-powered TV circuits; by using clip-on rf entry. If a hot chassis set must be used, here are some possible ways around the problem:

1. Add an isolation transformer.

A 110 volt to 110 volt isolation transformer whose wattage exceeds that of the set may be used. These are usually expensive, but a workable substitute can be made by placing two large surplus filament transformers back to back. For instance, a pair of 24 volt, 4 Amp transformers can handle around 100 Watts of set.

2. Use a three wire system with a solid ground.

Three prong plug wiring, properly polarized, will force the hot chassis connection to the cold side of the power line. This protection is useful only when three wire plugs are used in properly wired outlets. A severe shock hazard is reintroduced if a user elects to use an adaptor or plugs the system into an unknown or improperly wired outlet. The three wire system should NOT be used if anyone but yourself is ever to use the system.

3. Optically couple the input video.

Light emitting diode-photocell pairs are low in cost and can be used to optically couple direct video, completely isolating the video input from the hot chassis. Most of these optoelectronic couplers do not have enough bandwidth for direct video use; the Litronix TL-100 is one exception. Probably the simplest route is to use two separate opto-isolators, one for video and one for sync, and then recombine the signals inside the TV on the hot side of the circuit.

4. Use a totally packaged and sealed system.

If you are only interested in displaying messages and have no other input/output devices, you can run the entire circuit hot chassis, provided everything is sealed inside one case and has no chassis-to-people access. Interface to teletypes, cassettes, etc., cannot be done without additional isolation, and servicing the circuit presents the same shock hazards that servicing a hot chassis TV does.

AVI-7
we can do to present long lines of characters, depending on what set you start out with and how much you are willing to modify the set.

The best test signal you can use for bandwidth extension is the dot matrix data you actually want to display, for the frequency response, time delay, ringing, and overshoot all get into the act. What we want to end up with is a combination that gives us reasonably legible characters.

A good oscilloscope (15 MHz or better bandwidth) is very useful during bandwidth extension to show where the signal loses its response in the circuit. At any time during the modification process, there is usually one response bottleneck. This, of course, is what should be attacked first. Obviously the better a TV you start with, the easier it will be the task. Tube type gutsless wonders, particularly older ones, will be much more difficult to work with than with a modern, small screen, quality solid state portable.

Several of the things we can do are watching the control settings, getting rid of the sound trap, minimizing circuit strays, optimizing spot size, controlling peaking, and shifting to higher current operation. Let's take a look at these in turn.

Control Settings

Always run a data display at the lowest possible contrast and using only as much brightness as you really need. In many circuits, low contrast means a lower video amplifier gain, and thus less of a gain-bandwidth restriction.

Eliminate the Sound Trap

The sound trap adds a notch at 4.5 MHz to the video response. If it is eliminated or switched out of the circuit, a wider video bandwidth automatically

Fig. 9. How to Add a Direct Video Input to a TV Set.

1. Get an accurate and complete schematic of the set — either from the manufacturer's service data or a Photofact set. Do not try adding an input without this schematic!

2. Check the power supply to see if a power transformer is used. If it is, there will be no shock hazard, and the set is probably a good choice for direct video use. If the set has one side of the power line connected to the chassis, a severe shock hazard exists, and one of the techniques of Fig. 8 should be used. Avoid the use of hot chassis sets.

3. Find the input to the first video amplifier stage. Find out what the white level and sync level bias voltages are. The marked or quiescent voltage is usually the white level; sync is usually 2 volts less. A transistor TV will typically have a +3 volt white level and a -1 volt sync level. A tube type TV will typically have a zero volt white level and a -2 volt sync level.

4. Add a changeover switch using minimum possible lead lengths. Add an input connector, either a phono jack or the premium BNC type connector. Use shielded lead for interconnections exceeding three inches in length.

5. Select a circuit that couples the video and biases the first video amplifier stage so that the white and sync levels are preserved. For transistor sets, the direct coupled circuits of Fig. 5 may be used. For tube sets, the circuit of Fig. 7 is recommended. Avoid the use of ac coupled video inputs as they may introduce shading problems and changes of background as the screen is filled.

6. Check the operation. If problems with contrast or sync tearing crop up, recheck and adjust the white and sync input levels to match what the set uses during normal operation. Note that the first video stage must be biased to the white level during rf operation and to the sync level for direct video use. The white level is normally two volts more positive than the sync level.
Fig. 10. Removing the sound trap can extend video bandwidth.
(a) Response
(b) Parallel resonant trap — short or bypass.
(c) Series resonant trap — open or remove.
(d) Combined trap and pickup — open or remove (series resonant); short or bypass (parallel resonant).

results. Fig. 10 shows us the response changes and the several positions for this trap. Generally, series resonant traps are opened and parallel resonant traps are shorted or bypassed through suitable switching or outright elimination. The trap has to go back into the circuit if the set is ever again used for ordinary program reception. Sometimes simply bucking the slug on the trap all the way out will improve things enough to be useful.

Minimizing Strays
One of the limits of the video bandwidth is the stray capacitance both inside the video output stage and in the external circuitry. If the contrast control is directly in the signal path and if it has long leads going to it, it may be hurting the response. If you are using the TV set exclusively for data display, you can rearrange the control location and simplify and shorten the video output to picture tube interconnections.

Additional Peaking
Most TV sets have two peaking networks. The first of these is at the video detector output and compensates for the vertical sideband transmission signal that makes sync and other low frequency signals double the amplitude of the higher frequency ones. The second of these goes to the collector or plate of the video output stage and raises the circuit impedance and thus the effective gain for very high frequencies. Sometimes you can alter this second network to favor dot presentations.

Fig. 11 shows a typical peaking network and the effects of too little or too much peaking. Note that the stray capacitance also enters into the peaking, along with the video amplifier output capacitance and the picture tube’s input capacitance. Generally, too little peaking will give you low contrast dots, while too much will give you sharp dots, but will run dots together and shift the more continuous portions of the characters objectionably. Peaking is changed by increasing or decreasing the series inductor from its design value.

Running Hot
Sometimes increasing the operating current of the video output stage can increase the system bandwidth — if this stage is in fact the limiting response, and if the power supply can handle the extra current, and if the stage isn’t already parked at its gain-bandwidth peak, and if the extra heat can be gotten rid of without burning anything up. Usually, you can try adding a resistor three times the plate or collector load resistor in parallel, and see if it increases bandwidth by 1/3. Generally, the higher the current, the wider the bandwidth, but watch
carefully any dissipation limits. Be sure to provide extra ventilation and additional heat sinking, and check the power supply for unhappiness as well. For major changes in operating current, the emitter resistors and other biasing components should also be proportionately reduced in value.

Spot Size

Even with excellent video bandwidth, if you have an out-of-focus, blooming, or changing spot size, it can completely mask character sharpness. Spot size ends up the ultimate limit to resolution, regardless of video bandwidth.

Once again, brightness and contrast settings will have a profound effect, with too much of either blooming the spot. Most sets have a focus jumper in which ground or a positive voltage is selected. You can try intermediate values of voltage for maximum sharpness. Extra power supply filtering can sometimes minimize hum and noise modulation of the spot. Anything that externally raises display contrast will let you run with a smaller beam current and a sharper spot. Using circularly polarized filters, graticle masks, or simple colored filters can minimize display washout from ambient lighting. Fig. 12 lists several sources of material for contrast improvement. Much of this is rather expensive, with pricing from $10 to $25 per square foot being typical. Simply adding a hood and positioning the display away from room lighting will also help and is obviously much cheaper.

Direct RF Entry

If we want the convenience of a "free" display, the freedom from hot chassis problems, and "use it anywhere" ability, direct RF entry is the obvious choice. Its two big limitations are the need for FCC type approval, and a limited video bandwidth that in turn limits the number of characters per line and the number of dots per character.

An RF interface standard is shown in Fig. 13. It consists of an amplitude modulated carrier of one of the standard television channel video frequencies of Fig. 14. Channel 2 is most often used with a 55.250 MHz carrier frequency, except in areas where a local commercial Channel 2 broadcast is intolerably strong. Circuit cost, filtering problems, and stability problems tend to increase with increasing channel number.

The sync tips are the strongest part of the signal, representing 100% modulation, often something around 4 millivolts rms across a 300 Ohm line. The black level is 75% of the sync level, or about 3 millivolts for 4 millivolt sync tips. White level is less than 10% of maximum. Note that the signal is weakest when white and strongest when sync. This is the exact opposite of the video interface of Fig. 1.

RF modulators suitable for clip-on RF entry TV typewriter use are called Class 1 TV Devices by the FCC. A Class 1 TV device is supposed to meet the rules and regulations summarized in Fig. 15.

Fig. 14. Television Picture Carrier Frequencies.

Channel 2 .......... 55.25 MHz
Channel 3 .......... 65.75 MHz
Channel 4 .......... 76.25 MHz
Channel 5 .......... 86.75 MHz
Channel 6 .......... 97.25 MHz

Fig. 15. FCC Regulations on Class 1 TV Devices. More complete information appears in part H of Part 15 and subpart F of Part 2 of the Federal Communications Commission Rules and Regulations. It is available at many large technical libraries.

A Class 1 TV device generates a video modulated RF carrier of a standard television channel frequency. It is directly connected to the antenna terminals of the TV set.

The maximum rms of voltage must be less than 6 millivolts using a 300 Ohm output line. The maximum rf voltage on any frequency more than 3 MHz away from the operating channel must be more than 30 dB below the peak in-channel output voltage.

An antenna disconnect switch of at least 60 dB attenuation must be provided. No user adjustments are permitted that would exceed any of the above specifications. Residual rf radiation from case, leads and cabinet must be less than 15 microvolts per meter.

A Class 1 TV device must not interfere with TV reception.

Type approval of the circuit is required. A filing fee of $50 and an acceptance fee of $250 is involved.

Fig. 16 shows us a block diagram of the essential parts of a TV modulator. We start
with a stable oscillator tuned to one of the Fig. 14 frequencies. A crystal oscillator is a good choice, and low cost modules are widely available. The output of this oscillator is then amplitude modulated. This can be done by changing the bias current through a silicon small signal diode. One millimicro of bias current makes the diode show an ac and rf impedance of 26 Ohms. Half a mill will look like 52 Ohms, and so on. The diode acts as a variable resistance attenuator in the rf circuit, whose bias is set and changed by the video circuit.

Since diode modulators are non-linear, we can't simply apply a standard video signal to them and get a standard rf signal out. A differential amplifier circuit called a video slicer may be used to compensate for this non-linearity. The video slicer provides three distinct currents to the diode modulator. One of these is almost zero for the white level, while the other two provide the black and sync levels. A contrast control that sets the slicing level lets you adjust the sync tip height with respect to the black level. The video slicer also minimizes rf getting back into the video. An attenuator to reduce the size of the modulated signal usually follows the diode modulator.

An upper side band filter removes most of the lower sideband from the AM modulated output, giving us a vestigial sideband signal that stays inside the channel band limits. This same filter eliminates second harmonic effects and other spurious noise. The filter's output is usually routed to an antenna disconnect switch and the TV's antenna terminals. A special switch is needed to provide enough isolation.

Some of the actual circuitry involved is shown in Fig. 17. The video slicer consists of a pair of high gain, small signal NPN transistors, while the oscillator is a commercially available module.

RF entry systems always must be direct coupled to the antenna terminals of the set and should never provide any more rf than is needed for a minimum snow-free picture. They should be permanently tuned to a single TV channel. Under no circumstances should an antenna or cable service hookup remain connected to the set during TV use, nor should radiation rather than a direct rf cable connection ever be used.

Color Techniques

We can add a full color capability to a TV typewriter system fairly easily and cheaply — provided its usual black and white video dot rate is low enough in frequency to be attractively displayed on an ordinary color TV. Color may be used to emphasize portions of a message, to attract attention, as part of an electronic game, or as obvious added value to a graphics display. Color techniques work best on TV typewriter systems having a horizontal frequency very near 15,735 Hertz.

All we basically have to do is generate a subcarrier sine wave to add to the video output. The phase of this subcarrier (or its time delay) is shifted with respect to what the phase was immediately after each horizontal sync pulse to generate the various colors.

Fig. 18 shows us the differences between normal color and black and white operation. Black and white baseband video is some 4 MHz wide and has a narrow 4.5 MHz sound subcarrier. The video is amplitude modulated, while the sound is narrow band frequency.
fig. 18. difference between color and black and white spectra.
(a) black and white — baseband video.

modulated. This translates up to a 6 MHz rf channel with a
vestigial lower sideband as shown in fig. 18(b).

to generate color, we add a new pilot or subcarrier at a
magic frequency of 3.579545 MHz — see fig. 18(c). What
was the video is now called the luminance, and is the
same as the brightness in a
black and white system. The
new subcarrier and its
modulation is called the
chrominance signal and
determines what color gets
displayed and how saturated
the color is to be.

since the black and white information is a sampled data
system that is scanned at the
vertical and horizontal rates, there are lots of discrete holes
in the video spectrum that
aren’t used. The color
subcarrier is designed to stuff itself into these holes (exactly
in a NSTC color system, and
pretty much in a TVT
display). Both chrominance
and luminance signals use the

same spectral space, with the
one being where the other
one isn’t, overlapping comb
style.

the phase or relative delay of the chrominance signal
with respect to a reference
determines the instantaneous
color, while the amplitude of
this signal with respect to the
luminance sets the saturation
of the color. Low amplitudes
generate white or pastel
desires, while high amplitudes
of the chrominance signal
produce saturated and deep
colors.

At least eight cycles of a
reference or burst color phase
are transmitted immediately
following each horizontal
timer pulse as a timing
reference, as shown in fig.
19. The burst is around 25%
of maximum amplitude, or
about the peak to peak height
of a sync pulse.

the TV set has been
trained at the factory to sort
all this out. After video
detection, the set splits out
the chrominance channel
with a bandpass amplifier and
then synchronously
demodulates it with respect
to an internal 3.58 MHz
reference. The phase of this
demodulation sets the color
and the amplitude sets the
saturation by setting the

ratios of electron beam
currents on the picture tube’s
red, blue and green guns.

Meanwhile, the luminance
channel gets amplified as
brightness style video. It is
delayed with a delay line to
make up for the time delay
involved in the narrower band
channel processing channel. It is
then filtered with two traps —
the 4.5 MHz sound trap, and
a new trap to get rid of any
remaining 3.58 MHz color
subcarrier that’s left. The
luminance output sets the
overall brightness by
modulating the cathodes of
all three color guns
simultaneously.

Just after each horizontal
timer pulse, the set looks for
the reference burst and uses
this reference in a phase

fig. 19 adding a color reference burst to the back porch of the
horizontal sync pulses.

8 cycles (min)
of 3.57945 MHz
color reference
phase

black
sync
— 5.1μsec
(black & white)

color
detector circuit to keep its own 3.58 MHz reference locked to the version being transmitted.

Fig. 20 shows us the phase angles related to each color with respect to the burst phase. It also shows us the equivalent amount of delay we need for a given phase angle. Since we usually want only a few discrete colors, it’s far easier to digitally generate colors simply by delaying the reference through gates or buffers, rather than using complex and expensive analog phase shift methods.

Strictly speaking, we should control both the chrominance phase and amplitude to be able to do both pastel and strongly saturated colors. But simply keeping the subcarrier amplitude at the value we used for the burst — around 25% of video amplitude — is far simpler and will usually get us useful results.

A circuit to add color to a TV typewriter is shown in Fig. 21. A 3.579545 MHz crystal oscillator drives a string of CMOS buffers that make up a digital delay line. The output delays caused by the propagation delay times in each buffer can be used as

<table>
<thead>
<tr>
<th>Color</th>
<th>Approximate Phase</th>
<th>Approximate Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burst</td>
<td>0°</td>
<td>0</td>
</tr>
<tr>
<td>Yellow</td>
<td>15°</td>
<td>12 nanoseconds</td>
</tr>
<tr>
<td>Red</td>
<td>75°</td>
<td>58 nanoseconds</td>
</tr>
<tr>
<td>Magenta</td>
<td>135°</td>
<td>105 nanoseconds</td>
</tr>
<tr>
<td>Blue</td>
<td>195°</td>
<td>151 nanoseconds</td>
</tr>
<tr>
<td>Cyan</td>
<td>255°</td>
<td>198 nanoseconds</td>
</tr>
<tr>
<td>Green</td>
<td>315°</td>
<td>244 nanoseconds</td>
</tr>
</tbody>
</table>

Fig. 20. Colors Are Generated by Delaying or Phase Shifting the Burst Frequency.

The reference phase and the delayed color outputs go to a one-of-eight data selector. The data selector picks either the reference or a selected color in response to a code presented digitally to the three select lines. The logic that is driving this selector must return to the reference phase position (000) immediately before, during and for a minimum of a few microseconds after each horizontal sync pulse. This gives the set a chance to lock and hold onto the reference color burst.

The chrominance output from the data selector should be disabled for the duration of the sync pulses and any time a white screen display is wanted. The output chrominance signal is RC filtered to make it somewhat sinusoidal. It’s then cut down in amplitude to around one-quarter the maximum video white level and is capacitively coupled to the 100 Ohm video output of Fig. 2 or otherwise summed into the video or rf modulator circuitry. For truly dramatic color effects, the amplitude and delay of the chrominance signal can be changed in a more complex version of the same circuit.

More information useful in solving television interface appears in the Television Engineering Handbook, by Donald Fink, and in various issues of the IEEE Transactions on Consumer Electronics.

Fig. 21. Color subcarrier generator. Hex buffer used as delay line. Use supply voltage variations on 4049 to trim colors.