Cromemco

16KZ RAM

Instruction Manual

five dollars

Cromemco

16KZ RAM

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Introduction

The Cromemco 16KZ is a high-speed 16K RAM card designed for the S-100 microcomputer bus. The 16KZ can operate at 2MHz or 4 MHz system clock rates with no wait states whatsoever. A special Bank Select feature is incorporated on the 16KZ that allows memory space to be organized into as many as 8 banks of 64K each. The memory banks in which the 16KZ resides are selected by switches on each 16KZ card; the active banks of memory are selected under software control. The 16KZ also contains Direct Memory Access Override Circuitry that allows any DMA device to access different banks of memory during DMA operations than otherwise.

With its high-speed capability and memory bank expandability, the Cromemco 16KZ is designed to be a card of lasting value. It is particularly well-suited for use with the Cromemco line of S-100 bus computer equipment. It is also compatible with other S-100 bus computers including the Altair 8800 and the Imsai 8080.

Initial Switch and Jumper Setup

Logical Address Block Select

The 16KZ RAM board may be located in any one of four 16K blocks of memory space. The Block Select switches, labeled A14 and A15, are part of a 4-place DIP switch located in the upper middle of the card. These switches control address bits A14 and A15 respectively. Setting a switch to the UP position enables the card to respond to a high logic level in that address bit. Table I below summarizes the switch settings for each block.

Origin Address	End Address	A15	A14
0	3FFF	0	0
4000	7FFF	0	1
8000	BFFF	1	0
C000	FFFF	1	1

Table I

Memory Bank Mapping Select

With the unique, software-controllable Cromemco Memory Bank Select feature, the 16KZ card may be mapped to any combination of 8 levels of 64K memory space. The 8-place DIP switch in the upper middle of the card controls bank selection. A switch in the UP position assigns the card to the specific memory bank.

On power-up the active memory bank is Bank 0. Only memory boards mapped to this bank are immediately active after power-up. At this point, any bank or banks may be enabled under software control, by addressing I/O port 40H dedicated to this function. The 8 bits output from port 40H enable or disable the corresponding bank(s) in memory. A set bit "1" in the corresponding bit position will enable the memory bank. A reset bit "0" will disable it. A light emitting diode (D1) is used to indicate when the memory board is enabled.

Direct Memory Access Overide

The 16KZ RAM card also features Cromemco Direct Memory Access Override, a powerful hardware feature which allows memory blocks residing in different memory banks, with identical or overlapping addresses, to be accessible to DMA transfer.

Switches 3 and 4 in the 4-place DIP switch at the middle top of the card control this function.

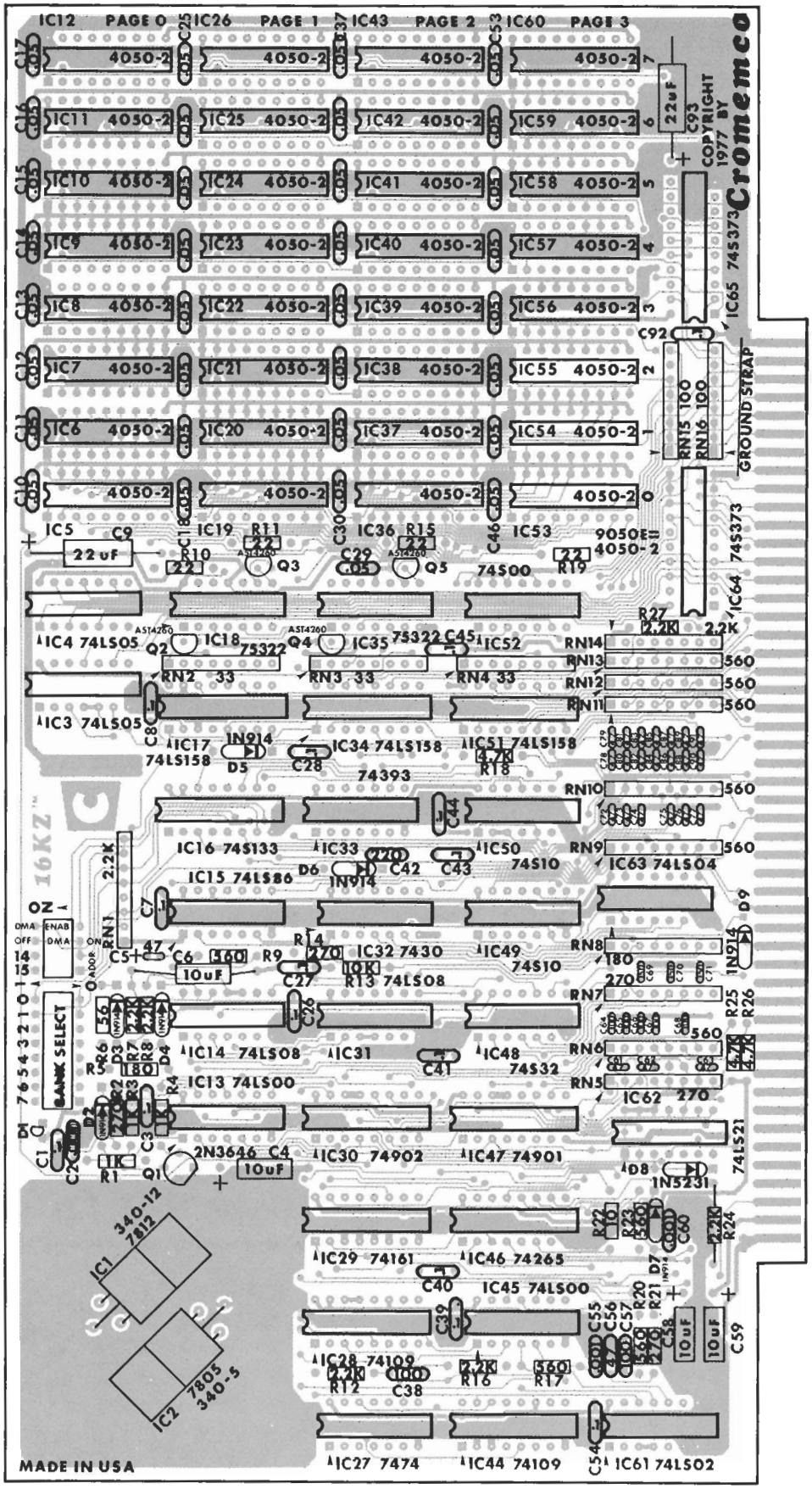
Switch 4, when in the UP position, enables the DMA override for the entire block. When DOWN, the DMA override is disabled. Switch 3, when in the UP position, locks out the block of memory during DMA transfer. When in the DOWN position, the memory is accessible to DMA regardless of whether or not it resides in the currently active memory bank. The setting of Swtich 3 is only relevant if Switch 4 is UP and then only during DMA operations. Normally both Switch 3 and Switch 4 and left in the DOWN position.

Assembly Information

Assembly Instruction

If you purchased your 16KZ memory card as a kit you will find construction to be straightforward. Be sure to use a fine-tipped, low wattage soldering iron

Parts Placement Diagram



for the assembly. Only rosin multi-core solder should be used. When soldering, be sure to heat each solder joint until the solder flows freely.

As each component is inserted into the board, it should be soldered in place. Take special care to observe the orientation of polarized components including the tantalum capacitors, diodes, resistor networks, and transistors. The location of all parts on the printed circuit card is shown in the Parts Placement Diagram.

Take special note that IC1 and IC2, although they may look physically similar, are *not* interchangeable. IC1 is a 12-volt regulator while IC2 is a 5-volt regulator.

For the ground strap shown on the Parts Placement Diagram use a small length of insulated solid AWG 24 wire as a jumper between the two ground pads shown.

Initial Checkout

After soldering all components in place but *before* inserting the ICs into their sockets, insert the 16KZ card into your computer and use a voltmeter to verify that all power supply voltages are properly regulated. The positive terminal of C9 should measure +12 volts. The positive terminal of C4 should measure +5 volts. The anode of diode D8 should measure -5 volts.

If all voltages check out properly, proceed to insert the ICs into their sockets. Take care to note the orientation of pin 1 of each IC. Make certain that every pin of every IC is properly engaged in its socket. THE SINGLE MOST COMMON ASSEMBLY ERROR IS A BENT IC PIN NOT ENGAGED IN THE IC SOCKET.

Your 16KZ memory card is now ready for final check-out and burn-in. Set address switches A15 and A14 for the desired memory address. Make certain that the BANK 0 switch is up so that the 16KZ card will be enabled on power-up.

Final Checkout and Burn-in

Final checkout is performed using the Cromemco 16KZ memory test described later in this manual. This is a very thorough test that will quickly isolate any problems with your 16KZ memory card.

To assure that your memory card will retain long-term reliability, we recommend that the 16KZ memory test be run for one week with your 16KZ card in a 55°C temperature ambient. Any memory chip failing this test should be replaced. To fully stress your 16KZ card, this test should use a Cromemco ZPU card running at full 4MHz speed with no wait states.

Theory of Operation

Bank Select Logic

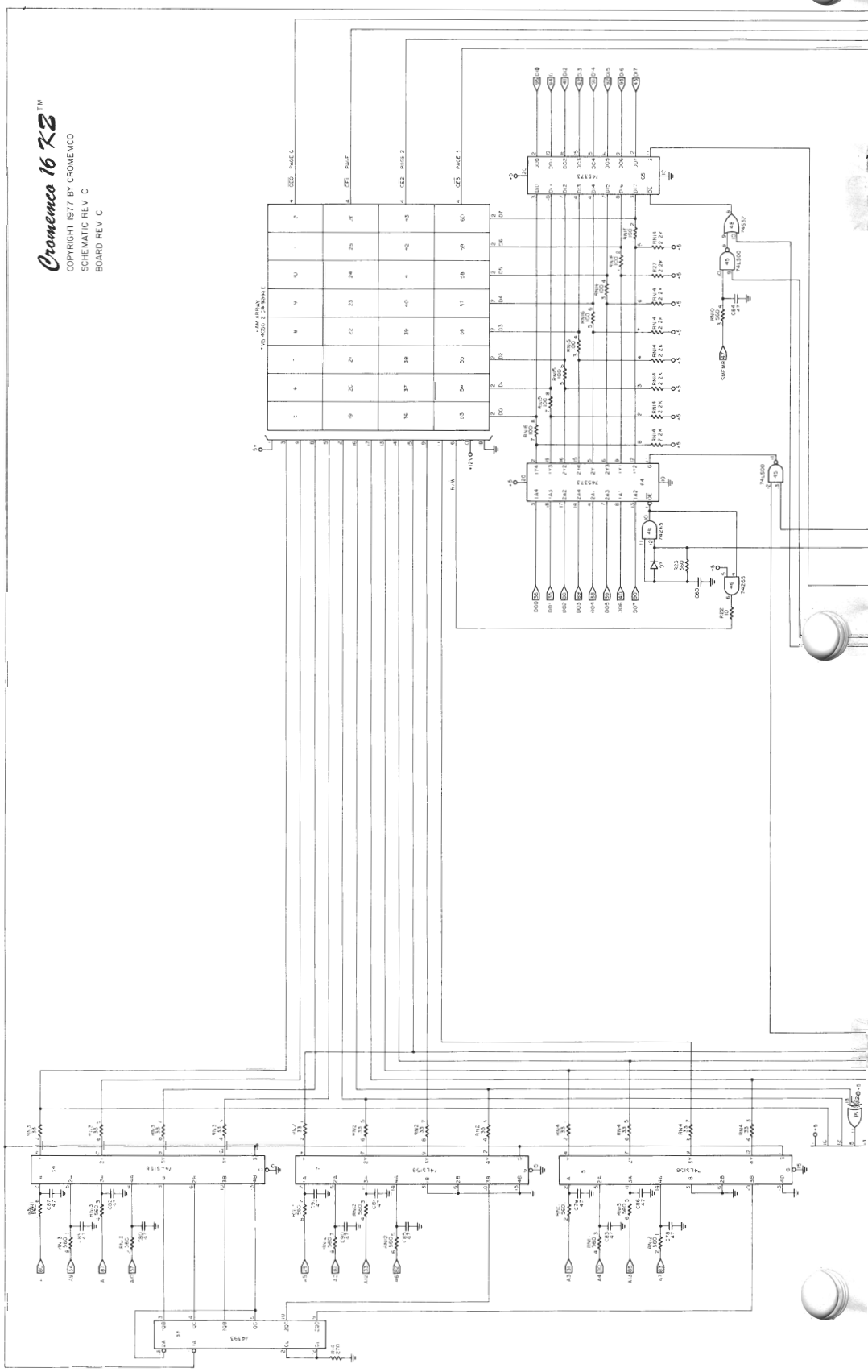
The bank select logic circuit decodes commands sent to output port 40H by the CPU to determine if the memory bank in question should be active. If the CPU sends a logic one to any bit position for which the bank select switch is ON, the board will be enabled. Otherwise, the board will disable. IC16 decodes the combination for SOUT, $\overline{PWR}$, and address 40H and sends a clock pulse to the bank select circuitry. The combination of open collector inverters IC3 and 4 does an AND-OR operation to detect the correct bank state. IC28 stores the current bank status, sends it to the LED D1 for indication, and controls the board enable gate IC32. The AND gates IC31 in combination with some discrete components cause the bank Ø switch setting to control the board status whenever $\overline{PRESET}$ and $\overline{POC}$ are pulsed. Thus the bank Ø switch determines the state the board comes up in whenever a RESET occurs.

Direct Memory Access Overide

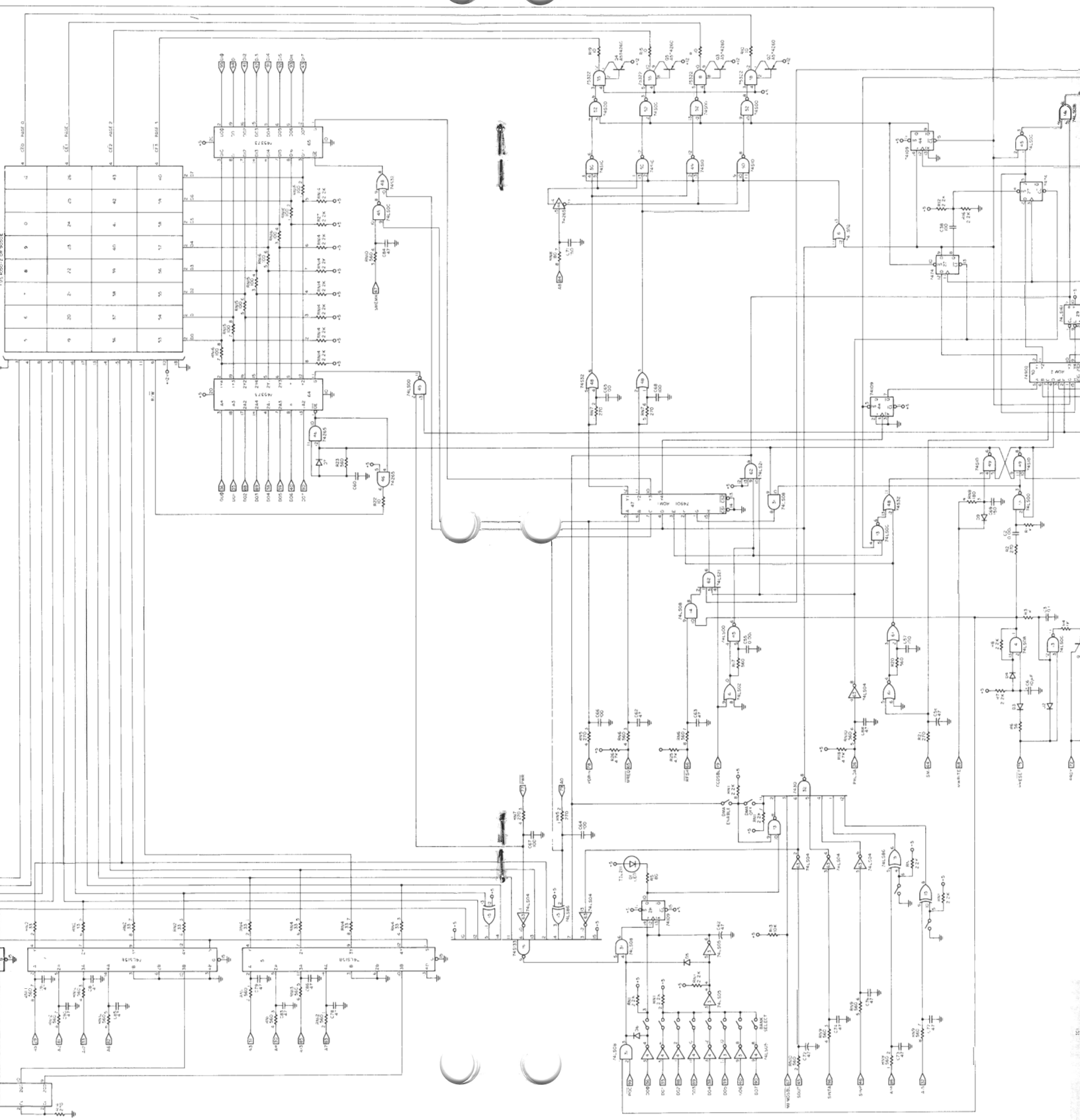
IC13 in conjunction with the DMA ENABLE and DMA OFF switches allows DMA operations to override the current bank selection if desired. If the DMA ENABLE switch is open (i.e. away from the top card edge), then the current bank select FF state governs the board state during DMA operations. In this case, the DMA OFF switch has no effect. If the DMA ENABLE switch is closed (i.e. towards the top card edge), then the DMA OFF switch determines whether the board is enabled during DMA operations. If the DMA OFF switch is open (away from the top card edge), then the memory card is enabled for DMA operations when addressed. If the DMA OFF switch is closed (towards the top card edge), the memory card is unconditionally disabled during all DMA operations.

Proper use of the DMA ENABLE and DMA OFF switches will permit DMA devices, such as video graphic display generators, to remain "in contact" with their own dedicated memory area regardless of the current memory bank selection. This prevents loss of the image when banks are switched. Of course, all memory cards in an address range where bank switching is used in conjunction with DNA ENABLE must have the DMA ENABLE switching capability to prevent bus conflicts.

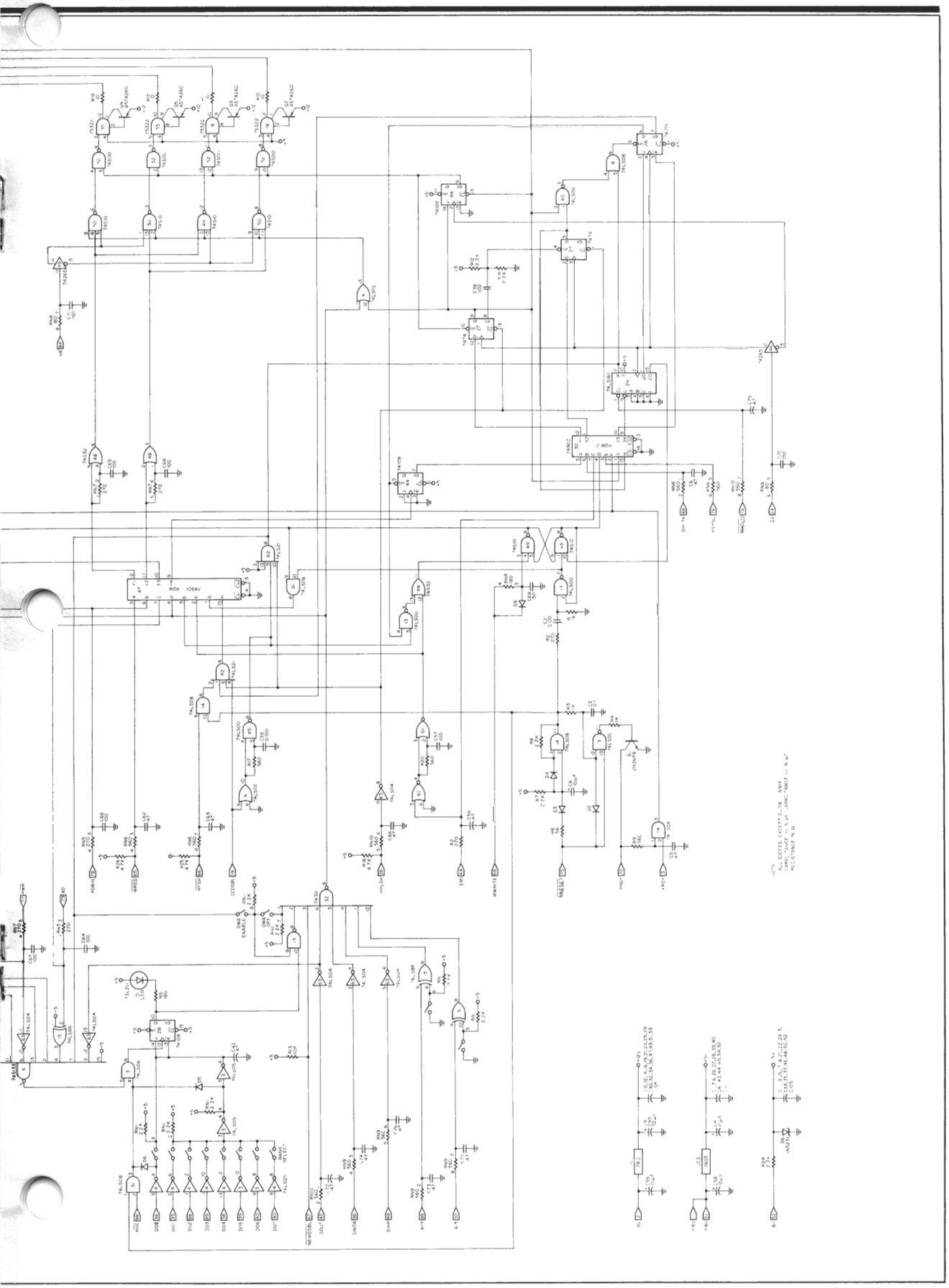
Schematic


Cromemco 16 K2™
COPYRIGHT 1977 BY CROMEMCO
SCHEMATIC REV C
BOARD REV C

Schematic Diagram



Diagram



Board Enable Decode

The overall board status is decoded by IC32. Address selection uses exclusive-OR logic gates in conjunction with two dip switch sections to select the 16K address block for which the board is active. If any of the status lines SINP, SOUT, or SINTA goes high, the board is disabled. Also, any device pulling the $\overline{\text{MDSBL}}$ bus line (pin 67) low will disable the memory board. This permits a ROM bootstrap to overlap the memory area if desired. If the bank select and other conditions are met, then the output of IC32 goes low to enable the 16KZ to perform memory cycles.

Chip Enable Generation

The 16KZ uses a direct read process for generation of the RAM chip enable signals. In general, whenever the address and other conditions are correct for addressing a particular RAM, the chip enable (CE) input will go high (+12V) if a memory cycle request occurs. This is when either MWRITE, PDBIN, or SM1 go high, or $\overline{\text{MREQ}}$ goes low. Since the bus signals are used directly to control the CE generation, all devices sending memory cycle signals on the bus *must* use a format similar to the 8080 and send only signals for complete memory cycles. Short pulses or address changes while CE is high will usually cause the RAM area addressed to fail to restore the data after reading it out. The data then changes state and is lost. Direct read operation was chosen to permit the shortest possible memory access operation and thereby allow operation at 4MHz with the Cromemco ZPU without wait states.

Decoding of the bus signal combinations giving valid CE operation occurs in IC47. Address line AØ determines whether the CE pulse will occur on pin 12 (AØ=0) or pin 11 (AØ=1). During CPU operations, CE pulse outputs can occur only if the address enable input is low and the gating pulse input H is high. During DMA operation the gating input H is held low. In general, gating input H is used to turn off the CE pulse whenever conditions requiring it occur. IC62 combines a number of these inhibiting conditions to produce the CE gating pulse. The signals of primary importance during CPU operation are the $\overline{\text{RFSH}}$ bus signal on pin 66, and the gating FF output from IC28 pin 7. The gating FF, IC28, takes pin 7 high whenever a CE pulse is allowed. If the current CE pulse lasts more than 8 cycles of Ø2, then the QD output of IC29 goes high. This sets IC28 and its pin 7 goes low to terminate the CE pulse. This prevents the CE pulse length from exceeding the RAM specifications if the CPU enters a wait state during a memory cycle. The wait state situation occurs primarily during front panel single step and reset operations, but could come from a hardware item elsewhere. Also, if a refresh cycle begins, $\overline{\text{CCDSBL}}$ goes low, or PHLDA goes high, IC 28 goes low to prevent CE pulses from IC47. When normal CPU operation resumes, a logic low level output from IC30 pin 10 causes IC28 to take pin 7 high again.

Chip Enable Control Logic

The chip enable pulses from IC47 go first through IC48, which stretches the trailing edges to eliminate any low going glitches which may be generated in IC47. The CE signals then go to IC49 and IC50 for selection of the block of 4K bytes to be accessed. The NOR gate IC61 turns off the CE pulse when the board is unaddressed or during a refresh cycle. IC52 inserts the refresh pulse, and IC18 and IC35 amplify the TTL signal to logic levels of 0 and +12V for the RAMs. The 75332's employ an external PNP transistor to pull their outputs up to +12V.

The CE generation and control logic divides the RAM array into 4K blocks depending on the states of AØ and A8. This permits fast DMA devices such as the Cromemco Dazzler interface to use ripple addressing with either AØ or A8 as the most rapidly changing address. Minimum access times result, with the read process occurring in a manner similar to static RAMs. In order to use this mode, all addresses and control lines must change at the same time.

RAM Array

The RAM array consists of 4 blocks or rows of 4K x 1 RAM chips, with like bit positions bussed together. All the similar address and control lines are tied together, with the CE pulse determining which row responds. Address data comes from multiplexers IC19, IC36, and IC53. These determine whether the RAMs use the CPU bus or the refresh counter for addressing. During write operations, IC64 transmits data from the CPU DO bus to the RAM chip data pins. The 3 state output of IC64 turns ON whenever an MWRITE pulse occurs. A stretching network with IC46 prolongs the MWRITE pulse trailing edge to allow for propagation delays through the CE logic. Data entry into IC64 is enabled whenever either $\overline{\text{PWR}}$ or PRDY are low. This allows the memory write cycle to complete after the CPU changes DO for the next advanced status.

Data read out of the RAM array is latched into IC65. Thus it is available to the CPU and front panel after the memory completes its cycle. PDBIN,

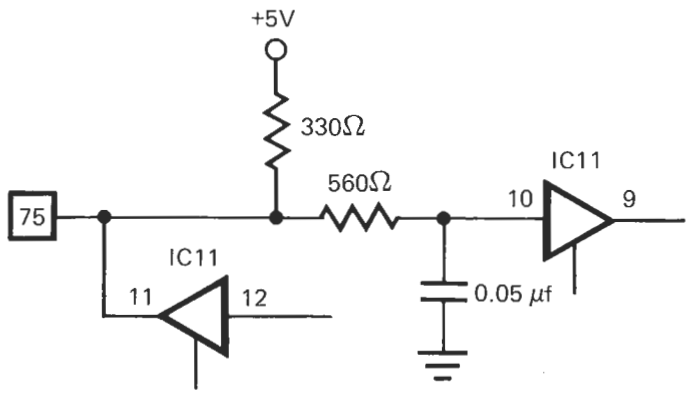
SMEMR, and board enable control gating of the data onto the DI bus. The latch enable signal comes from IC47 and goes high whenever the RAM array is read or written for data.

Refresh Cycle Generator

This memory board uses an M1 refresh state process. Advantage is taken of the fact that 8080 and Z80 CPU's use at least 4 clock cycles for their M1 states to fetch and decode instructions. The normal data fetch occurs during the first 2 clock cycles, and then memory refresh occurs during the 3rd and 4th clock cycles of M1. When a coincidence of SM1.PSYNC=1 occurs at a Ø2 positive going edge, IC27 pin 5 goes high to note this. One Ø2 cycle later, IC27 pin 9 goes high to begin a refresh sequence. During refresh, IC61 turns off any CE signals from IC47. At the first Ø2 negative going edge after refresh begins, IC44 pin 9 goes low to turn ON the CE's for all RAM's and refresh their data. One Ø2 cycle later, IC44 turns OFF, completing the refresh and incrementing the refresh address counter IC33. IC29 then turns OFF and returns the RAM to CPU control. If the RAM is used with a Z80, IC14 uses the $\overline{\text{RFSH}}$ signal to prevent action by the CPU refresh pulse on $\overline{\text{MREQ}}$. Otherwise, some wait state conditions may cause the generation of CE glitches. When the refresh cycle begins, IC45 causes IC28 pin 7 to go low. It stays this way until the trailing edge of SM1 clocks IC44 pin 4, which causes IC30 to make IC28 pin 7 high again. IC44 clocks at the trailing edge of SM1 and PHLDA and the leading edges of MWRITE. During times when CPU operation is suspended, IC30 pin 9 goes high, causing IC29 to count. After 8 cycles of Ø2, the CE outputs of IC47 are disabled. After 16 cycles of Ø2, the CE outputs of IC47 are disabled. After 16 cycles of Ø2, IC29 pin 15 goes high, causing autonomous memory refresh cycles. These refresh cycles continue to occur once per 16 Ø2 cycles until CPU operation resumes. Two sections of IC49 arbitrate between MWRITE and refresh pulses to prevent CE conflicts during front panel write operations with the CPU stopped.

Reset Circuitry

The reset circuitry takes care of the special CE management problems that occur with dynamic memories using a direct read process. When the $\overline{\text{PRESET}}$ line goes low, IC13 and Q5 immediately pull down the PRDY line. This causes the CPU to halt during execution of the current memory cycle. The memory board then times out eight Ø2 cycles and IC28 pin 7 turns off the CE pulse. The CPU board *must have* a 10 μsec delay network in series with its $\overline{\text{PRESET}}$ input. The current revision Cromemco ZPU card does have such a delay network, but older ZPU cards may need modification. In particular ZPU REV A and ZPU REV B must have an RC network inserted in series with the reset line as shown in the schematic diagram below:



Provision of a 10 μsec delay permits the memory board to turn off before the CPU terminates the current operation.

When the $\overline{\text{PRESET}}$ line is released, IC14 produces a delay of about 50 msec to allow for multiple switch bouncing. At the end of this time, IC13 and IC31 cause the data at memory location Ø to be read into the data latch IC65. After another 50 μsec, IC13 and Q5 release the PRDY line, allowing CPU operation to resume if in the run state. This procedure prevents the occurrence of partial memory cycles and resulting data loss caused by the reset switch bouncing.

Memory Test

Every Cromemco 16KZ RAM card is provided with a paper tape listing of the 16KZ Memory Test program. The 16KZ Memory Test loads and executes at any address except ØIØIH through ØFFFH. It requires at least 4K of RAM addressed at Ø and situated in all eight banks. (Set the address DIP switches of the Cromemco 4KZ or 16KZ to Ø and raise all eight of the bank-select DIP switches.)

In particular, it can be stored and executed in a pair of 2708 PROMs at any address in upper memory. The program is compatible with either the Z80 or the 8080 instruction set.

The Memory Test can check 16KZ cards at any address except Ø and in any bank. It includes five different tests.

The Peak test shifts a one in a field of zeroes through the card. It loads a byte with one bit high into the top location of the card. The next location gets the byte shifted left, say. After the 1 is shifted into the carry flag, the shift direction is reversed. Each byte is checked after it is written and again after the entire card is loaded. The test is repeated for each of the 18 possible ways of loading such a pattern.

The Valley test is like the Peak test except that it uses a zero in a field of ones.

The Delay test checks long-term memory retention. The card is filled with a pattern and then tested to see if it can retain the pattern for at least 6 seconds (at 4 MHz). The test is repeated for each of several patterns.

The MI test checks the capability of the card to be read during MI machine cycles.

The Bank test determines in which banks the card appears.

Using the Test

The Memory Test checks 16KZ cards addressed at 4, 8 or C (i.e. 4000H, 8000 or C000H).

Assume that the Memory Test resides at 1000H and that we wish to check cards at 8 and C in bank Ø and at 4, 8 and C in bank 7.

Make sure that there is RAM at Ø in all banks. Execute 1000H. When prompted by 'BANK: ' type the bank number followed by a space. After the prompt 'CARDS: ' type the card numbers separated by spaces. The last card number should be followed by a carriage-return. The prompt 'BANK: ' will again be issued. If no further cards are to be tested type a carriage-return.

```
BANK: Ø CARDS: 8 C (CR)
BANK: 7 CARDS: 4 8 C (CR)
BANK: (CR)
```

If an entry error is made, a '?' will be printed, the card queue cleared and prompts mode to begin again.

Testing of the cards continues until either the ESCAPE key or CONTROL-'Q' is depressed. (See Control Functions.)

Error Print-out

If any errors occur in the Peak, Valley or Delay test, an image of the card will be printed indicating the physical locations of the RAMs in which the errors occurred. In the following example errors occurred in bits 1 and 3 of rows 1 and 2, respectively, of card C in bank 7.

```
(CARD C)   -Ø-  -1-  -2-  -3-  -4-  -5-  -6-  -7-
(BANK 7) Ø: ...  ...  ...  ...  ...  ...  ...  ...
         1: ...  PVD  ...  ...  ...  ...  ...  ...
         2: ...  ...  ...  PVD  ...  ...  ...  ...
         3: ...  ...  ...  ...  ...  ...  ...  ...
```

The MI test and the Bank test are only made if there are no errors in the first three tests.

Control Functions

Pushing CONTROL – 'P' causes a print-out of the image of the card currently under test. After print-out the test resumes at the point it was interrupted.

CONTROL – 'E' causes a listing of all the cards in which errors have occurred. The test then resumes at the point it was interrupted.

ESCAPE or ALT MODE causes a print-out of the current card image followed by termination of the test and prompting for a new test.

CONTROL – 'S' causes the remainder of a print-out to be skipped. The test then resumes as if the print-out had been finished.

CONTROL – 'Q' causes the Memory Test to be quit. Transfer to the warm-start entry point (E008) of the Z80 Monitor is made.

Loading the Paper Tape

The memory test program assumes that data transfer occurs on I/O port 1. Status flags are on input port Ø. The data-available flag is on bit 6 of input port Ø. The transmitter-buffer-empty flag is on bit 7 of input port Ø. Both flags are active high.

The following program can be used to load the binary paper tape of the memory test program into RAM at location Ø.

```
1ØØØ    21 ØØ ØØ          LD HL, Ø
1ØØ3    DB ØØ ØØ    LOOP: IN A, Ø
        E6 4Ø               AND 4ØH
        CA Ø3 1Ø            JP Z, LOOP
        DB Ø1               IN A, 1
        77                  LD(HL), A
        23                  INC HL
        C3 Ø3 1Ø            JP LOOP
```

The tape can also be loaded with the Cromemco Z80 Monitor by typing R Ø 6ØØ (CR)

Parts List

CAPACITORS

C	1	.1 Disc
	2	.001 Disc
	3	.1 Disc
	4	10 UF Tant
	5	47 Pf Mono
	6	10 UF Tant
	7	.1 Disc
	8	.1 Disc
	9	22 UF Tant
	10-25	.05 Disc
	26-28	.1 Disc
	29-37	.05 Disc
	38	100 Pf Disc
	39-41	.1 Disc
	42	220 Pf Disc
	43-45	.1 Disc
	46-53	.05 Disc
	54	.1 Disc
	55	.001 Disc
	56	47 Pf Disc
	57	100 Pf Disc
	58	10 UF Tant
	60	.001UF Disc
	61-63	47 Pf Mono
	64-68	100 Pf Mono
	69-71	150 Pf Mono
	72-91	47 Pf Mono
	92	.1 Disc
	93	22 UF Tant
	59	6.8UF@35V

SOCKETS

32	18 Pin
2	20 Pin
10	16 Pin
19	14 Pin

MISC

1	8 Pole Dip Switch
1	4 Pole Dip Switch
1	Heatsink
4	6-32 Pan Head Screws
4	6-32 Hex Nuts
1	PC Board
1	Paper tape listing of memory test program
1	16 KZ instruction manual

DIODES

D1	LED, TIL-211
D2-D7	IN914/IN4148
D8	IN5231
D9	IN914/IN4148

TRANSISTORS

1	2N3646
4	A5T4260

IC	1	7812/340-12
	2	7805/340-5
	3	74LS05
	4	74LS05
	5-12	TMS4050-2/9050E
	13	74LS00
	14	74LS08
	15	74LS86
	16	74S133
	17	74LS158
	18	75322
	19-26	TMS4050-2/9050E
	27	7474
	28	74109
	29	74161
	30	74902 ROM2
	31	74LS08
	32	7430
	33	74393
	34	74LS158
	35	75322
	36-43	TMS4050-2/9050E
	44	74109
	45	74LS00
	46	74265
	47	74901 ROM1
	48	74S32
	49-50	74S10
	51	74LS158
	52	74S00
	53-60	TMS4050-2/9050E
	61	74LS02
	62	74LS21
	63	74LS04
	64-65	74S373

RESISTOR NETWORKS

RN1	2.2K, Sip, 7 Resistors, 8 Pin, P/N 003-00008
RN2,3,4	33 , Sip, 4 Resistors, 8 Pin, P/N 003-00000
RN5	270 , Sip, 4 Resistors, 8 Pin, P/N 003-00003
RN6	560 , Sip, 4 Resistors, 8 Pin, P/N 003-00006
RN7	270 , Sip, 4 Resistors, 8 Pin, P/N 003-00003
RN8	180 , Sip, 4 Resistors, 8 Pin, P/N 003-00002
RN9-13	560 , Sip, 4 Resistors, 8 Pin, P/N 003-00006
RN14	2.2K, Sip, 7 Resistors, 8 Pin, P/N 003-00008
RN15-16	100 , Sip, 4 Resistors, 8 Pin, P/N 003-00001

RESISTORS

R1	1K	R10	22	R19	22
2	270	11	22	20	560
3	1K	12	2.2K	21	270
4	1K	13	10K	22	10
5	180	14	270	23	560
6	56	15	22	24	2.2K
7	2.2K	16	2.2K	25	4.7K
8	2.2K	17	560	26	4.7K
9	560	18	4.7K	27	2.2K

Warranty

Your factory-built 16KZ 4 MHz RAM card is warranted against defects in materials and workmanship for a period of 90 days from the day of delivery. We will repair or replace products that prove to be defective during the warranty period provided that they are returned to Cromemco. No other warranty is expressed or implied. We are not liable for consequential damages.

Should your factory-built 16KZ 4 MHz RAM card fail after the warranty period it will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any product that in our opinion has been subject to abnormal electrical or mechanical abuse. The service fee is currently $70 and is subject to change.

Your assembled 16 KZ 4 MHz RAM card kit will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any kit that in our opinion has not been assembled in a workmanlike manner or has been subject to abnormal electrical or mechanical abuse. Payment of the service fee must accompany the returned merchandise. The service fee is currently $70 and is subject to change.