wynchester

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Introduction

Appendix

INTRODUCTION

WYNCHESTER SYSTEMS AND ELECTRONICS INC. is the designer and manufacturer
of the W7993 series of small computer systems. Using stable design concepts
the products offer a low cost vehicle for systems houses that develop
custom programs for either straight line applications or specific end users.
The W7993 uses industry standards both in the architecture and the operating
system and therefor is compatible with the majority of similar systems on
the market. Compatibility is important in both hardware and software in
the fast moving micro computer environment, allowing full advantage to be
taken of new devices and methods that are continually being offered both by
the semiconductor manufacturers and the many software houses.

In the competitive environment of small computers, the W7993 represents the
best price performance of any system on the market today.

SPECIFICATION

W7993-725 - TERMINAL

W7993-725
TERMINAL

Installation

The 725 should be positioned on a steady surface at a comfortable level for the user. A space of at least three inches should be provided at the rear of the 725 to provide ease of access to the power switch and brightness control. Care should be taken to keep the ventillation holes on the top rear and underside from becoming blocked. The line cord should be plugged into a three pin grounded outlet.

The 725 power switch (located on the rear) should illuminate when turned on. After a one minute warm-up period the monitor should display a block cursor in the upper left corner of the screen. This position will be referred to as the HOME or HOME-UP position throughout this manual. If the cursor does not appear in the home position of an otherwise clear screen, depress the [CLEAR] Key. If the cursor still does not appear, refer to Section 8 of this manual.

Depress the [LINE/LOCAL] key on the keyboard. Type on the keyboard. Characters will appear corresponding to the keys you strike and the cursor will advance to indicate the next position into which a character will be written.

Adjust the brightness control on the rear of the 725 cabinet for suitable viewing while maintaining a black background. Excessive brightness can cause premature phosphor degradation or "burning" not covered under the CRT warranty. When leaving displayed data on the screen for extended periods of time (overnite for example), reducing the brightness will prolong the CRT lifetime.

1.1 Using the 725 Operation Manual

All the information necessary to realize the full potential of this product is contained in this operating manual. We strongly urge you to read the manual thoroughly before you use the terminal.

Section 2: describes the various emulations available.

Section 3: details the operation of the keyboard and describes the operation of all function keys as well as the numeric cluster.

Section 4: lists the features offered by the 725 and describes each feature in alphabetical order. Should you encounter problems when attempting to use a particular feature of the 725 you may refer to its description in Section 4 for clarification.

Section 5: describes the Input/Output and Auxilliary interfaces. Information contained in this section is useful to insure compatibility between the 725 and your host computer.

Section 6: explains the user selectable options which include: terminal
emulation, ADM 3A wrap or no wrap, and video attribute selection.
Instructions are provided for changing these options to meet your
specific tastes or application.

Section 7: contains the Appendices which include the following useful
information, a complete list of available features in each of
the three terminal emulation modes; tables for use with the
cursor positioning features; a complete list of the ASCII codes
including their Hexidecimal, Octal, Binary and Decimal equivalents.

2.0 Operating Modes

For efficient communications, the Local mode with associated editing features may be utilized to minimize use of costly host CPU time or to minimize the number of packets transmitted in a pay-by-the-packet system. The Local mode can also be used for testing and studying the operation of various terminal features.

2.1 Terminal Emulation Selection

The 725 may be commanded to emulate one of three terminals: The Lear Seigler ADM 3A, Hazeltine 1400, or 725. Mode switches 1 and 2 (T.0.1 and T.0.2) select the terminal to be emulated as follows:

T.0.1	T.0.2	Emulation
OFF	OFF	725 WRAP*
OFF	ON	1410 WRAP*
ON	OFF	ADM 3A NO WRAP
ON	ON	ADM 3A WRAP*

Wrap/No Wrap refers to the action taken when the last position on the line is filled with a displayable character. To wrap is to proceed filling the next line; to not wrap is to leave the cursor in the last column and "overprint" characters.

2.2 Local Self Test

The LOCAL mode also provides a means of testing the terminal manually. If the terminal works in the LOCAL mode, any problems are limited to either the 725 interface, the communication link between the 725 and the host computer, or the host computer.
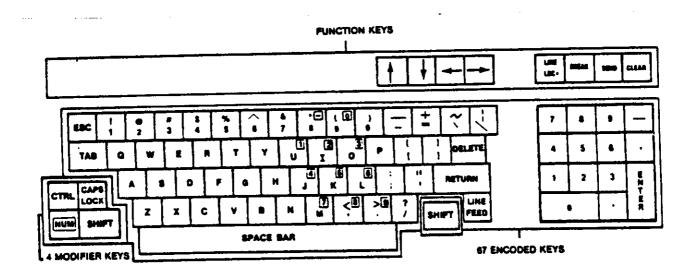
2.3 Transparency Mode

A very useful feature of the 725 is its capability to display a unique symbol for each of the ASCII control codes when in the Display Control Code mode. This mode can be entered and exited only by depressing the [CTRL] and [Q] keys simultaneously while in the LOCAL mode. This aids both the receive and transmit operations. On the receive side it permits one to identify every character received by the terminal settling any format problems caused by otherwise unseen control characters. On the transmit side it allows control characters to be imbedded in the displayed data for transmission in block mode to the computer or printer.

3.0 Keyboard

The 725 keyboard contains 80 keys which may be classified as either encoded, modifier, or function keys (see Figure 3.1 below).

The keyboard features typamatic (Auto-Repeat) operation at a rate of 30 characters per second (CPS) after a one second delay.
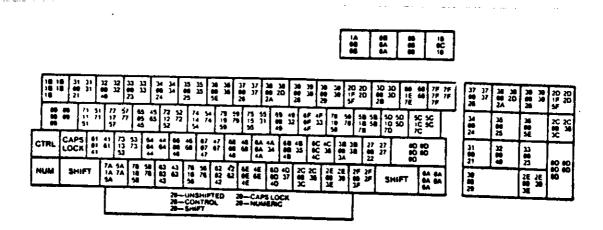

FUNCTION KEYS

4 MODIFIER KEYS   67 ENCODED KEYS

3.1 Encoded and Modifier Keys

The majority of keys on the keyboard generate an output code when struck. The assignment of output codes to keys is illustrated in Figures 3.1 and 3.2. Note that the output codes generated by the encoded keys depend on the state of the four modifier keys-[CAPS/LOCK], [CTRL], [NUM], and [SHIFT]. The modifier keys do not generate output codes when they are depressed.

NOTE: The encoded key [ESC] and the modifier key [CTRL] have special significance to 725 and appear frequently in this manual in conjunction with another key e.g. [ESC] [H], [CRTL] [G].   The

[ESC] key (because it is an encoded key), should be depressed and released before striking the [H] key in the above example but the [CTRL] key (because it is a modifier key) must be depressed and held down while simultaneously striking the [G] key and released after the [G] key is released.

Figure 3.2 Keyboard Output Codes

3.2 Function Keys

The top row of eight keys on the 725 keyboard may generate output codes but are primarily used to control various functions. These functions are described below.

3.2.1 [Line/Loc.] Key

This key controls whether the 725 is in the ON-LINE OR LOCAL mode. When ON-LINE (key up) , all codes generated by the encoded key are transmitted out the I/O and AUX ports is accepted and displayed. When in the LOCAL mode (key down), all codes generated by the encoded keys are "echoed" to the screen and are not transmitted out either the I/O or AUX ports. Data may be sent out these ports when in the LOCAL mode by invoking a SEND command as described in Section 3.2.5 below.

2.2.2 Cursor Control Keys

In LOCAL mode, these keys move the cursor in the indicated direction without transmitting any codes to the host. These keys peg the cursor at the screen boundaries.

In the ON LINE mode, each cursor control key transmits a unique sequence of codes dependent upon the emulation status of the terminal. The following table lists the cursor control key output codes for the various emulation modes.

Key	725	ADM 3A	H1410
UP	CTRL Z	CTRL K	CTRL K
DOWN	CTRL K	CTRL J	CTRL J
LEFT	CTRL H	CTRL H	CTRL H
RIGHT	CTRL X	CTRL L	CTRL P

NOTE: There are two differences between the Hazeltine 1410 cursor movement and the 725 emulation: the cursor up function has been added to the 725; when moving left and right the cursor does not wrap to the previous or next lines as on the 1410.

3.2.3 Break Key

This key forces the serial output to assume the space (logical 0) state for as long as it is depressed.

3.2.4 Clear Key

Depressing the clear key causes the 725 to clear the screen and to read the setting of the MODE SELECT switches described in Section 2.1 above.

3.2.5 Send Key

This key commands the 725 to transmit the contents of its screen out pin 2 of its I/O and AUX communication ports.

NOTE: While sending the 725 ignores characters received from the host computer. When in the LOCAL mode if no data is being sent to the computer in the block transmission mode the 725 will accept and process data from the host. This allows the user to edit the data on the screen, send it and receive a response from the host without changing the position of the [LINE/LOC.] keyswitch. It also insures that any messages from the computer are not lost while in the LOCAL mode.

3.2.6 Delete Key

When this key is pressed in the local mode, the character immediately to the left of the cursor is erased from the screen. When struck in the on-line mode, the code [7F] is transmitted.

3.3 Numeric Data Entry

There are three methods provided by the 725 keyboard for facilitating the entry of numeric data. These are: typewriter style – the numbers 1 through 9 and 0 appear in the top row of the main keyboard just as on a modern typewriter; calculator style – a 14 key calculator format numeric pad is provided for accounting type data entry; keypunch style – when the [NUM] key is depressed, a numeric key cluster identical to the IBM Model 29 keypunch format is available inlaid in the main keypad. This feature is especially attractive to keypunch operators since they need not sacrifice their speed learning the calculator format. To disable the [NUM] key, it should be pressed again and it will disengage.

NOTE: When the [NUM] key is down and the [8] key is depressed in the 14 key numeric pad, the code for a - will be generated. Similarly, if the [9] key is struck in the 14 numeric pad and the [NUM] key is down, the code for a 0 will be generated. This is due to the fact that the 14 keys in the numeric pad are functionally indistinguishable from 14 keys in the main keypad. The pairing of numeric pad keys and main pad keys is:

Numeric Pad Key	Same as	Main Pad Key
[0]		[)/0]
[1]		[!/1]
[2]		[@/2]
[3]		[#/3]
[4]		[$/4]
[5]		[%/5]
[6]		[¢/6]
[7]		[&/7]
[8]		[*/8-]
[9]		[(/90]
[.]		[/.9]
[,]		[/,8]
[-]		[-/-]
[ENTER]		[RETURN]

4.0 <u>Response To Control Codes and Escape Sequences</u>

Numbers shown in braces (e.g (07)) represent the Hexadecimal equivalent
of the associated ASCII code.

The symbol N/A is used to indicate that the feature is not available
in the selected emulation mode.

The Lead-In character for the Hazeltine 1410 mode may be either an
ESCAPE (7F) or TILDE (7E). Throughout this section, the ESCAPE is
assumed as the Lead-In character.

4.1   <u>Absolute Cursor Positioning (Direct Cursor Addressing)</u>

ABSOLUTE CURSOR POSITIONING allows the user to position the cursor
anywhere within the 24 x 80 display matrix. The general format is
a lead-in code, or codes, followed by two address co-ordinates. These
co-ordinates must be transmitted to the terminal in ASCII. The cursor
assumes the new position after the co-ordinates have been given.
No other coding may be imbedded within this string of characters.

<u>NOTE</u>:   Please refer to Appendix 7.2 for the ABSOLUTE CURSOR ADDRESSING
         TABLES and Appendix 7.3 for a complete list of decimal/hex/ASCII
         conversions.

4.1.1 <u>725 Cursor Positioning</u>

To position the cursor, the ASCII code (14) must be received followed
by the appropriate line # (0-23) and the column # (0-79). If an invalid
line is received, it is reduced modulo 24 until a valid line 0-23
is produced. Similarly, an invalid column is reduced modulo 80.
The top line of the display is line, 0; the leftmost column is column 0.

<u>EXAMPLE</u>:   To position the cursor, on the tenth line down and in the
           fifth column from the left, the following codes must be
           received by the terminal.

<u>Keys</u>	[CTRL] [T]	[CTRL] [I/2]	[CTRL] [D]
<u>Codes</u>	(14)	(09)	(04)

4.1.2. ADM 3A Cursor Positioning

To position the cursor, the ASCII codes (1B) (ESC) and (3D) (=) must
be received followed by the appropriate row number ASCII codes (40) through
(77) and column number (codes (20) through (6F)).

EXAMPLE: To position the cursor on the tenth row down and in the fifth
          column from the left, the following codes must be received by the
          terminal.

Keys	[ESC]	[+/=]	[I/2]	[$/4]
Codes	(1B)	(3D)	(49)	(24)

4.1.3 Hazeltine 1410 Cursor Positioning

To position the cursor, the ASCII codes (1B) (11) must be received followed
by the appropriate column number and row number. The 80 columns range from
0 to 79, and the rows range from 0 to 23.

The column addresses are modulo (60) as follows:

Hexadecimal Address	Column (Decimal)
(0) through (4E)	0 through 78
(4F) through (5F)	79
(60) through (7F)	0 through 31

The row addresses are molulo (20) as follows:

Hexadecimal Address	Row (Decimal)
(0) through (16)	0 through 22
(17) through (1F)	23
(20) through (36)	0 through 22
(37) through (38)	23
(40) through (56)	0 through 22
(57) through (5F)	23
(60) through (76)	0 through 22
(77) through (7F)	23

4.2 Backspace

This will cause the cursor to move one character position to the left without
erasing data on the screen. When the cursor reaches to leftmost column it
will stop.

	725	ADM3A	H1410
Key(s)	[CTRL] [H] or [<-]	[CTRL] [H] or [<-]	[CTRL] [H] or [<-]
Code(s)	(08)	(08)	(08)

4.3 Bell

When the BELL code is received, an audible tone of 1760 hertz is generated for one half second. The cursor position is not affected.

	725	ADM 3A	H1410
Key(s)	[CTRL] [G]	[CTRL] [G]	[CTRL] [G]
Code(s)	(07)	(07)	(07)

4.4 Carriage Return

LOCAL: The cursor is moved to the leftmost position of the next line. If it is on the bottom line, the screen will scroll.

LINE: The cursor is moved to the leftmost position on the present line except in the H1410 mode. In the H1410 mode, a RETURN code causes a carriage return and line feed operation.

	725	ADM 3A	H1410
Key(s)	[RETURN] or [CTRL] [M/7]	[RETURN] or [CTRL] [M/7]	[RETURN] or [CTRL] [M/7]
Code(s)	(0D)	(0D)	(0D)

4.5 Cursor Down

On receipt of the CURSOR DOWN command, the cursor is moved down one line in the same column. If the cursor is on the bottom line of the screen, the position of the cursor will not change nor will the display scroll.

	725	ADM 3A	H1410
Key(s)	[CTRL] [K/5]	N/A	N/A
Code(s)	(0B)		

4.6 Cursor Right

The cursor advances one column to the right. The display is not altered. If in the last column it will not move.

	725	ADM 3A	H1410
Key(s)	[CTRL] [X] or [-]	[CTRL] [L/6] or [-]	[CTRL] [P] or [-]
Code(s)	(18)	(0C)	(10)

4.7 Cursor Up

On receipt of the CURSOR UP command, the cursor is moved up one line in the same column. If the cursor is on the top line of the screen, the position of the cursor will not change.

	725	ADM 3A	H1410
Key(s)	[CTRL] [Z] or Cursor Up	[CTRL] [K/5] or Cursor Up	[CTRL] [K/5] or Cursor Up
Code(s)	(1A)	(0B)	(0B)

4.8 Delete Character

Delete the character denoted by the cursor. All characters to the right of the cursor position are moved left by one column. The rightmost position is cleared to the video attribute of the last character on the line. Since the DELETE functions take several milliseconds to execute, it is recommended that they be used in the LOCAL mode from the keyboard. When sending the DELETE CHARACTER or DELETE LINE codes from the computer, filler codes must be used.

	725	ADM 3A	H1410
Key(s)	[CTRL] [D]	N/A	N/A
Code(s)	(04)	---	---

4.9 Delete Line

All data on the line denoted by the cursor is eliminated. Pre-existing data below the cursor is moved up one line and the bottom line is cleared to the present attribute type. When deleting lines the cursor must not be positioned in the first column. See note in DELETE CHARACTER.

	725	ADM 3A	H1410
Key(s)	[CTRL] [W]	N/A	N/A
Code(s)	(17)	---	---

4.10 Erase To End of Frame (EEOF)

All characters from the cursor position to the end of the screen are erased to spaces of the present video attribute type. The cursor position is not affected.

	725	ADM 3A	H1410
Key(s)	[CTRL] [SHIFT] [-/-1]	N/A	N/A
Code(s)	(1F)	---	---

4.11 Erase To End of Line (EEOL)

All positions from the cursor to the right margin are replaced by spaces of the present video attribute type.

	725	ADM 3A	H1410
Key(s)	[CTRL] [SHIFT] [6/⌃]	N/A	N/A
Code(s)	(1E)	---	---

4.12 Home

This function moves the cursor to the upper left corner of the screen.

	725	ADM 3A	H1410
Key(s)	[CTRL] [)/]]	[CRTL] [SHIFT] [6/⌃]	[ESC] [CTRL] [R]
Code(s)	(1D)	(1E)	(1B) (12)

4.13 Home and Clear

The screen is cleared to spaces, and the cursor is moved to the upper left hand corner of the screen.

	725	ADM 3A	H1410
Key(s)	[CTRL] [L/6]	[CTRL] [Z]	[ESC] [CTRL] [!/\]
Code(s)	(0C)	(1A)	(1B) (1C)

4.14 Insert Character(s)

Insert subsequent characters into the cursor row at the cursor position. After this command, all characters at the cursor position and to its right are moved one position to the right each time a displayable character is typed at the keyboard. To exit from this displayable mode, any control character may be typed. The 725 will act upon the control character and sound the BELL to indicate an exit from the insertion mode.

NOTE: Since INSERT functions take several milliseconds to execute it is recommended that they be used in the LOCAL mode from the keyboard. When sending the INSERT CHARACTER or INSERT LINE codes from the computer, filler codes must be used.

	725	ADM 3A	H1410
Key(s)	[CTRL] [S]	N/A	N/A
Code(s)	(13)	--	--

4.15 Insert Line(s)

This will allow a new line of text to be added between any two pre-existing lines on the screen. A blank line will be inserted on the row denoted by the cursor. All pre-existing text on the cursor row and below is moved down by one line and the last line scrolls downward off the screen. The blank line will be cleared to spaces with the present video attribute. See note in INSERT CHARACTER.

	725	ADM 3A	H1410
Key(s)	[CTRL] [A]	N/A	N/A
Code(s)	(01)	---	---

4.16 Line Feed

The cursor moves down one line in the same column. If it is on the bottom line of the screen the screen will scroll upwards.

	725	ADM 3A	H1410
Key(s)	[CTRL] [J/4]	[CTRL] [J/4]	[CTRL] [J/4]
Code(s)	(0A)	(0A)	(0A)

4.17 Lock Keyboard

After receipt of this command the keyboard will not generate any output codes until either an unlock command is received or the [CLEAR] key is struck.

	725	ADM 3A	H1410
Key(s)	N/A	[CTRL] [O/3]	[ESC] [CTRL] [U]
Code(s)	---	(OF)	(1B) (15)

4.18 New Line

This command forces the terminal to perform a CARRIAGE RETURN and a LINE FEED.

	725	ADM 3A	H1410
Key(s)	N/A	N/A	[CTRL] [SHIFT] [-/-]
Code(s)	---	---	(1F)

4.19 Null

Sending the ASCII NULL (00) is accomplished by holding the [CTRL] key down and then typing the @ sign, (ˆ) or space bar. This is generally used as a filler code and is not acted upon when received.

	725	ADM 3A	H1410
Key(s)	---[CTRL]	ANY NUMBER KEY	---

4.20 Report Character at Cursor Position

The ASCII code for the character at the cursor position is transmitted to the computer followed by a carriage return code.

	725	ADM 3A	H1410
Key(s)	[CTRL] [R]	N/A	[ESC] [CTRL] [T]
Code(s)	(12)	--	(1B) (14)

4.21 Report Cursor Position

After receiving the appropriate command sequence, the terminal will respond by reporting the cursor's current address co-ordinates. Please refer to Appendix 7.2 for the ABSOLUTE CURSOR ADDRESSING TABLES and Appendix 7.3 for a complete list of decimal/hex/ASCII conversions.

	725	ADM 3A	H1410
Key(s)	[CTRL] [E]	N/A	[ESC] [CTRL] [E]
Code(s)	(05)	--	(1B) (05)

4.22 Send Page - Remote

Sends data from the home position to the present cursor position. At the end of each line a carriage return and line feed code is sent. The SEND operation can be initiated locally by depressing the SEND key as described in Section 3.2.5.

	725	ADM 3A	H1410
Key(s)	[CTRL] [B] or [Send]	N/A	N/A
Code(s)	(02)	---	---

4.23 Tab - Column

The cursor will advance to the next fixed TAB stop on the present line. The fixed TAB stops are in column 8, 16, 24, 32, 41, 49, 57, 65, and 73. If the cursor is in columns 73 through 78, it will advance one column. In column 79, the cursor will not move.

	725	ADM 3A	H1410
Key(s)	[CTRL] [I/2]	N/A	N/A
Code(s)	(09)	---	---

4.24 Toggle Video Attribute

When this code is received the video attribute is changed. All subsequently received characters will be displayed at the new setting of the video attribute. The video attribute is user selectable to be either reduced/full intensity or normal (white characters on a black background)/reverse video. The selection of this option is described in Section 6.2.

	725	ADM 3A	H1410
Keys	[CTRL] [N]	N/A	N/A
Codes	(OE)	---	---

4.25 Unlock Keyboard

Receipt of this command enables the keyboard to generate output codes.

	725	ADM 3A	H1410
Keys	N/A	[CTRL] [N]	[ESC] [CTRL] [F]
Codes	---	(OE)	(1B) (06)

5.0 Interface Instructions

All connections and switches mentioned in the following sections are shown in Figure 5.2.

5.1 EIA Connector Pin Assignments

The pin assignments for the two 25 pin EIA connectors on the rear of the 725 are as follows:

I/O Connector:

Pin Number	Signal
1	Ground
2	Serial RS232c data out of terminal
3	Serial RS232c data into terminal
6	Data Set Ready (into terminal)
7	Ground
10	Current Loop Output (+)
11 (or 9)	Current Loop Output (-)
12	Current Loop Input (+)
13	Current Loop Input (-)
20	Data Terminal Ready (High whenever terminal is on)

AUX Connector:

Pin Number	Signal
1	Ground
2	Serial RS232c data out of terminal
3	Serial RS232c data into terminal
7	Ground

The AUXILLIARY connector provides a means of "eavesdropping" on the conversation taking place between the terminal and the computer. Pins 2 and 3 of the AUX connector are electrically connected to pins 2 and 3 of the I/O connector.

5.2 Current Loop Interface

An optically isolated, polarized, passive, 20mA current loop interface is available as a standard feature of the 725. In order to enable it pins 10, 11, 12 and 13 on the I/O connector must be connected to the computer as follows:

I/O Connector:

Pin Number	Signal
12	Receiver Current input (+)
13	Receiver Current return (-)
10	Transmitter Current sink (+)
11 (or 9)	Transmitter Current source (-)

In order to activate the current loop interface the switch on the rear of the terminal must be positioned properly.

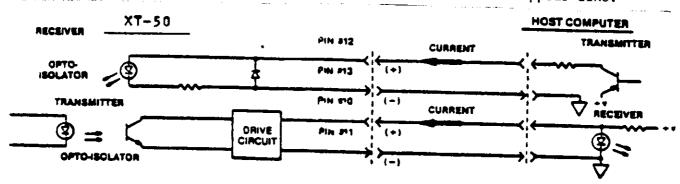Since the interface is passive, a typical installation would appear like:

Figure 5.1 Typical Current Loop Connection

5.3 Full and Half Duplex Operation

The 725 may operate in either full or half duplex modes. In full duplex, all characters typed at the keyboard and sent to the host computer are echoed by the host and appear on the screen. In the half duplex mode, the host does not echo the characters sent to it so the 725 provides a local echo of each transmitted character. Some modems require the half duplex mode - otherwise full duplex is usually the preferred mode of operation. A switch is provided at the rear of the terminal for selecting between the full and half duplex modes.

5.4 Data Rate Selection

The 725 features data transmission/reception rates of 110, 300, 600, 1200, 2400, 4800 and 9600 baud (bits/second) for the I/O and AUXILLIARY communication ports.

Figure 5.2 indicates the location of the 7 switches that select the I/O dat rate. No two switches should be turned on at the same time.

I/0	Switch	Data Rate (Baud)
7		9600
6		4800
5		2400
4		1200
3		600
2		300
1		110

5.5 UART Options

The 725 is factory set to transmit and receive a data word consisting of 1 start bit, an 8th bit (tied high on transmit, ignored on receive) and two stop bits. The parameters of the data word may be modified by reset-ting the UART option switches located on the logic board in the rear of the cabinet (see photo below). The UART option switches have the following effects on the data transmission format:

UART Switch #	Function
3	8th bit transmit select: OFF (switch down) causes a logical 0 (space).
4	Parity select: OFF (switch down) selects no parity; ON enables the type of parity selected by switch 8.
5	Number of stop bits: OFF (switch down) selects 2 stop bits; ON selects one stop bit.
6,7	Word length: Lengths of 5,6,7, or 8 are possible. The parity bit (if selected) is added on to the word length.

Length (Bits)	Switch 7	Switch 6
8	OFF	OFF
7	OFF	ON
6	ON	OFF
5	ON	ON

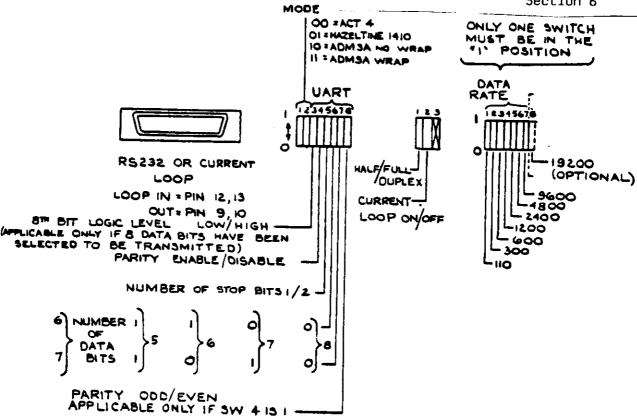|	
8	Odd/Even Parity Select: OFF (switch down) selects odd parity; ON (Switch Up) selects even parity. Switch 10 must be on to enable parity generation.

UART switches three through eight are all factory set to the off position.

MODE
OO = ACT 4
OI = HAZELTINE 1410
IO = ADM 3A NO WRAP
II = ADM3A WRAP

ONLY ONE SWITCH
MUST BE IN THE
"I" POSITION

UART

DATA RATE

RS232 OR CURRENT LOOP

LOOP IN = PIN 12,13
OUT = PIN 9,10
8TH BIT LOGIC LEVEL   LOW/HIGH
(APPLICABLE ONLY IF 8 DATA BITS HAVE BEEN
SELECTED TO BE TRANSMITTED)
PARITY ENABLE/DISABLE

HALF/FULL/DUPLEX

CURRENT LOOP ON/OFF

19200 (OPTIONAL)
9600
4800
2400
1200
600
300
110

NUMBER OF STOP BITS 1/2

6 } NUMBER
    } OF   } 5   } 6   } 7   } 8
7 } DATA
    } BITS

PARITY ODD/EVEN
APPLICABLE ONLY IF SW 4 IS I

6.0 User Selectable Options

6.1 Terminal Emulation Selection

The 725 may be commanded to emulate one of three terminals: The Lear
Siegler ADM 3A, Hazeltine 1400, or 725 Mode Switches 1 and 2 (T.O.1 and
T.O.2) select the terminal to be emulated as follows:

T.O.1	T.O.2	Emulation
OFF	OFF	725 Wrap*
OFF	ON	1410 Wrap*
ON	OFF	ADM 3A No Wrap*
ON	ON	ADM 3A Wrap*

*Wrap/No Wrap refers to the action taken when the last position on the
line is filled with a displayable character. To wrap is to proceed filling
the next line; to not wrap is to leave the cursor in the last column and
"overprint" characters.

6.2 Video Attribute Select

Each character in the display memory is displayed according to the video attribute that was in effect when the character was received. The video attribute may be either high or low intensity or it may be either normal or reverse video.

In order to change the video attribute from high/low intensity (the factory setting), W1 must be inserted as follows:

W1 Connection	Video Attribute
S-A	High/Low Intensity (Factory Setting)
S-B	Normal/Reverse Video

NOTE: Terminals with serial numbers greater than A0106061 have the video attributes switch selectable. Switch 8 in the baud rate switchpack when in the "ON" position selects High/Low Intensity; in the "OFF" position, Normal/Reverse Video is the current video attribute.

Refer to Figure 5.2.

7.0 Appendices

7.1 Function Summaries

7.1.1 725 Control Code Summary

HEX Code	Control Character	Function
00	@	Null
01	A	Insert Line
02	B	Send Page
04	D	Delete Character
05	E	Report Cursor Position
07	G	Bell
08	H	Backspace
09	I	Column Tab
0A	J	Line Feed
0B	K	Cursor Down
0C	L	Home and Clear to Present Attribute
0D	M	Carriage Return
0E	N	Change Attribute
12	R	Report Character at Cursor
13	S	Insert Character
14	T	Cursor Addressing (Y,X)
17	W	Delete Line
18	X	Cursor Right
1A	Z	Cursor Up
1D	]	Home Up
1E	^	Clear From Cursor to End of Line
1F	_	Clear From Cursor to End of Screen

7.1.2 ADM 3A Control Code Summary

HEX Code	Control Character	Function
00	@	Null
07	G	Bell
08	H	Backspace
0A	J	Linefeed
0B	K	Cursor Up
0C	L	Cursor Right
0D	M	Return
0E	N	Unlock Keyboard
0F	O	Lock Keyboard
1A	Z	Home and Clear
1B	[	Curosr Addressing (=, Column, row)
1E	^	Home Up

7.1.3 Hazeltine 1410 Control Code Summary

HEX Code	Control Character	Function
00	@	Nulls
07	G	Bell
08	H	Backspace
0A	J	Linefeed
0B	K	Cursor Up*
0D	M	Return (New Line)**
10	P	Cursor Right
1B	[	Lead in Characters***

7.1.4 Hazeltine 1410 Escape Response Summary

HEX Code	Control Character	Function
05	E	Report Cursor Address
06	F	Unlock Keyboard
11	Q	Address Cursor, Column, Row
12	R	Home Up
14	T	Report Character at Cursor
15	U	Lock Keyboard
1C	\	Home and Clear Screen

Notes:

*   The cursor up function has been added to the Hazeltine 1410 command
    set to allow complete cursor positioning capability.

** Per Hazeltine 1410: receipt of "return" causes a new line. Receipt
    of either sequence "return, linefeed" or "linefeed, return" effects
    a single new line (no double spacing).

*** The lead in character may be either ESC (1B) or ~ (7E).

7.2 Absolute Cursor Positioning Tables

7.2.1 725 Cursor Address Tables

DECIMAL	ASCII	ROW	COLUMN	DECIMAL	ASCII	ROW	COLUMN
0	CTRL 0	0	0	64	@	16	64
1	CTRL A	1	1	65	A	17	65
2	CTRL B	2	2	66	B	18	66
3	CTRL C	3	3	67	C	19	67
4	CTRL D	4	4	68	D	20	68
5	CTRL E	5	5	69	E	21	69
6	CTRL F	6	6	70	F	22	70
7	CTRL G	7	7	71	G	23	71
8	CTRL H	8	8	72	H	0	72
9	CTRL I	9	9	73	I	1	73
10	CTRL J	10	10	74	J	2	74
11	CTRL K	11	11	75	K	3	75
12	CTRL L	12	12	76	L	4	76
13	CTRL M	13	13	77	M	5	77
14	CTRL N	14	14	78	N	6	78
15	CTRL O	15	15	79	O	7	79
16	CTRL P	16	16	80	P	8	0
17	CTRL Q	17	17	81	Q	9	1
18	CTRL R	18	18	82	R	10	2
19	CTRL S	19	19	83	S	11	3
20	CTRL T	20	20	84	T	12	4
21	CTRL U	21	21	85	U	13	5
22	CTRL V	22	22	86	V	14	6
23	CTRL W	23	23	87	W	15	7
24	CTRL X	0	24	88	X	16	8
25	CTRL Y	1	25	89	Y	17	9
26	CTRL Z	2	26	90	Z	18	10
27	CTRL [	3	27	91	[	19	11
28	CTRL \	4	28	92	\	20	12
29	CTRL]	5	29	93	]	21	13
30	CTRL ^	6	30	94	^	22	14
31	CTRL _	7	31	95	_	23	15
32		8	32	96	`	0	16
33	!	9	33	97	a	1	17
34	"	10	34	98	b	2	18
35	#	11	35	99	c	3	19
36	$	12	36	100	d	4	20
37	%	13	37	101	e	5	21
38	&	14	38	102	f	6	22
39	'	15	39	103	g	7	23
40	(	16	40	104	h	8	24
41	)	17	41	105	i	9	25
42	*	18	42	106	j	10	26
43	+	19	43	107	k	11	27
44	,	20	44	108	l	12	28
45	-	21	45	109	m	13	29
46	.	22	46	110	n	14	30
47	/	23	47	111	o	15	31
48	0	0	48	112	p	16	32
49	1	1	49	113	q	17	33
50	2	2	50	114	r	18	34
51	3	3	51	115	s	19	35
52	4	4	52	116	t	20	36
53	5	5	53	117	u	21	37
54	6	6	54	118	v	22	38
55	7	7	55	119	w	23	39
56	8	8	56	120	x	0	40
57	9	9	57	121	y	1	41
58	:	10	58	122	z	2	42
59	;	11	59	123	{	3	43
60	<	12	60	124	|	4	44
61	=	13	61	125	}	5	45
62	>	14	62	126	~	6	46
63	?	15	63				

7.2.2 ADM 3A Cursor Address Tables

ASCII DECIMAL CODE	CHARACTER	CRT POSITION ROW #	COLUMN #
0	CTRL 0		
1	CTRL A		
2	CTRL B		
3	CTRL C		
4	CTRL D		
5	CTRL E		
6	CTRL F		
7	CTRL G		
8	CTRL H		
9	CTRL I		
10	CTRL J		
11	CTRL K		
12	CTRL L		
13	CTRL M		
14	CTRL N		
15	CTRL O		
16	CTRL P		
17	CTRL Q		
18	CTRL R		
19	CTRL S		
20	CTRL T		
21	CTRL U		
22	CTRL V		
23	CTRL W		
24	CTRL X		
25	CTRL Y		
26	CTRL Z		
27	CTRL [		
28	CTRL \		
29	CTRL]		
30	CTRL ^		
31	CTRL _		
32			0
33	!		1
34	"		2
35	#		3
36	$		4
37	%		5
38	&		6
39	'		7
40	(		8
41	)		9
42	*		10
43	+		11
44	,		12
45	-		13
46	.		14
47	/		15
48	0		16
49	1		17
50	2		18
51	3		19
52	4		20
53	5		21
54	6		22
55	7		23
56	8		24
57	9		25
58	:		26
59	;		27
60	<		28
61	=		29
62	>		30
63	?		31

ASCII DECIMAL CODE	CHARACTER	CRT POSITION ROW #	COLUMN #
64	@	0	32
65	A	1	33
66	B	2	34
67	C	3	35
68	D	4	36
69	E	5	37
70	F	6	38
71	G	7	39
72	H	8	40
73	I	9	41
74	J	10	42
75	K	11	43
76	L	12	44
77	M	13	45
78	N	14	46
79	O	15	47
80	P	16	48
81	Q	17	49
82	R	18	50
83	S	19	51
84	T	20	52
85	U	21	53
86	V	22	54
87	W	23	55
88	X		56
89	Y		57
90	Z		58
91	[		59
92	\		60
93	]		61
94	^		62
95	_		63
96	`		64
97	a		65
98	b		66
99	c		67
100	d		68
101	e		69
102	f		70
103	g		71
104	h		72
105	i		73
106	j		74
107	k		75
108	l		76
109	m		77
110	n		78
111	o		79
112	p		
113	q		
114	r		
115	s		
116	t		
117	u		
118	v		
119	w		
120	x		
121	y		
122	z		
123	{		
124				
125	}		
126	~		

7.2.3 Hazeltine 1410 Cursor Address Tables

ASCII DECIMAL CODE	CHARACTER	CRT POSITION ROW #	CRT POSITION COLUMN #	ASCII DECIMAL CODE	CHARACTER	CRT POSITION ROW #	CRT POSITION COLUMN #
0	CTRL 0	0	0	64	@	0	64
1	CTRL A	1	1	65	A	1	65
2	CTRL B	2	2	66	B	2	66
3	CTRL C	3	3	67	C	3	67
4	CTRL D	4	4	68	D	4	68
5	CTRL E	5	5	69	E	5	69
6	CTRL F	6	6	70	F	6	70
7	CTRL G	7	7	71	G	7	71
8	CTRL H	8	8	72	H	8	72
9	CTRL I	9	9	73	I	9	73
10	CTRL J	10	10	74	J	10	74
11	CTRL K	11	11	75	K	11	75
12	CTRL L	12	12	76	L	12	76
13	CTRL M	13	13	77	M	13	77
14	CTRL N	14	14	78	N	14	78
15	CTRL O	15	15	79	O	15	79
16	CTRL P	16	16	80	P	16	
17	CTRL Q	17	17	81	Q	17	
18	CTRL R	18	18	82	R	18	
19	CTRL S	19	19	83	S	19	
20	CTRL T	20	20	84	T	20	
21	CTRL U	21	21	85	U	21	
22	CTRL V	22	22	86	V	22	
23	CTRL W	23	23	87	W	23	
24	CTRL X		24	88	X		
25	CTRL Y		25	89	Y		
26	CTRL Z		26	90	Z		
27	CTRL [		27	91	[		
28	CTRL \		28	92	\		
29	CTRL]		29	93	]		
30	CTRL ^		30	94	^		
31	CTRL _		31	95	_		
32		0	32	96	`		
33	!	1	33	97	a	0	0
34	"	2	34	98	b	1	1
35	#	3	35	99	c	2	2
36	$	4	36	100	d	3	3
37	%	5	37	101	e	4	4
38	&	6	38	102	f	5	5
39	'	7	39	103	g	6	6
40	(	8	40	104	h	7	7
41	)	9	41	105	i	8	8
42	*	10	42	106	j	9	9
43	+	11	43	107	k	10	10
44	,	12	44	108	l	11	11
45	-	13	45	109	m	12	12
46	.	14	46	110	n	13	13
47	/	15	47	111	o	14	14
48	0	16	48	112	p	15	15
49	1	17	49	113	q	16	16
50	2	18	50	114	r	17	17
51	3	19	51	115	s	18	18
52	4	20	52	116	t	19	19
53	5	21	53	117	u	20	20
54	6	22	54	118	v	21	21
55	7	23	55	119	w	22	22
56	8		56	120	x	23	23
57	9		57	121	y		24
58	:		58	122	z		25
59	;		59	123	{		26
60	<		60	124	|		27
61	=		61	125	}		28
62	>		62	126	~		29
63	?		63				30

The recommended cursor addresses are shown in the outlined areas; they are the codes produced when the cursor address is requested. Other codes send will produce the row & column indicated.

7.3 Table of ASCII Codes

CTRL	Character	Binary Bit 7 to Bit 0	Octal	Decimal	Hexadecimal
@	NUL	00000000	000	000	00
A	SOH	00000001	001	001	01
B	STX	00000010	002	002	02
C	ETX	00000011	003	003	03
D	EOT	00000100	004	004	04
E	ENQ	00000101	005	005	05
F	ACK	00000110	006	006	06
G	BEL	00000111	007	007	07
H	BS	00001000	010	008	08
I	HT	00001001	011	009	09
J	LF	00001010	012	010	0A
K	VT	00001011	013	011	0B
L	FF	00001100	014	012	0C
M	CR	00001101	015	013	0D
N	SO	00001110	016	014	0E
O	SI	00001111	017	015	0F
P	DLE	00010000	020	016	10
Q	DC1	00010001	021	017	11
R	DC2	00010010	022	018	12
S	DC3	00010011	023	019	13
T	DC4	00010100	024	020	14
U	NAK	00010101	025	021	15
V	SYN	00010110	026	022	16
W	ETB	00010111	027	023	17
X	CAN	00011000	030	024	18
Y	EM	00011001	031	025	19
Z	SUB	00011010	032	026	1A
[	ESC	00011011	033	027	1B
\	FS	00011100	034	028	1C
]	GS	00011101	035	029	1D
^	RS	00011110	036	030	1E
_	US	00011111	037	031	1F
	SP	00100000	040	032	20
	!	00100001	041	033	21
	"	00100010	042	034	22
	#	00100011	043	035	23
	$	00100100	044	036	24
	%	00100101	045	037	25
	&	00100110	046	038	26
	'	00100111	047	039	27
	(	00101000	050	040	28
	)	00101001	051	041	29
	*	00101010	052	042	2A
	+	00101011	053	043	2B
	,	00101100	054	044	2C
	-	00101101	055	045	2D
	.	00101110	056	046	2E
	/	00101111	057	047	2F
	0	00110000	060	048	30
	1	00110001	061	049	31
	2	00110010	062	050	32
	3	00110011	063	051	33
	4	00110100	064	052	34
	5	00110101	065	053	35
	6	00110110	066	054	36
	7	00110111	067	055	37
	8	00111000	070	056	38
	9	00111001	071	057	39
	:	00111010	072	058	3A
	;	00111011	073	059	3B
	<	00111100	074	060	3C
	=	00111101	075	061	3D
	>	00111110	076	062	3E
	?	00111111	077	063	3F
	@	01000000	100	064	40
	A	01000001	101	065	41
	B	01000010	102	066	42
	C	01000011	103	067	43
	D	01000100	104	068	44
	E	01000101	105	069	45
	F	01000110	106	070	46
	G	01000111	107	071	47
	H	01001000	110	072	48
	I	01001001	111	073	49
	J	01001010	112	074	4A
	K	01001011	113	075	4B
	L	01001100	114	076	4C
	M	01001101	115	077	4D
	N	01001110	116	078	4E
	O	01001111	117	079	4F
	P	01010000	120	080	50
	Q	01010001	121	081	51
	R	01010010	122	082	52
	S	01010011	123	083	53
	T	01010100	124	084	54
	U	01010101	125	085	55
	V	01010110	126	086	56
	W	01010111	127	087	57
	X	01011000	130	088	58
	Y	01011001	131	089	59
	Z	01011010	132	090	5A
	[	01011011	133	091	5B
	\	01011100	134	092	5C
	]	01011101	135	093	5D
	^	01011110	136	094	5E
	_	01011111	137	095	5F
	`	01100000	140	096	60
	a	01100001	141	097	61
	b	01100010	142	098	62
	c	01100011	143	099	63
	d	01100100	144	100	64
	e	01100101	145	101	65
	f	01100110	146	102	66
	g	01100111	147	103	67
	h	01101000	150	104	68
	i	01101001	151	105	69
	j	01101010	152	106	6A
	k	01101011	153	107	6B
	l	01101100	154	108	6C
	m	01101101	155	109	6D
	n	01101110	156	110	6E
	o	01101111	157	111	6F
	p	01110000	160	112	70
	q	01110001	161	113	71
	r	01110010	162	114	72
	s	01110011	163	115	73
	t	01110100	164	116	74
	u	01110101	165	117	75
	v	01110110	166	118	76
	w	01110111	167	119	77
	x	01111000	170	120	78
	y	01111001	171	121	79
	z	01111010	172	122	7A
	{	01111011	173	123	7B
	|	01111100	174	124	7C
	}	01111101	175	125	7D
	~	01111110	176	126	7E
	DEL	01111111	177	127	7F

CTRL	ABBR.	DESCRIPTION
@	NUL	null, or all zeros
A	SOH	start of heading
B	STX	start of text
C	ETX	end of text
D	EOT	end of transmission
E	ENQ	enquiry
F	ACK	acknowledge
G	BEL	bell
H	BS	backspace
I	HT	horizontal tabulation
J	LF	line feed
K	VT	vertical tabulation
L	FF	form feed
M	CR	carriage return
N	SO	shift out
O	SI	shift in
P	DLE	datalink escape
Q	DC1	device control 1 (X ON)
R	DC2	device control 2
S	DC3	device control 3 (X OFF)
T	DC4	device control 4
U	NAK	negative acknowledge
V	SYN	synchronous idle
W	ETB	end of transmission block
X	CAN	cancel
Y	EM	end of medium
Z	SUB	substitute
[	ESC	escape
\	FS	file separator
]	GS	group separator
^	RS	record separator
_	US	unit separator
	SP	space
	DEL	delete

7.4 <u>Control Character Set Dot Pattern</u>

@	A	B	C	D	E	F	G
H	I	J	K	L	M	N	O
P	R	S	T	U	V	W	X
Y	Z	[	\	]	^	_

SPECIFICATION

W7993-800 - C.P.U.

W7993-864 - 64K DYNAMIC RAM

C.P.U.

The WYNCHESTER central processor and input/output system provides all of the CPU and I/O facilities required for the W7993.

The single card has the following features:

2 Mhz. 8080A Microprocessor with fully buffered S-100 bus interface system.

EIA RS-232 compatible terminal port with software programmable baud rates from 110 baud to 76 kilobaud.

Fully vectored interrupt system using TMS-5501 integrated circuit.

Five programmable interval timers with interrupt capability using the TMS-5501 integrated circuit.

An EIA compatible auxiliary pseudo-serial port suitable for interfacing with a serial printer at baud rates of up to 2400 baud.

An interface compatible with many common diskette and miniature diskette drives supporting IBM 3740 soft-sectored format.

On-board digital data separator for full size diskette drives.

Provision for up to 2K bytes of EPROM memory (2708 or 2716) with power on vectoring to allow page 0 to be left free for RAM (does not require memory cards with phantom option).

24 spare parallel user I/O lines with provisions for fully handshaked use as input or output ports (8255).

Unique dual-mapped I/O interfacing allows optimal programming for I/O access. All devices may be accessed either in I/O space or as memory locations as the programmer desires.

MWRITE generation on board so that no front panel is needed.

Low power operation, typically requires 8V at 0.8A, 15V at 0.15A, and -15V at 0.05A

Auxiliary cassette input and output (software driven) is available for use without disk in some stand alone applications.

The design accommodates an optional switch for generation of a user interrupt on level RST 7 for use with a debugger or user program.

W.7993-CPU

MEMORY MAP FOR CP/M OPERATION

```
ffff    ********************************************************
        top half of 2716
fc00    ********************************************************
        bottom half of 2716
f800    ********************************************************
                    8255 PPI        ctrl      f700-f7ff
                                    C port    f600-f6ff
                    (user IO)       B port    f500-f5ff
                                    A port    f400-f4ff
f400    ********************************************************
                    FD1771          data      f300-f3ff
                    diskette        sector    f200-f2ff
                    controller      track     f100-f1ff
                                    st/cmd    f000-f0ff
f000    ********************************************************
                    TMS5501         none      ef00-efff
                                    none      ee00-eeff
                                    timer5    ed00-edff
                                    timer4    ec00-ecff
                                    timer3    eb00-ebff
                                    timer2    ea00-eaff
                                    timer1    e900-e9ff
                                    mask      e800-e8ff
                                    par.out   e700-e7ff
                                    tx buff   e600-e6ff
                                    baud      e500-e5ff
                                    cmnd      e400-e4ff
                                    stat      e300-e3ff
                                    rst #     e200-e2ff
                                    par.in    e100-e1ff
                                    rx in     e000-e0ff
e000    ********************************************************


                                RAM BOARDS

07ff    ********************************************************

                EPROM ALIAS during boot until first
                memory write or IO write after reset
                and then USER INSTALLED MEMORY

0000    ********************************************************
```

Note that all on-card IO devices may also be accessed at IO port addresses corresponding to the high order byte of their memory mapped IO address. E.g. the 8255 A port is at 8080 IO address f4h.

Note also that input port addresses between f8h and ffh return that byte of the EPROM whose memory address is equal to the low and high bytes both having that port address. E.G. In f8h returns the contents of EPROM address f8f8h. This may be used to provide a default emulation of the common front panel switch registers found in many computers at input ffh by placing the desired switch register value into the EPROM at location ffffh (or fbffh in the case of a 2708).

After bootstrap has completed, memory utilization is as indicated in CP/M documentation. All BIOS variables are located in the area reserved for them between 40h and 4fh.

Note that all data input and output to the FD1771 is inverted relative to the description in the data sheet for that part.

SYSTEM I/O PORT ASSIGNMENTS

The TMS5501 is normally reserved for use by the system software. The following bits are located on its parallel input and output ports and are used for the purposes indicated.

PARALLEL INPUT BITS

IO address e1h memory address e100h to e1ffh

BIT 7   INTRQ flag from disk controller, 1=done, also generates RST7
BIT 6   Common seek sense input from jumper N-O
                if jumper is installed = 0 else 1
BIT 5   Auxiliary protocol from pin 13 on io connector, 1=asserted
                normally used as lpt Clear-to-send input
                -also cassette input if jumpered
BIT 4   Auxiliary protocol from pin 11 on io connector, 1=asserted
BIT 3   Auxiliary protocol from pin 4 on io connector, 1=asserted
BIT 2   INTE readback from 8080 - 1 means interrupts are enabled
BIT 1   HLD readback from 1771 - 1 means controller asserting select
BIT 0   DRQ flag from disk controller, 1= data request, also RST 2

PARALLEL OUTPUT BITS

IO address e7h, memory address e700h to e7ffh

BIT 7   Auxiliary protocol line to pin 14 on io connector, 1=+8
                normally used as lpt data out where 0=MARK
                -also cassette output
BIT 6   Auxiliary protocol line to pin 12 on io connector, 1=+8
BIT 5   Auxiliary protocol line to pin 5 on io connector, 1=+8
BIT 4   RST 7 multiplex control, 1= switch, 0= INTRQ
BIT 3   Hard Restore command line - 0= restore
BIT 2   Force drive select - overrides 1771 deselection of drive
                0=force selection
BIT 1   Disk unit select msb (inverted)
BIT 0   Disk unit select lsb (inverted)

Restart 2 is usable by the system to indicate disk DRQ although it is not used by the present BIOS. Restart 7 is used during disk IO operations only to indicate completion. Whatever was present in the vector at entry to the disk IO call will be restored before control is returned to the user program. This vector is default initialized to produce a warm start unless altered by a transient program.

Note that all data input from and output to the FD1771 disk controller ports must be inverted relative to the descriptions in the data sheet for that port.

The CBIOS EPROM included with the W7993's CPU card have been designed primarily to support the CP/M disk operating system as supplied by DIGITAL RESEARCH CORP-ORATION.

Upon power-up or reset, the standard BIOS software waits for the user to set the terminal baud rate before it does anything else. It cannot prompt for this action because it does not yet know terminal speed. The user must strike the spacebar on his terminal to set baud rate. Once this has been done the terminal should display the following banner message:

> W7993 System Loader V 4.2
> (Disk Drive Information)
> (Printer baud rate information)

> MOUNT DISK A

If this message does not appear, try resetting the computer via the front panel interrupt switch, and re-striking space bar. Striking any other key may set an incorrect baud rate.

Once the banner has been printed, the BOOT routines will try to access Drive A. An attempt will be made to load the head and the operating system if a disk has been mounted.

If a proper copy of CP/M is found on the disk, there will be a number of disk accesses to the first three tracks of the disk, and about two seconds later the CP/M operating system should prompt with the correct drive name: A > as described in the CP/M manuals.

If the system cannot be loaded, the system will display a set of error codes detailing the failure and HALT the computer. Once the fault has been corrected, the computer must be reset before attempting to load the system again. After the A > prompt appears, operation is as described in the CP/M manuals with the exception of items noted under "Things not to do".

Occasionally, disks of unknown origin or ancestry contain information that can fool the tests for a valid system disk. If neither the error codes nor the CP/M prompt appear within 5 seconds, remove the disk, reset the system, and investigate.

WRITE PROTECTION

The CP/M operating system does not allow the use of hardware write-protect. Even if it is only reading a file, it will still update the directory entry involved whenever an extent boundary is crossed. As a result, it is not recommended that write-protected disks be used even though the system drives have write-protect sensors installed. CP/M provides a software write-protect scheme that is adequate for most purposes. If hardware write-protection is used, a non-fatal error will occur each time the system tries to update a directory entry on the write-protected disk.

INPUT-OUTPUT SYSTEM

When operating under CP/M, the normal CP/M logical devices are implemented as follows:

CON:	is the serial port
PUN:	is the serial port output
RDR:	is the serial port input (no echo)
LPT:	is the printer port

Since there are no alternative I/O devices, the IOBYTE feature is not implemented but the I/O byte is set to 0 at cold start to ensure compatibility.

PRINTER

The printer port waits for CTS to be true before sending anything. This allows use with printers that support hand-shaking to maximize printing speed. For use with DESPOOL (c DIGITAL RESEARCH), a printer status routine will interrogate the state of this CTS signal and return it to the caller as a flag (O/ff, ff=ready). Version 4.2 BIOS provide automatic check and configuration to serial or parallel printer port.

DUAL-MAPPED I/O

All on-card devices have been wired to allow access using either 8080 I/O instructions, or as memory-mapped I/O devices. You may choose to access the device in either way at any time. This allows optimizing I/O programming for maximum throughput and code efficiency. Refer to the I/O map for details on port addressing. Note also that the memory-mapped access codes ignore the least significant byte of the memory address. This allows the use of the low half of a memory pointer register containing an I/O port address for any other purpose without conflicting with the I/O operation. This technique is used to advantage by disk I/O routines.

For the user's convenience, a switch is provided on the front panel that will generate an interrupt 7 at any time when not in conflict with disk I/O routines. This is useful when debugging programs under DDT or SID. This switch will normally cause a warm boot to occur, when depressed. However, note that some random access programs may lose data base integrity if aborted without a normal exit as programmed by their designers. Avoid aborting such programs and always use caution in aborting any program.

BIOS ERROR CODES

Whenever a non-recoverable disk I/O error occurs, the BIOS software provides auxiliary diagnostic information beyond that supplied by CP/M.

There are two types of such errors: if further attempts at operation are impossible or dangerous, the error is classed as FATAL, and after the error message is printed, the system will HALT with interrupts disabled. Once the error has been corrected it will be necessary to reset the computer system before continuing.

Ordinary READ or WRITE errors are classed as non-fatal, and after the message is printed, control is returned to the calling program with a CP/M compatible error flag in the accumulator.

Normally only the first two hex numbers are of interest, but write down the entire code. It may be of use if you communicate with WYNCHESTER SYSTEMS or a program's authors.

The BIOS error message is of form: I/O Err=a/b/c/d/e/f/g/h/ where all returned values are hexadecimal:

> a is FD1771 command under execution
> b is returned controller status after error
> c is current disk selected when error occurred
> d is LSTDSK value (diagnostic use only)
> e is current track
> f is current sector
> g is low-order address of disk buffer
> h is high-order address of disk buffer

a, contains a code of 0 if boot operation fails, Possible causes are: insufficient memory for program being loaded, bad memory (the last page used by CP/M is non-destructively tested at load time), bad disk, disk without proper CP/M, or possible hardware failure.

Refer to the BIOS documentation and the FD1771 data sheet to interpret status byte and command field value. Generally:
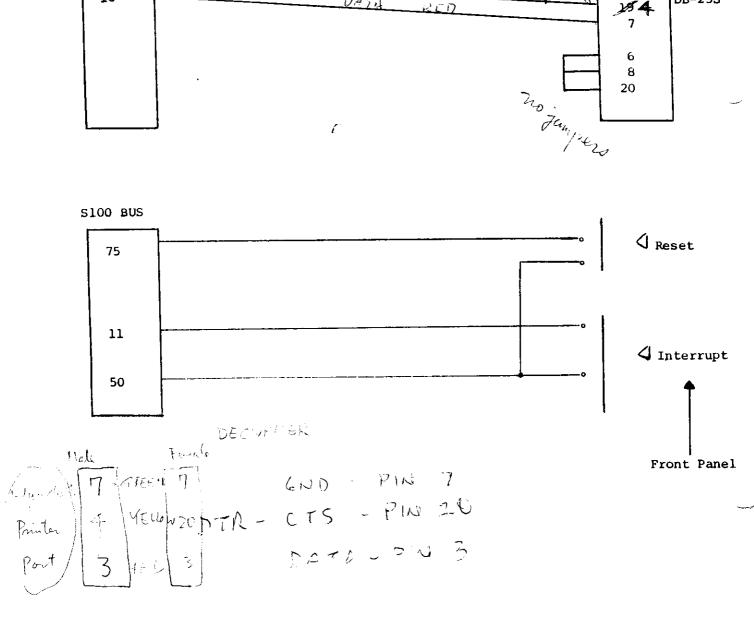
> 00=BOOT FAILURE   0x=RESTORE DRIVE   1x=SEEK TRACK
>
> 8x=READ SECTOR   Ax=WRITE SECTOR

Serial
1/0

J.4

2
3

7

Terminal
DB-25S

2
3
4
5
7
6
20

14
13
16

16
13
14

GND   GREEN   3
CTS   YELL   4
DATA   RED

Printer
DB-25S

3
4
5
34
7

6
8
20

no jumpers

S100 BUS

75

◁ Reset

11

50

◁ Interrupt

Front Panel

DECWRITER

Male   Female

7 GREEN 7
4 YELLOW 20
3 RED   3

Printer
Port

GND - PIN 7
DTR - CTS - PIN 20
DATA - PIN 3

PINS	FUNCTION		DEFAULT
A	Test point and auxiliary power	0 Volts	OPEN
B		-5 Volts	OPEN
C		+5 Volts	OPEN
D		+12 Volts	OPEN
E,F	Jumper enables tape offset trimmer		OPEN
H,G	G to H to use Aux Protocol line as tape input		OPEN
H,I	H to I to use Aux Protocol line as protocol		INSTALLED
J	Posts allows wire-wrap to spare I/O pins 10		OPEN
K	9		OPEN
L	8		OPEN
M	1		OPEN
N,O	Jumper if odd and even disk units are to be treated as having a common positioning mechanism by the BIOS software.		OPEN
P,Q,R, S,T	EPROM type select jumpers. Normally set for 2716 EPROM.		
	FOR 2708 A to R, S to P		OPEN
	FOR TMS 2716 P to Q, S to T		INSTALLED
U,Z	Drive present indication from disk pin 32 on modified drive.		INSTALLED
V,AH	RESTORE hard wire output to drive. This is output bit 3 on Port OE7H.		OPEN
W,X	Jumper disable Formatting of diskettes		OPEN
W,AM	Jumper to allow Formatting of diskettes		INSTALLED
X,AG	Write Current switch (TG43).		INSTALLED
Z	See U		
AA,AJ	Connects pin 32 on 8 inch drive connector to DS4 from system.		INSTALLED

The W7993 CPU card varies slightly in its jumpering. To accomodate the use of 8 inch drives that stop at a 3ms. rate, have optional second heads and fixed disk systems (W740).

1. AK to AI is jumpered
    AK to AM is open
    this enables high speed seek

2. Y to AD is open to enable TG43 Signal

3. The EPROM is jumpered for a TMS-2716 to allow the larger
    BIOS code with full error messages.

4. N to O is jumpered
    note that the BIOS EPROM Ver 4.2 make both surfaces of Drive A
    on the same physical spindle and both surfaces of Drive B on the same
    physical spindle.

5. Note that the Ver 4.2 BIOS EPROM initializes the printer
    baud rate to 2400 instead of 300 baud and is self configuring to
    serial or parallel port.

6. Cut E & F
    Close H & I

7. J.$ - 2-EIA Serial From Terminal
            3-EAI Serial to Terminal
            7-Signal Ground
           13-Serial to Printer
           14-Clear to Send From Printer
           16-Signal Ground

SERIAL INTERFACE CONNECTOR PINOUT (J4)

PIN ***	FUNCTION ********
1	SPARE - connected to wirewrap pin M
2	EIA level serial data input to TMS5501
3	EIA level serial data output from TMS5501
4	EIA level protocol input line #1 (bit 3)
5	EIA level protocol output line #1 (bit 5)
6	EIA "true" level for protocol use (+5V)
7	SIGNAL GROUND
8	SPARE - connected to wirewrap pin L
9	SPARE - connected to wirewrap pin K
10	SPARE - connected to wirewrap pin J
11	EIA level protocol input line #2 (bit 4)
12	EIA level protocol output line #2 (bit 6)
13	EIA level protocol input line #3 (bit 5)
14	EIA level protocol output line #3 (bit 7)
15	EIA "true" level for protocol use (+5V)
16	SIGNAL GROUND
17	CASSETTE INPUT - sliced input to bit #5 (if jumpered)
18	CASSETTE OUTPUT - filtered output from bit #7
19	CASSETTE SIGNAL GROUND
20	NOT USED

If normal use with the CP/M operating system, only the following lines are functional:

2	EIA serial data input from console terminal device
3	EIA serial data output to console terminal device
4	SIGNAL GROUND to console terminal device
11	EIA clear-to-send input to computer from LIST device
14	EIA serial data output to LIST device
16	SIGNAL GROUND for LIST device

All other protocol signals for console and list device are normally tied back to their complementary signal in order to improve interchangeability and simplify user cabling.

The spare lines on the connector may be used for reset and/or interrupt switch wiring if it is considered desireable to bring these out to switches on the terminal device.

S100 BUS SIGNAL DEFINITIONS

PIN	NAME	FUNCTION
***	****	********
1	+8VDC	Unregulated supply
2	+16VDC	Unregulated supply
3	----NOT USED----	
4	XRDY	Connected directly to PRDY
5-10	----NOT USED----	
11	VI7	DEBOUNCED active low interrupt 7 input
12-17	----NOT USED----	
18	/STSDSBL	tri-state disable for status signals
19	/CCDSBL	tri-state disable for bus control signals
20-21	----NOT USED----	
22	/ADDRDSBL	tri-state disable for address outputs
23	/DODSBL	tri-state disable for data outputs
24	phi-2	phase 2 cpu clock output (2.000 MHZ)
25	phi-1	phase 1 cpu clock output (2.000 MHZ)
26	PHLDA	CPU acknowledgement of DMA request
27	PWAIT	CPU acknowledgement of wait request
28	PINTE	CPU output indicates interrupts enabled
29	A5	CPU address output
30	A4	CPU address output
31	A3	CPU address output
32	A15	CPU address output
33	A12	CPU address output
34	A9	CPU address output
35	DO1	CPU data bus output
36	DO0	CPU data bus output
37	A10	CPU address output
38	DO4	CPU data bus output
39	DO5	CPU data bus output
40	DO6	CPU data bus output
41	D12	CPU data bus input
42	D13	CPU data bus input
43	D17	CPU data bus input
44	SM1	Status output - FETCH cycle in progress
45	SOUT	Status output - OUTPUT cycle in progress
46	SINP	Status output - INPUT cycle in progress
47	SMEMR	Status output - MEMORY READ cycle in progress
48	SHLTA	Status output - CPU halted
49	/CLOCK	complement of phase 2 CPU clock
50	GND	Ov return and signal return
51	+8V	Unregulated supply
52	-16V	Unregulated supply
53	----NOT USED----	
54	/EXTCLR	Reset output from CPU card to other bus devices
55-67	----NOT USED----	
68	MWRT	CPU write strobe signal to memory devices
69-71	----NOT USED----	
72	PRDY	CPU ready input (tied directly to XRDY)
73	/PINT	interrupt request input
74	/PHOLD	DMA hold request input

75	/PRESET	Board reset input signal from reset switch
76	PSYNC	start of machine cycle strobe
77	/PWR	CPU memory or io write strobe
78	PDBIN	CPU input strobe (mem, io or interrupt)
79	A0	CPU address bus output
80	A2	CPU address bus output
81	A2	CPU adresss bus output
82	A6	CPU address bus output
83	A7	CPU address bus output
84	A8	CPU address bus output
85	A13	CPU address bus output
86	A14	CPU address bus output
87	A11	CPU address bus output
88	D02	CPU data bus output
89	D03	CPU data bus output
90	D07	CPU data bus output
91	DI4	CPU data bus input
92	DI5	CPU data bus input
93	DI6	CPU data bus input
94	DI1	CPU data bus input
95	DI0	CPU data bus input
96	SINTA	Status output - INTERRUPT cycle in progress
97	/SWO	Status output - WRITE cycle in progress
98	SSTACK	Status output - STACK cycle in progress
99	/POC	Reset output provided by CPU to bus
100	GND	0v return and signal return

```
                    ;        DECODING PATTERN FOR SELECT PROM #1 FOR
                    ;        SYSTEM CPU BOARD
                    ;
                    ;
                    ;
                    ;
                    ;
                    ;
                    ;
                    ;
                    ;        PATTERN FOR MEMORY MAP / IO MAP
                    ;               TMS 5501         0E000H TO 0EFFFH
                    ;               FD 1771B-1       0F000H TO 0F3FFH
                    ;               8255A            0F400H TO 0F7FFH
                    ;               2708/2716        00000H TO 007FFH AT BOOT ONLY
                    ;                                0F800H TO 0FFFFH ALWAYS
                    ;
                    ;        CONDITION INPUTS
                    ;        A7      IS SYSTEM BOOT MODE FLAG (0=BOOT)
                    ;        A6      IS SYSTEM ADDRESS LINE A15
                    ;        A5      IS SYSTEM ADDRESS LINE A14
                    ;        A4      IS SYSTEM ADDRESS LINE A13
                    ;        A3      IS SYSTEM ADDRESS LINE A12
                    ;        A2      IS SYSTEM ADDRESS LINE A11
                    ;        A1      IS SYSTEM ADDRESS LINE A10
                    ;        A0      IS DMA DISABLE (HLDA=1)
                    ;        /CS1    IS INTA DISABLE (INTA=1) DISABLES ALL DECODING
                    ;        /CS2    IS ALWAYS 0
                    ;
                    ;        SYMBOLIC PROM ENABLES
                    ;        ALL SELECTS ARE LOW GOING (/CS) MODE
000F =                NONE   EQU     0FH     ;ALL DISABLED
0007 =                UART   EQU     07H     ;5501 IS BIT D3
000B =                EPRM   EQU     0BH     ;EPROM IS BIT D2
000D =                FDCC   EQU     0DH     ;DISK CONTROLLER IS BIT D1
000E =                PPI1   EQU     0EH     ;USER PPI IS BIT D0
                    ;
0000                  ORG     0     ;RELATIVE OFFSET OF 0
              START:
                    ;        THIS IS BOOT HALF OF PROM
0000 0B0F0B0F0FADR00:  DB     EPRM,NONE,EPRM,NONE,NONE,NONE,NONE,NONE
0008 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0010 0F0F0F0F0FADR10:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0018 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0020 0F0F0F0F0FADR20:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0028 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0030 0F0F0F0F0FADR30:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0038 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0040 0F0F0F0F0FADR40:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0048 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0050 0F0F0F0F0FADR50:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0058 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0060 0F0F0F0F0FADR60:  DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0068 0F0F0F0F0F        DB     NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
0070 070F070F07ADR70:  DB     UART,NONE,UART,NONE,UART,NONE,UART,NONE
0078 0D0F0E0F0B        DB     FDCC,NONE,PPI1,NONE,EPRM,NONE,EPRM,NONE
```

```
                    ;          THIS IS NORMAL MODE HALF OF PROM
 0080  0F0F0F0F0FADR80:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 0088  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 0090  0F0F0F0F0FADR90:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 0098  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00A0  0F0F0F0F0FADRA0:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00A8  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00B0  0F0F0F0F0FADRB0:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00B8  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00C0  0F0F0F0F0FADRC0:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00C8  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00D0  0F0F0F0F0FADRD0:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00D8  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00E0  0F0F0F0F0FADRE0:   DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00E8  0F0F0F0F0F         DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,NONE
 00F0  070F070F07ADRF0:   DB      UART,NONE,UART,NONE,UART,NONE,UART,NONE
 00F8  0D0F0E0F0B         DB      FDCC,NONE,PPI1,NONE,EPRM,NONE,EPRM,NONE
                    ;
 0100                     END
```
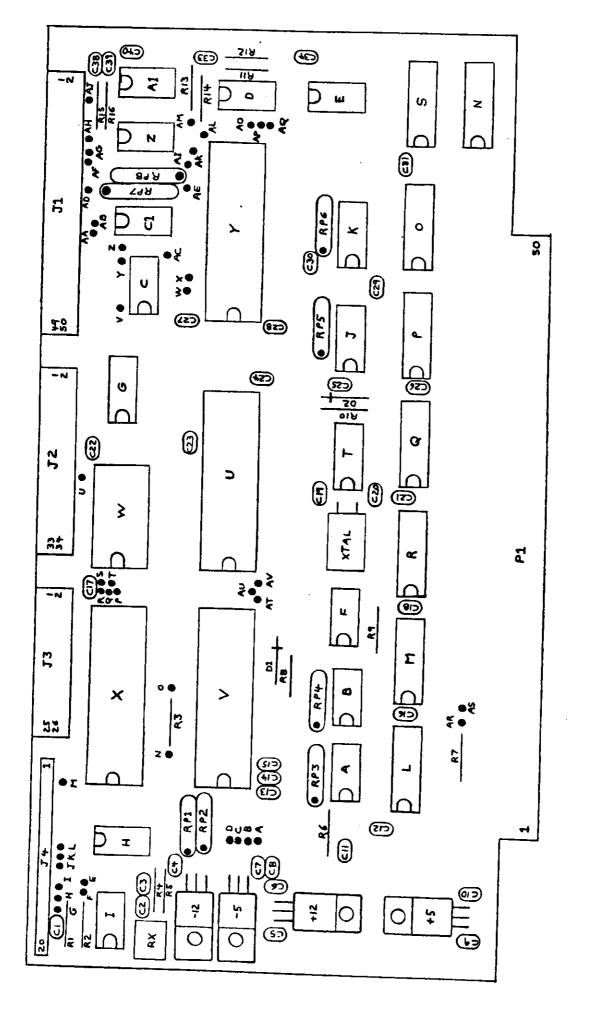
```
;                 DECODING PATTERN FOR CONTROL PROM #2 FOR
;                 SYSTEM CPU BOARD
;
;
;
;
;
;
;
;
;                 PATTERN FOR MEMORY MAP / IO MAP
;                       TMS 5501          0E000H TO 0EFFFH
;                       FD 1771B-1        0F000H TO 0F3FFH
;                       8255A             0F400H TO 0F7FFH
;                       2708/2716         00000H TO 007FFH AT BOOT ONLY
;                                         0F800H TO 0FFFFH ALWAYS
;
;                 CONDITION INPUTS
;                 A7        IS PPI REQUEST (0=REQUEST)
;                 A6        IS FDCC REQUEST (0=REQUEST) (1 WAIT STATE)
;                 A5        IS EPROM REQUEST (0=REQUEST)
;                 A4        IS UART REQUEST (0=REQUEST)
;                 A3        IS INTR REQUEST FLAG FROM 5501  (1=REQUEST)
;                 A2        IS INTA ACKNOWLEDGE FLAG (1=ACKNOWLEDGE)
;                 A1        IS WAIT ACKNOWLEDGE FROM 8080 (1=WAIT)
;                 A0        IS DBIN STROBE FROM 8080 (1=READ)
;                 /CS1      IS ALWAYS 0
;                 /CS2      IS ALWAYS 0
;
;                 SYMBOLIC PROM OUTPUTS
;
0008 =            EPRM      EQU     8H        ;ENABLE EPROM READ (/CS)
000B =            UART      EQU     0BH       ;ENABLE 5501 READ/WRITE (CS)
000D =            WAIT      EQU     0DH       ;WAIT STATE FOR FDCC IN PROGRESS
0009 =            ONBD      EQU     9H        ;ONBOARD DEVICE, NO WAIT IN PROGRESS
0001 =            OFBD·     EQU     1H        ;NOT ONBOARD DEVICE, ENABLE OFFBD INPUT
                  ;
0000              ORG       0                 ;RELATIVE OFFSET OF 0
                  START:
0000 0909090909   ADR00:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0008 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0010 0909090909   ADR10:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0018 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0020 0909090909   ADR20:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0028 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0030 0909090909   ADR30:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0038 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0040 0909090909   ADR40:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0048 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0050 0909090909   ADR50:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0058 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0060 0909090909   ADR60:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0068 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0070 0909090909   ADR70:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0078 0909090909            DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0080 0909090909   ADR80:   DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
```

```
0088  0909090909             DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0090  0909090909ADR90:       DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
0098  0909090909             DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00A0  0909090909ADRA0:       DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00A8  0909090909             DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00B0  0D0D090909ADRB0:       DB      WAIT,WAIT,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00B8  0D0D090909             DB      WAIT,WAIT,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00C0  0909090909ADRC0:       DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00C8  0909090909             DB      ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD,ONBD
00D0  0908090809ADRD0:       DB      ONBD,EPRM,ONBD,EPRM,ONBD,ONBD,ONBD,ONBD
00D8  0908090809             DB      ONBD,EPRM,ONBD,EPRM,ONBD,ONBD,ONBD,ONBD
00E0  0B0B0B0B09ADRE0:       DB      UART,UART,UART,UART,ONBD,ONBD,ONBD,ONBD
00E8  0B0B0B0B09             DB      UART,UART,UART,UART,ONBD,ONBD,ONBD,ONBD
00F0  0901090109ADRF0:       DB      ONBD,OFBD,ONBD,OFBD,ONBD,OFBD,ONBD,OFBD
00F8  0901090109             DB      ONBD,OFBD,ONBD,OFBD,ONBD,ONBD,ONBD,ONBD
                             ;
0100                         END
```

```
DIODES
D1,D2     2   1N4148                              silicon switching diode

INTEGRATED REGULATORS
          1   7805                                TO-220 regulator
          1   7812                                TO-220 regulator
          1   7905                                TO-220 regulator
          1   7912                                TO-220 regulator

INTEGRATED CIRCUITS
L-R       7   74LS244                             octal tri-state buffers
S         1   74LS273                             octal latch with clear
E         1   74LS02                              quad 2 input nor gate
D         1   74LS32                              quad 2 input or gate
C         1   7406                                hex inverting o.c. driver
G         1   74145                               bcd o.c. decoder/driver
Z         1   74LS393                             dual 4 bit async. counter
A1        1   74LS86                              quad 2 input xor gate
F         1   74LS74                              dual type d flip-flop
A,B,C1    3   74LS14                              hex schmitt inverter
I         1   1489                                quad EIA line rcvr.
H         1   1488                                quad EIA line driver
T         1   8224        NS/AMD/INTEL            clock oscillator
U         1   8080A       NS/AMD/INTEL/TI         microprocessor
V         1   TMS5501     TI                      interface adaptor
X         1   8255        NS/INTEL/AMD            parallel interface adaptor
Y         1   FD1771-1    NS/WD                   diskette controller

PROPRIETARY COMPONENTS
J         1   82S126/SYS1           CONTROL PROM  PATTERN COPYRIGHT
K         1   82S126/SYS2           CONTROL PROM  WYNCHESTER SYSTEMS
W         1   2716                  BIOS EPROM,
```

Some variations in capacitor values are normal to board production. Replacement of standard TTL parts with LS parts and vice-versa is not recommended in most component positions although there are exceptions made in some production runs due to parts unavailability. For maintenance purposes, such substitute parts should always be replaced with the types shown in the parts list rather than the type removed since, when used, such alternate parts may be graded by the factory.

COMPONENT LAYOUT

S-100 CPU-CARD

Wynchester
systems and electronics

Although most disk drives have provisions for power supply sequencing, and the W7993 has been designed to avoid accesses to the disk drives during its power-up sequence, these measures may not be effective in cases of repeated power transients. You are urged, as a precaution, to remove disks during power-up and power-down of the system.

DO NOT reset the computer or remove a disk, while the drive containing that disk is being accessed. This may result in premature termination of a sector write operation, and in the case of a directory operation can make recovery of information on a disk impossible.

If a program should ever lose control and the disk remains accessed, try using the interrupt switch before deciding to reset.

Since the system card uses memory-mapped I/O for speed, the user must avoid inadvertent I/O access by programs reading or writing into memory regions that exert I/O control.
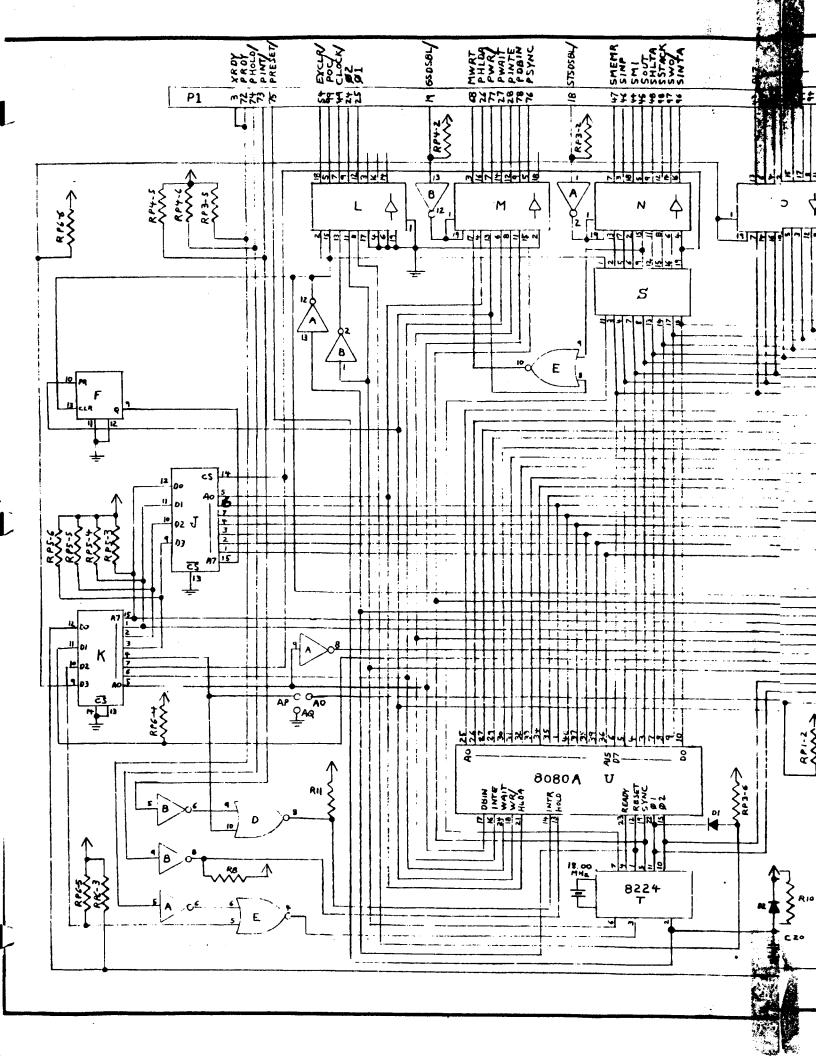
Note the following precautions: Do not use any form of MOVCPM command other than "MOVCPM xx *" where xx is the number of Kbyte RAM in your system.
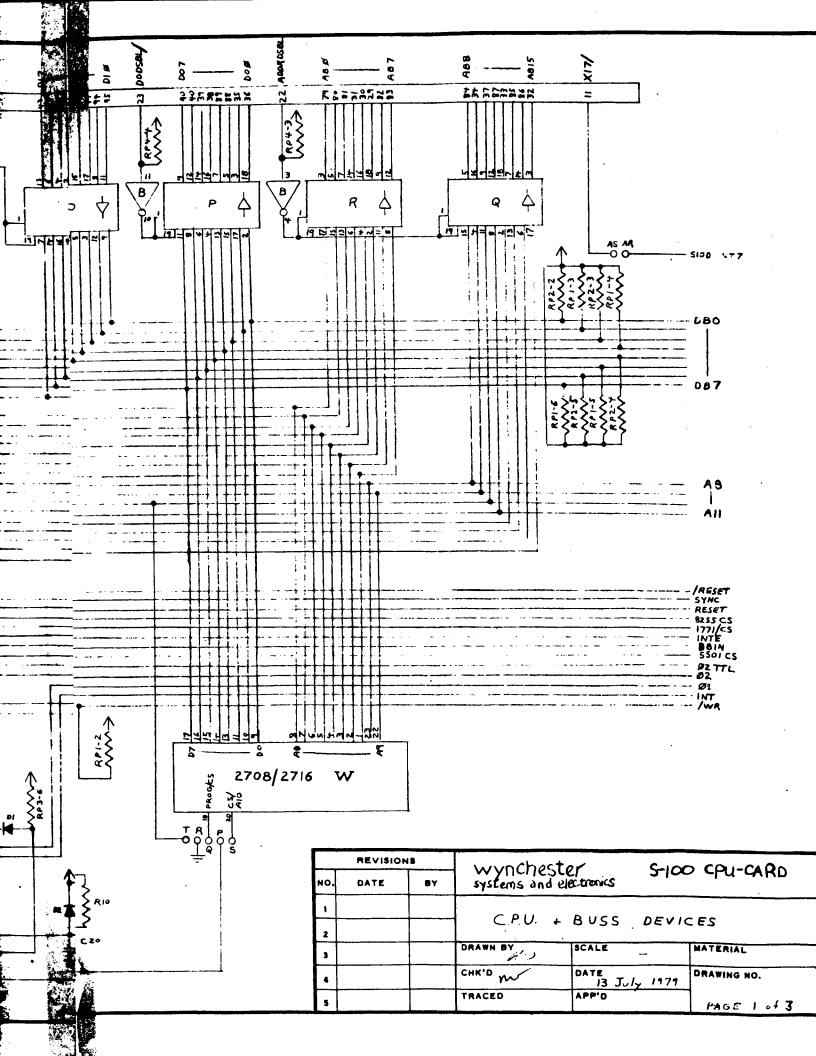
Do not use programs that size memory by running their own tests. Such tests often give commands that can lock up a controller, serial port, or worse. Facilities to find out how much memory is available are provided by the operating system.
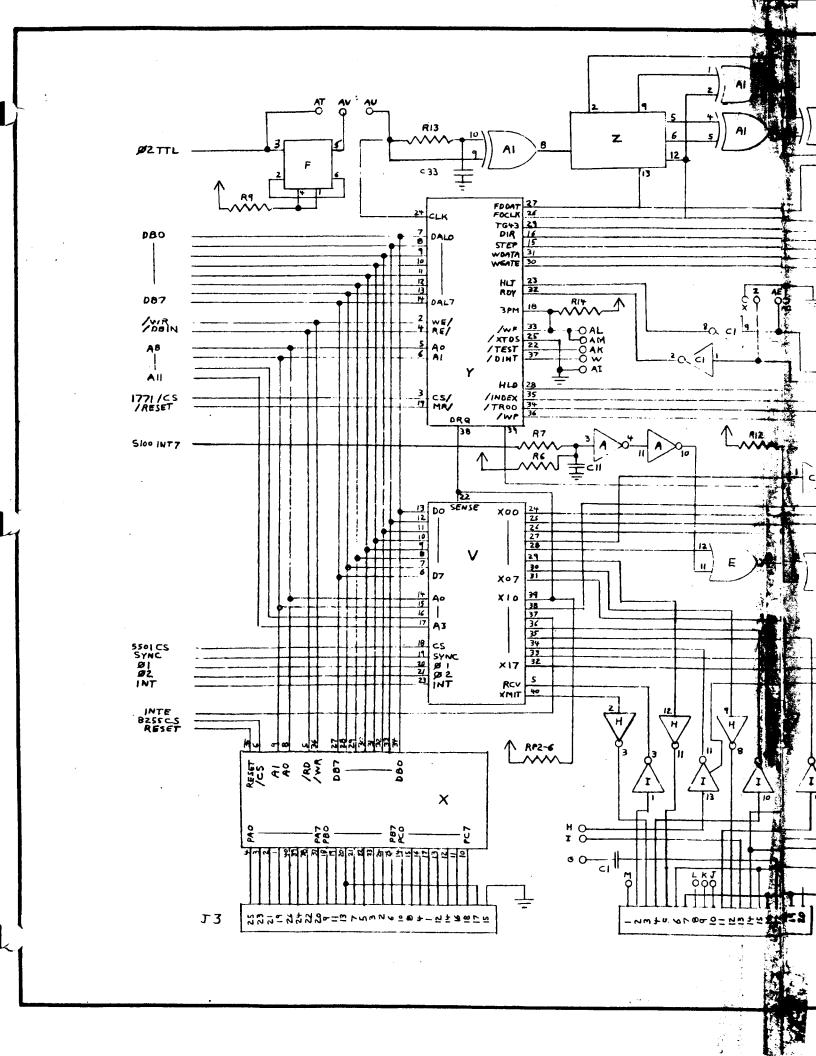
Do not use the interrupt system unless conversant with its action. It is reserved, along with TMS5501/FD1771 ports, mainly for system use. These devices are easy to use, but make suitable allowances for the system's use of them. The use especially of the 5501 timers, requires interplay with system interrupt masking routines.
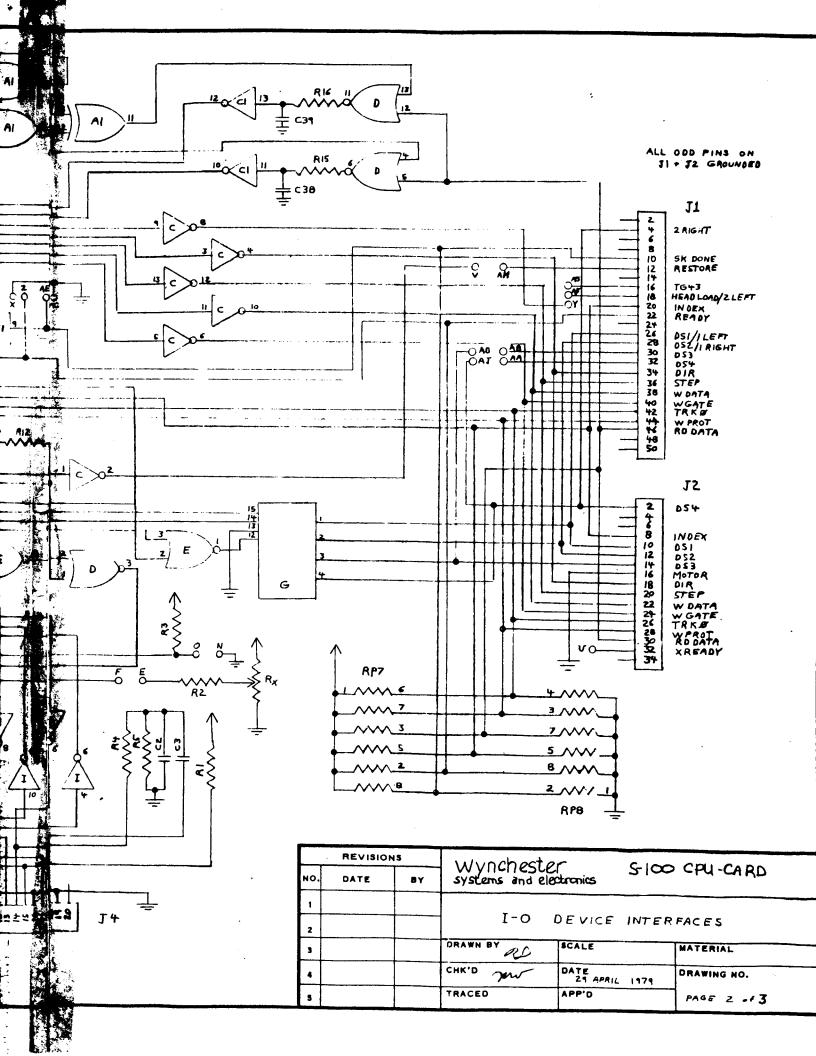
Be careful when debugging programs. This applies especially to programs from user's libraries or other installations. Many such programs make assumptions about safe practices which are valid only on the Author's original system. Remove disks from the computer during debugging unless they contain disk I/O and be prepared to use scratch disks as needed.

It cannot be over-emphasized that there is more than ample documentation contained in your manuals as well as many help files on your system disks (*.HLP). The small amount of time required to persue them will avoid potential frustration and enhance the usefulness of the W7993 system.

Schematic — S-100 CPU-CARD — C.P.U. + BUSS DEVICES

Top bus signal labels: DI8, DODSB/, DO7, DO8, ADDRDSB, AB0, AB7, AB8, AB15, X17/

Logic blocks: C, P, R, Q

Resistor packs: RP4, RP4-3, RP2-2, RP1-3, RP2-3, RP1-4, RP1-6, RP2-5, RP1-5, RP2-4, RP1-2, RP3-6

Right-side signal labels: AS AR, S100, DB0, DB7, A8, A11, /RESET, SYNC, RESET, 8255 CS, 1771/CS, INTE, 88IN, S501 CS, ØZ TTL, Ø2, Ø1, INT, /WR

Lower device: 2708/2716 W — D7 ... D0, A0 ... A9, PROGKS, CS, A10 — T R Q P S

R10, C20

REVISIONS			wynchester systems and electronics	S-100 CPU-CARD
NO.	DATE	BY		
1			C.P.U. + BUSS DEVICES	
2				
3			DRAWN BY · SCALE —	MATERIAL
4			CHK'D · DATE 13 July 1979	DRAWING NO.
5			TRACED · APP'D	PAGE 1 of 3

ALL ODD PINS ON
J1 & J2 GROUNDED

R16
C39
R15
C38

J1

2
4   2 RIGHT
6
8
10   SK DONE
12   RESTORE
14
16   TG43
18   HEAD LOAD/2 LEFT
20   INDEX
22   READY
24
26   DS1/1 LEFT
28   DS2/1 RIGHT
30   DS3
32   DS4
34   DIR
36   STEP
38   W DATA
40   WGATE
42   TRK Ø
44   W PROT
46   RD DATA
48
50

J2

2   DS4
4
6
8   INDEX
10   DS1
12   DS2
14   DS3
16   MOTOR
18   DIR
20   STEP
22   W DATA
24   W GATE
26   TRK Ø
28   W PROT
30   RD DATA
32   X READY
34

RP7

RP8

R3
R2
Rx
R4 R5 C2 C3 R1

J4

---- I.C. CONSIST ----

ES	DEVICE TYPE	POWER CONNECTIONS				
		+12	+5	GND	-5	-12
A	74LS14	—	14	7	—	—
A1	74LS86	—	14	7	—	—
B	74LS14	—	14	7	—	—
C	7406	—	14	7	—	—
C1	74LS14	—	14	7	—	—
D	74LS32	—	14	7	—	—
E	74LS02	—	14	7	—	—
F	74LS74	—	14	7	—	—
G	74LS145	—	16	8	—	—
H	1488	14	—	7	—	1
I	1489	—	14	7	—	—
J	3601	—	16	8	—	—
K	3601	—	16	8	—	—
L	74LS244	—	20	10	—	—
M	74LS244	—	20	10	—	—
N	74LS244	—	20	10	—	—
O	74LS244	—	20	10	—	—
P	74LS244	—	20	10	—	—
Q	74LS244	—	20	10	—	—
R	74LS244	—	20	10	—	—
S	74LS273	—	20	10	—	—
T	8224	9	16	8	—	—
U	8080A	28	20	2	11	—
V	TMS5501	3	2	4	1	—
W	TMS2716/2708	19	24	12	21	—
X	8255A	—	26	7	—	—
Y	1771E-1	40	21	20	1	—
Z	74LS393	—	14	7	—	—

---- SIP RESISTOR ARRAYS ----

(UNMARKED PINS NOT USED)

RP1

RP2

RP3

RP4

RP5

RP6

RP7

RP8

GND

50,

52 −16

C8
4.7/25

3
7912
0.47 1
C4 2
A

2 +16

C6
4.7/25

1
7812
0.1 3
C5 2 D

1.51 +8

C9
4.7/25

1
78.25
0.2 3
C10 2 C

3
79.05
0.47 1
C7 2 B

GND

−12 −5 +12 +5

——— ON-BOARD POWER SUPPLY ———

3 C1 4

5 C1 6

8
9 E 10

17 L 3

6 L 14

4 L 16

2 M 18

——— UNUSED DEVICES ———

REVISIONS			wynchester	S-100 CPU-CARD
NO.	DATE	BY	systems and electronics	
1			POWER SUPPLY - UNUSED DEVICES - SIP R's	
2				
3			DRAWN BY	SCALE	MATERIAL
4			CHK'D	DATE 13 July 1977	DRAWING NO.
5			TRACED	APP'D	PAGE 3 of 3

IN CASE OF TROUBLE

If error messages or other signs of trouble are encountered, track down their causes using standard troubleshooting techniques such as monitoring chip select signals on the various devices with a good triggered scope. However, before trying exotic techniques it is wise to go over the following check list of common problems since we have found that most problems are caused by one or more of these very simple omissions or errors:

>   -faulty cabling to I/O devices
>   -defective power supplies
>   -incorrectly addressed memory cards
>   -bad system disks

It is suggested that if any difficulty is encountered, these areas be investigated first since they require little or no test equipment to check and are frequently overlooked even by experienced technicians.

If another working system is available, the fastest and simplest way to trouble-shoot is by substituting boards and modules such as disk drives. Your Distributor may be of some assistance here.

If you need to diagnose your problem on a component level, you will have to trace the system operation step by step using a triggered scope, and a little common sense. The following check points may be very useful in locating the problem:

-measure the regulated power-supplies on the card at the outputs of the regulators
-ensure that the CPU clocks are of the correct rate and levels at the 8080A itself
-monitor the boot flip-flop operation with a scope. It should be low during reset and should remain low for about 10 to 15 microseconds after reset is released.
-monitor the 5501 chip select line to see if it is being accessed at the correct times.
-monitor the 5501 transmit data ouptut at the chip. If it is sending data but you are not receiving it on the terminal, the driver, cabling and terminal are suspect.
-monitor drive select, index and read data lines during the boot operation. These signals usually point up incorrect drive jumpering very quickly.

MEMORY

The memory board is a high performance dynamic RAM board using state-of-the-art
MOS dynamic memory devices. It is configured to have a memory capacity of 64K
bytes of memory using the MK 4116 (16,384x1 MOS dynamic RAM) memories. An
eight position DIP switch provided for positioning memory on any 8K or 16K
boundary. Other features of the memory board include:

    1. Bank selectable write protect
    2. Phantom output disable or manual switch selectable output disable
    3. Typical power dissipation of 5 watts
    4. S-100 Bus Structure

The board is implemented on a single 5.25" x 10.0" x 0.65" printed circuit
board. The board requires three DC voltages at levels of +7V to +10V, +14V to
+18V, and -14V to -18V DC.

As installed, the W7993's memory card is configured to support the CP/M opera-
ting system. For operation under CP/M, cards are installed so that they provide
continuous RAM memory starting at location 0 and extending to the highest
address. No "phantom" provisions are required, board control logic. 64K of
memory is installed in standard systems.

For maximum flexibility, high-speed memory is used for all RAM cards. The
disk driver software supplied will operate with data RAM requiring up to one
wait state but if slower memory is used, or if it is desired to place disk
I/O code into slow RAM memory (instead of the EPROM supplied) the software
will need to be rewritten. Control signals appear on the bus that allow
operation with dynamic RAM cards using transparent refresh strapped for 8080
mode. Avoid additional memory cards which do not emulate those in the current
system.

Memory Capacity	65,536 bytes (16K RAM)
Memory Access	375 ns max.
Memory Cycle	500 ns min.
Interface Levels	TTL compatible
Power (2 µs memory cycle)	+7V to +10V @ 400 mA (max.) +14V to +20V @ 200 mA (max.) -14V to -20V @ 30 mA (max.)

RAM MEMORY FUNCTIONAL DESCRIPTION

Memory Array - The memory array consists of 16K dynamic random access memory elements. Each 16K has a 16,384 x 1 bit capacity. The 16K RAMS each contribute one bit to an addressable location. The total storage capacity of the memory is 65,535 bytes.

Memory Decode and Control - The memory decode and control section is responsible for generating the timing signals for the memory decode and control section is generated by a TTL compatible delay line.

Address Multiplexer - The address multiplexer is responsible for taking the address bits from the address bus buffers and multiplexing the proper row and column address into the memory array under control of the memory decode and control section.

Data Buffers - The data buffers, controlled by the memory decode and control section, isolate the memory array from the data bus.

Address switch positions for the 64K board

```
                                          Set 1-4 to off position
       ┌──────────┐
       │ Not used │
  on   │┌────────┐│
       ││ 1 2 3 4││ 5 6 7 8
       └┴────────┴┴────────┘
  off                │ │ │ └── C000-FFFF   (Bank 3)
                     │ │ └──── 8000-BFFF   (Bank 2)
                     │ └────── 4000-7FFF   (Bank 1)
                     └──────── 0   -3FFF   (Bank 0)
```
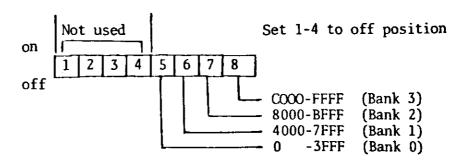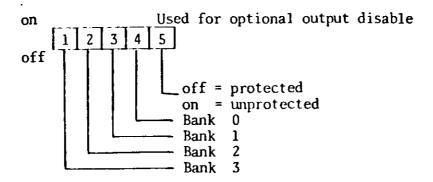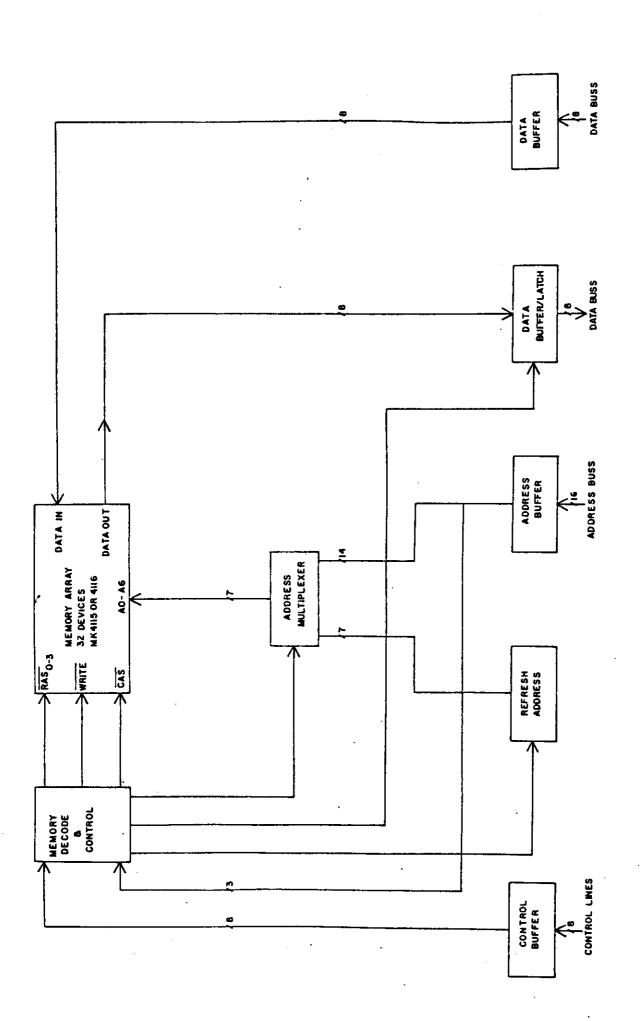
Figure 4-2

BANK SELECTABLE WRITE PROTECT SWITCH

The positions for the bank selectable write protect switch.

```
  on               Used for optional output disable
       ┌──────────┐
       │ 1 2 3 4 5│
  off  └──────────┘
         │ │ │ │ └── off = protected
         │ │ │ │     on  = unprotected
         │ │ │ └──── Bank  0
         │ │ └────── Bank  1
         │ └──────── Bank  2
         └────────── Bank  3
```

DATA BUFFER

DATA BUSS

Wynchester Systems
and Electronics Inc.

DRAWN JAA   DATE 8/11
CKD
APPD
RLSD
SCALE NONE
SHEET 1 OF 1
SIZE A   "0"
RE VISION E

DATA IN

DATA OUT

MEMORY ARRAY
32 DEVICES
MK 4115 OR 4116

A0-A6

RAS 0-3

WRITE

CAS

MEMORY
DECODE
&
CONTROL

ADDRESS
MULTIPLEXER

/7

/14

/7

DATA
BUFFER/LATCH

/8

DATA BUSS

ADDRESS
BUFFER

/16

ADDRESS BUSS

REFRESH
ADDRESS

/3

CONTROL
BUFFER

/8

CONTROL LINES

/8

/8

/8

```
ADDR  OBJECT        ST # SOURCE STATEMENT

                    0001 ; TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                    0002 ;
                    0003 ; THIS IS A MODIFIED ADDRESS STORAGE TEST WITH
                    0004 ; AN INCREMENTING PATTERN
                    0005 ; .
                    0006 ; 256 PASSES MUST BE EXECUTED BEFORE THE MEMORY
                    0007 ; IS COMPLETELY TESTED
                    0008 ;
                    0009 ; IF AN ERROR OCCURS, THE PATTERN WILL BE STORED
                    0010 ; AT LOCATION 002C'H AND THE ADDRESS OF THE
                    0011 ; ERROR LOCATION WILL BE STORED AT '002D'H
                    0012 ; AND '002E'H.
                    0013 ;
                    0014 ; THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
                    0015 ; SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                    0016 ; MEMORY SIZE TESTED
                    0017 ;
                    0018 ; TOP OF MEMORY TO
                    0019 ; BE TESTED                          VALUE OF EPAGE
                    0020 ;
                    0021 ;     4K                                  '10'H
                    0022 ;     8K                                  '20'H
                    0023 ;    16K                                  '40'H
                    0024 ;    32K                                  '80'H
                    0025 ;    48K                                  'C0'H
                    0026 ;    64K                                  'FF'H
                    0027 ;
                    0028 ; THE PROGRAM IS SET UP TO START TESTING AT
                    0029 ; LOCATION '002F'H.  THE STARTING ADDRESS FOR THE
                    0030 ; TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                    0031 ; '0003'H-'0004'H AND '0011'H-'0012'H.
                    0032 ;
                    0033 ; TEST TIME FOR A 16K BY 8 MEMORY IS APPROX. 4 MIN.
                    0034 ;
                    0035 ;        PSECT    ABS
   >0000            0036 ;        ORG      0000H
   0000  0600       0037 ;        LD       B, 0     ;CLEAR B PATRN MODIFIER
                    0038 ; LOAD UP MEMORY
   0002  212F00     0039 ; LOOP:  LD       HL, START; GET STARTING ADDR
   0005  7D         0040 ; FILL:  LD       A,H      ; LOW BYTE TO ACCM
   0006  AC         0041 ;        XOR      H        ; XOR WITH HIGH BYTE
   0007  A8         0042 ;        XOR      B        ; XOR WITH PATTERN
   0008  77         0043 ;        LD       (HL),A   ; STORE IN ADDR
   0009  23         0044 ;        INC      HL       ; INCREMENT ADDR
   000A  7C         0045 ;        LD       A, H     ; LOAD HIGH BYTE OF ADDR
   000B  FE10       0046 ;        CP       EPAGE    ; COMPARE WITH STOP ADDR
   000D  C20500     0047 ;        JP       NZ,FILL  ; NOT DONE, GO BACK
                    0048 ; READ AND CHECK TEST DATA
   0010  212F00     0049 ;        LD       HL, START; GET START ADDR
   0013  7D         0050 ; TEST:  LD       A, L     ; LOAD LOW BYTE
   0014  AC         0051 ;        XOR      H        ; XOR WITH HIGH BYTE
   0015  A8         0052 ;        XOR      B        ; XOR WITH MODIFIER
   0016  BE         0053 ;        CP       (HL)     ; COMPARE WITH MEMORY LOC
   0017  C22500     0054 ;        JP       NZ, FXIT ; ERROR EXIT
   001A  23         0055 ;        INC      HL       ; UPDATE MEMORY ADDR
   001B  7C         0056 ;        LD       A, H     ; LOAD HIGH BYTE
   001C  FE10       0057 ;        CP       EPAGE    ; COMPARE WITH STOP ADDR
   001E  C21300     0058 ;        JP       NZ, TEST ; LOOP BACK
```

```
ADDR   OBJECT      ST # SOURCE STATEMENT

0021   04          0059            INC      B        ; UPDATE MODIFIER
0022   C30200      0060            JP       LOOP     ; RST WITH NEW MODIFIER
                   0061 ; ERROR EXIT
0025   222D00      0062    EXIT:   LD       (BYTE), HL; SAVE ERROR ADDRESS
0028   322C00      0063            LD       (PATRN), A ; SAVE BAD PATTERN
002B   76          0064            HALT               ; FLAG OPERATOR
>002C              0065    PATRN:  DEFS     1
>002D              0066    BYTE:   DEFS     2
002F   2F00        0067    START:  DEFW     $
0031   3100        0068            DEFW     $          ; PLACE FOR FIRST ADDR
>0010              0069    EPAGE:  EQU      10H        ; SET UP FOR 4K TEST
                   0070            END
```

ERRORS=0000

MEMORY REMAP

This modification allows use of up to 60K of RAM memory.

REVISED MEMORY MAP:

0F800h - 0FFFFh	2716/2708	(read only)
0F400h - 0F7FFh	1771	(read/write)
0F300h - 0F3FFh	5501 Stat in	(read only)
0F200h - 0F2FFh	5501 RST # in	(read only)
0F100h - 0F1FFh	5501 Parallel in	(read only)
0F000h - 0F0FFh	5501 Rx in	(read only)

REVISED 10 MAP:

0F0h - 0FFh	5501 as 10 ports	(read/write)
0ECh - 0EFh	8255 as 10 ports	(read/write)

MODIFICATIONS TO SELECT PROM1:

ODD locations are Memory mapped, EVEN are 10 mapped.

        Only the following 32 bytes need revision:

```
ADR70:  DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,PPI1
        DB      UART,UART,FDCC,UART,EPROM,UART,EPROM,UART

ADRFO:  DB      NONE,NONE,NONE,NONE,NONE,NONE,NONE,PPI1
        DB      UART,UART,FDCC,UART,EPROM,UART,EPROM,UART
```

MODIFICATIONS TO SOFTWARE:

The following points should be noted re software compatibility:

        -The 5501 is now at a different base address (was E0, now F0)
        -Only the first 4 ports of the 5501 may now be memory accessed
        -The 1771 may now ONLY be accessed as memory
        -The 1771 is now at a different base address (was F0, now F4)
        -The EPROM may no longer be accessed as an 10 device
        -The 8255 may now ONLY be accessed as an 10 device
        -The 8255 is now at a differnet base address (was F4, now EC)

5¼" FLEXIBLE DISK DRIVES

Introduction

This specification describes the W7993-320 series of 5¼" flesible disk   X
drives. These units are intended for mini or microcomputer applications
which require random access disk storage at low cost.   These drives
are designed for single density (FM) or double density (MFM or M²FM)
operation at standard data densities.

Each unit consists of a drive mechanics assembly and electronics circuit
board. TRhe drive provides an industry compatible interface for attachment
to an external controller. Up to four drives can be connected to the
controller interface.

<p style="text-align:center">Table 1   Basic Model Numbers</p>

Models	Heads/Drive	Tracks/Surface
320 Mod I	1	35
* 320 Mod II	1	77-100 TPI *
320 Mod III	2	35
320 Mod IV	2	77
320 Mod I	1	70
320 Mod VI	2	70

(X to the right of 320 Mod I / 70 row)

Since no data decoding circuits are provided in the 320 drive the format
and encoding schemes are completely determined by the host controller.
Thus, any combination of hard/soft sector format and FM, MFM, M²FM
encoding schemes may be used at standard densities depending on system
requirements.

Compatibility

Media The 320 series drives use an industry compatible 5¼" diskette
which is available in unsectored, 10 sector, and 16 sector formats.

Interchange The 320 Mod I and Mod III provide mechnaical and data transfer
characteristics identical to the Shugart SA400 and SA450, respectively.
When properly formatted, diskettes are fully interchangeable with the
SA400/SA450 or equivalent drives.

Interface The external signal interface is pin and plug compatible
with the SA400/SA450. Additional interface lines and also provided.

* W7993-2 Series computers are provided with Series 320 Mod II Drives.

Physical Specification

Parameter	Model 320 Drive
Environment	
Ambient Temp.	50°–105°F
Rel. Humidity	20%–80% (No Condensation)
Mechanical	
Height (overall)	3-3/8"
Width (overall)	5-7/8"
Depth (overall)	8-1/2"
Weight	3.9 lbs.
Dissipation	
Standby	8 watts
Operating	16 watts

Reliability Specification

MTBF	8500 hrs.
PM	Not required
MTTR	30 mins.
Error Rate	
Soft Read Errors	1 in 10^9 bits read
Hard Read Errors	1 in 10^{12} bits read
Seek Errors	1 in 10^6 seeks
Media Life	
Passes per track	3.0×10^6
Insertions	30,000 $^+$

General Description

The 320 consists of a drive mechanism and a drive electronics PCB assembly.
These combine together to perform the following functions under the
control of the host system:

Interrupt and generate control signals

Position the read/write head on the desired track

Read and write Data

Disk Drive

Basic Mechanism

The diskette is inserted through the access door on to a registration
hub which centers the media on the spindle shaft. When the door is
closed, the media is clamped and rotated by the spindle motor at the
rated speed. A mechanical interlock prevents the door from being closed
if a diskette is not inserted or is not correctly seated. A microswitch
senses when the door is closed.

Positioning Mechanism

A stepper motor/lead screw combination is used to position the head
at the desired track. The head is attached to a carriage mechanism
which moves along a radial line with respect to the media when the lead
screw is rotated. Each user step input increments the stepper and causes
the head to move one track positon in the specified direction.

Read/Write Head

This consists of a single or dual read/write head assembly with trailing
tunnel erase gaps. The heads are designed to provide maximum signal
transfer to and from the diskette with a minimum of wear. When the
head load solenoid is actuated, ^(optional no head–load–solenoid when
the door is closed) a pressure pad (or the opposing head) moves the
media against the head surface allowing read or write data transfers
to take place. During write operations the tunnel erase gap trims the
write data to produce an erased area between adjacent tracks. This
provides a mechanical tolerance which allows diskettes to be interchanged
with those from other drives without affecting data reliability.

Sector/Indes Sensor

An LED/photosense circuit is used to detect the occurrence of the sector
and index holes punched in the diskette media.   The sector holes divide
the diskette surface into equal angular segments and are used by the
controller for formatting purposes. The index hole is located midway
between the sector holes for the last sector and sector 0.

Track Ø Sensor

The track Ø microswitch detects when the read/write head is positioned at track Ø. After power on, the initial position of the R/W head with respect to the data tracks is unknown. The user must first initialize the positioner mechanism by stepping out until track Ø is detected. A similar procdure is used if a positioning error is suspected.

Write Protect

The diskette write protect status is determined by a cutout along one edge of the diskette jacket which is sensed by a microswitch in the drive mechanism. If the cutout is covered, the write circuits are disabled and the diskette cannot be accidently overwritten. When the cutout is uncovered, writing is allowed. The write protect status is communicated to the host system via an interface line.

Drive Electronic PCB Assembly

This contains the control, read/write, and interface electronics as follows:

    (a) Drive select logic

    (b) Drive ready logic

    (c) Sense amps. and status logic

    (d) Positioner control logic and drivers

    (e) Write amp. and trim erase circuit

    (f) Read amp. and peak sensor circuit

    (g) Interface drivers

Controls and Indicators

Select Indicator

An LED on the front bezel is illuminated when the drive is selected by the host system.

Electrical Interface

Signal Interface

Signal Connector J1 provides the interface between the 320 drive and the host controller. This is a 34 pin edge connector located on the electronics assembly. Up to four 320 drives can be daisy chained on this interface.

Either flat cable or twisted pair may be used with a maxmim cable length of
20 feet. The mating connectors are: Scotchflex P/N 3463-0001 or equivalent.
The connector is keyed between pins 4 and 6.

Figure 3 lists the interface lines and figure 4 provides a summary of
the electrical characteristics of the interface.

Termination resistors for the input lines are provided on the Drive
Electronics PCB assembly. They should be installed in the last module
only.

The interface consists of 11 input lines and 5 output lines. All lines
are low true with the folloiwng logic levels:

True	=	Logic Zero	=	0-0.4V
False	=	Logic One	=	2.5-5.25V

Input Lines

MTRN Motor on

This line provides the ability to simultaneously enable or disable the
spindle drive motor for all disk drives in the system.

The spindle motor is controlled by the logical AND function of MTRN
and the door closed microswitch. A mechanical interlock in the drive
mechanism prevents the access door from being closed unless a diskette
is inserted and is correctly seated on the registration hub.

When MTRN goes true, those drives with the power on and a diskette inserted
and the access door closed are energized and begin accelerating to operating
speed. The remaining drives are not affected. After an acceleration
delay of 1.5 sec., (.5 secs for no head-load-solenoid option drives)
the active drives go ready (RDY true) and are available for use by the
host system.

If the access door is opened, the drive goes not ready and decelerates
to a halt. If the door is closed again, the drive accelerates and goes
ready as described above. When MTRN goes false, all disk drives in
the system go not ready and decelerate to a halt.

As an alternate to this, the user may tie MTRN permanently true and
make use of the door switch only for motor control (for no head-load-
solenoid option MTRN should be disabled whenever the drive is not accessed).
In either case, it is generally recommended not to leave a diskette running for
long periods of time when not in use, especially with the head loaded.

DSI-4 Drive Select Lines

These four lines select a specific drive for connection to the controller.
When selected, a drive responds to signals on the input lines, and the
output lines are enabled.

The address of each drive is determined by a jumper connection on
the Drive Electronics PCB to one of the four select lines. Not more
than one select line may be true at a time. All interface lines except
MTRN and HDLD are internally gated with drive selected.

HDLD Head Load (optional)

In the normal mode of operation the read/write head is automatically
loaded/unloaded from the diskette media when the drive is selectred/deselected.   ╳
A load time of 75 ms should be allowed before a read or write operation
is performed.

For systems requiring rapid access to different drives the head load
time can be eliminated by use of the HDLD line. When HDLD is true (low)
the heads on all active drives (pwer on and door closed) in the system
are simultaneously loaded. Different drives can be accessed without
delay. In the case of no head-load-solenoid option, the head(s) are
loaded when the door is closed and this line is ignored.

It is recommended that the system design leaves all heads unloaded or
motor disabled when there is no disk activity.

DIRN Step Direction

This line specifies the direction of motion when a STEP command is issued.

True (low) = STEP IN   toward center   ;   increase track number
False (high) = STEP OUT away from center   ;   decrease track number

STEP Step Command

Each pulse on this line causes the positioner to move one track position
in the direction specified by DIRN. Motion is initiated on the trailing
(positive) edge of each signal pulse. The minimum pulse width is 250 ns
and any change in DIRN must be at least 250 ns before the trailing edge
of STEP.

The minimum time between consecutive STEP commands is 30 ms when moving
in the same direction, or 40 ms when changing direction. A period of
40 mn must be allowed after the last STEP command before attempting   ╳
a read or write operation.

STEP commands are not recognized when a write operation is in progress
(WRT true). If a STEP OUT command is issued at track 0, the positioner
will encounter a mechanical stop and remain at track 0.

Figure 5 shows the timing for the DIRN and STEP input lines.

WDA Write Data

This line carries encoded write data to be recorded on the diskette.
The leading (negative) edge of each pulse causes the current through
the write head to be reversed, thereby writing a flux transition on
to the media. Pulse width should be between 200 ns and 2 us. WDA is
enabled when WRT is ture, provided that the diskette is not write protected
adn a STEP command is not in progress.

The leading edge of each pulse should be timed to within 0.1% of the data cell time as shown in Figure 7.

It is recommended that WDA be disabled at the controller when a read operation is in progress.

WRT Write Gate

This line controls the read/write mode of the selected drives. The write circuits are enabled when WRT is true provided that the diskette is not write protected and a STEP command is not in progress. The data appearing on WDA is now recorded on to the diskette. On conclusion of a write operation, WRT false disables the write circuits.

The trim erase head is energized 425 us after the leading edge of WRT and de-energized 350 us after the trailing edge of WRT. The read circuits are disabled during WRT true, and during the trim erase period for MOD I and MOD II units. STEP commands are disabled when WRT is true.

Note that the first and last data transition to be written may suffer excessive peak shift.

HSLT Head Select

This line selects either the lower or upper head (disk surface) for MOD III and MOD IV drives as follows:

                          False (high) = Lower Head
                          True (low)   = Upper Head

Output Lines

RDY Ready

The RDY line indicates the operational status of the selected drive. It is true when all of the following conditions are met:

    a) Power on and D.C. supplies established
    b) MTRN True
    c) Diskette fully inserted and the access door closed
    d) 1.5 sec (.5 sec for no head-load-solenoid option) motor start
        delay timed out (i.e., at speed)
    e) Drive selected.

The controller should test the state of RDY before performing a read or write operation.

SECP Sector/Index Pulse

This line goes true for 4 + 1 ms each time a sector or index hole is detected in the selected diskette. The leading (negative) edge must be used as the time reference.

The SECP output is not valid until the diskette has reached operating speed (RDY true). Figure 6 shows the timing for a 16 sector diskette rotating at 300 RPM.

WPT Write Protect

WPT indicates the write protect status of the selected diskette. This status is determined by a cutout along one edge of the diskette jacket.

When the cutout is covered WPT is true and the write circuits are internally disabled irrespective of the state of WRT. The diskette cannot be accidentally overwritten.

When the cutout is uncovered WPT is false and the write operations are allowed.

RDA Read Data

This line transmits composite read data from the selected drive to the controller. The data consists of a series of low true pulses; one for each flux transition recorded on the media. The pulse width is 0.7 ± 0.4 us and the leading (negative) edge of each pulse should be used as the time reference.

This output is inhibited during a write operation (WRT true), and also during the trailing trim erase delay (850 us) for Mod I and Mod II units. A further 100 us read amplifier recovery time is required before the output data is valid.

The amount of peak shift experienced by the read data is dependent on the data pattern, the encoding method, and the data transfer rate. Figure 8 shows the worst case peak shift conditions for single density and double density (MFM) encoding at the recommended data transfer rates. When used with properly designed decoding electronics, the specified data reliability rate is met for both single and double density without the need for time precompensation of the write data. If precompensation is included in the controller, a reduction in peak shift and a corresponding increase in decoding margins can be expected. The amount of precompensation should be in the range 8-10% of a data cell, and preferably be used on the inner tracks only ($\geq$ track 44).

SPECIFICATION

W7993-401 - POWER SUPPLY

A specially designed power supply is provided for the S100 cards and for the disk drives in the system. Most S100 cards require that the supplies be within the following range:

        PIN 1,51   8.5 to 10.0 Volts DC max 5% ripple
        PIN 2   15.0 to 18.0 volts max 5% ripple
        PIN 52   -15.0 to -18.0 volts max 5% ripple

Use of higher voltages may result in overheating of regulators. Lower supply voltages may cause dropout of regulators. Consult the manuals for S100 cards to make sure that they are happy with the supply as some cards with analog I/O require more critical supplies for pins 2 and 52. With supplies in the above range, the W7993's cards should draw less than 1.2 Amps from the 8 volt supply, less than 0.2 amps from the +18 volt supply and less than 0.1 amp from the -18 volt supply. Typical boards draw considerably less. Consult the manual for your disk drive to determine its power requirements. The 24 volt supply required by most disk drives is derived by the specially designed transformer and rectifier since this supply often introduces severe transients into a system.
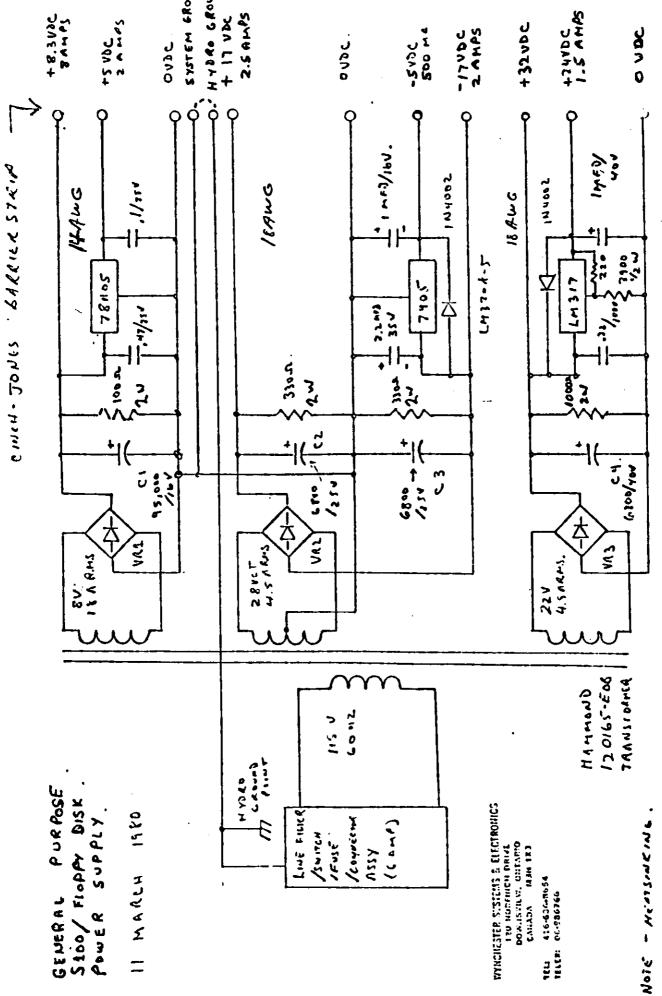
The power supply's output is as follows:

                        + 8.3 VDC   8 AMPS
                        + 5.0 VDC   2 AMPS
                        +17.0 VDC   2.5 AMPS
                        - 5.0 VDC   500 MA
                        -17.0 VDC   2 AMPS
                        +32.0 VDC   1.5 AMPS
                        +24.0 VDC   1.5 AMPS

For maximum immunity against power transients the power supply has time constants in excess of 50 ms.

The supply wiring is designed to handle the currents involved without significant drops, even if future cards are added.

The power supply is modular and housed in its own casing to facilitate ease of service.

GENERAL PURPOSE
S100/ FLOPPY DISK.
POWER SUPPLY.

11 MARCH 1980

CINCH - JONES · BARRIER STRIP

+8.3VDC 8 AMPS
+5 VDC 2 AMPS
0VDC
SYSTEM GROUND
HYDRO GROUND
+17 VDC 2.5 AMPS
0VDC
-5VDC 500 MA
-17VDC 2 AMPS
+32VDC
+24VDC 1.5 AMPS
0 VDC

14AWG
78H05
.1/25V
100Ω 2W
.47/25V
C1 35,000/16V
VR1
8V 18A RMS

18AWG
330Ω 2W
C2 6800/25V
VR2
28VCT 4.5 AMPS

.1MFD/16V
7905
2.2MFD 35V
330Ω 2W
C3 6800/25V
1N4002
LM320T-5

18AWG
1MFD/40V
LM317
220
2100 1/2W
.22/100
100Ω 2W
C4 6800/40V
1N4002
VR3
22V 4.5AMPS

HAMMOND
120165-E06
TRANSFORMER

115 V 60HZ

HYDRO GROUND POINT

LINE FILTER /SWITCH /FUSE /CONVENIENT ASSY (6 AMP)

WYNCHESTER SYSTEMS & ELECTRONICS
120 NORFINCH DRIVE
DOWNSVIEW, ONTARIO
CANADA   M3N 1X3

TEL: 416-636-8054
TELEX: 06-986766

NOTE - HEATSINKING.

78H05 DISSIPATES 12 WATTS MAX
7905 DISSIPATES 5 WATTS MAX
LM ? DISSIPATES 9 WATTS EACH M

QTY		PG	
1	2	804	Corcom 6J1
or			or
1	1	804	Corcom 6EF1 or 6EF2
1	1	736	Littlefuse 348655 Fuseholder
5	10	731	AGC-3 fuse
1	1	894	Belden 17250 Line Cord
1	1	466	Cinch Jones 14-541 Terminal Strip
			or 15-541, 16-541 et c.
1 pkg 100		906	Panduit Lug
100 pc			PV18-6F-C or PV18-6FX-C
2	2	213	Philips Ca/ 431 CR F3400 + 3400 - see substitutio
1	1	213	Philips Ca/ 431 CR G3400 + 3400 - see substitutio
3	3	213	Philips Mounting Clamps
1	2	75	Motorola MDA3501 Bridge
2	4	97	Varo VJ248X Bridge
			or VJ248X
2	4	53	National LM317 K regulator
1	2	48	Fair 78H05 KC
1	2	51	National LM320K-5
4	6	381	Keystone 4725 TO3 mounting kit
1	1	238	Mallory CG953 U O 15X4C
1	1	239	Mallory mounting clamp

∞ CRL must $= > 20$

≈ 740 $CR_L = 20$ $RL = .8\wedge$ for 8V supply
        $CRl = 20/740$ $RL = 6.8\wedge$ for +17V supply
        $C = 1/(37xRl)$ $RL = 6.8\wedge$ for -17V
                              $RL = 9.6\wedge$ for 24V 2.51

RECOMMENDED COMPONENTS   (or equivalent)

YR1	Motorola	MDA 3501	100 PIV @ 35A	(400 Surge)
VR2	Varo	VL 248	200 PIV @ 15A	(100 Surge)
VR3	Varo	VL 248	200 PIV @ 15A	(100 Surge)
C1	Mallory	CG953U015X4C 95000 MFD/15V		Computer Grade
C2	Phillips	431CR/F3400+3400 DUAL 3400 MFD/25V Parallelled		
C3	Phillips	431CR/F3400+3400 DUAL 3400 MFD/25V Parallelled		
C4	Phillips	431CR/G3400+3400 DUAL 3400 MFD/40V Parallelled		

SUBSTITUTE

C4	Sprague	36DX 7200-50WVDC	7534L-441804
C2-3	Nippon	CEEW 25V 13000 PFO	

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accomodates the interface signals from most drive manufactures. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.
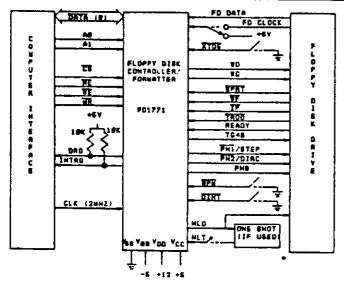
The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS
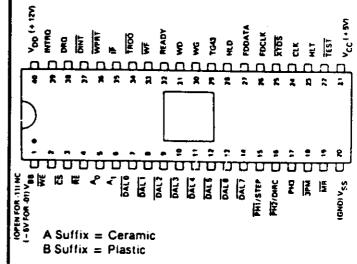
o   FLOPPY DISK DRIVE INTERFACE

o   SINGLE OR MULTIPLE DRIVE

    CONTROLLER/FORMATTER

o   NEW MINI-FLOPPY CONTROLLER

FEATURES

o   SOFT SECTOR FORMAT COMPATIBILITY

o   AUTOMATIC TRACK SEEK WITH VERIFICA—TION

o   READ MODE
    Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
    Selectable 128 Byte or Variable Length Record

o   WRITE MODE
    Single/Multiple Record Write with Automatic Sector Search
    Entire Track Write for Diskette Initialization

o   PROGRAMMABLE CONTROLS
    Selectable Track to Track Stepping Time
    Selectable Head Settling and Head Engage Times
    Selectable Three Phase or Step and Direction and Head Positioning Motor Controls

o   SYSTEM COMPATIBILITY
    Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and status
    DMA or Programmed Data Transfers
    All Inputs and Outputs are TTL Compatible

o   No — 5VDC Power Supply Required on — 11 version

MARCH 1978
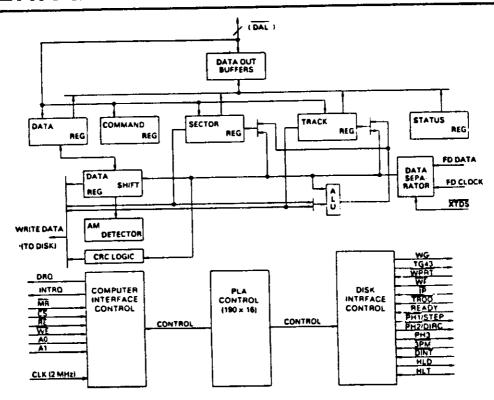
FD1771 SYSTEM BLOCK DIAGRAM
FIG 1

A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

FD1771 BLOCK DIAGRAM
FIG 3

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on Page 2. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read,

Write, and Verify operations. The Track Register car be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector - The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control - All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0		READ (RE)	WRITE (WE)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing, (may be 1.0 MHz for mini floppy.)

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three Phase Motor or a Step-Direction Motor through the device interface. When the 3PM input is connected to ground the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2 and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input 3PM open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds width. The Phase 2 pin PH2 becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 µs prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track

Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

TABLE 1
STEPPING RATES

r1	r0	1771-X1 CLK=2MHZ TEST=1	1771-X1 CLK=1MHZ TEST=1	1771 or-X1 CLK=2MHZ TEST=0	1771 or-X1 CLK=1MHZ TEST=0
0	0	6ms	12ms	*APPROX. 400us	*APPROX. 800us
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 KHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 KHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 KHz data clock. The 500 KHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator (XTDS) INPUT. When the Read Data input makes a high to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8 bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic o in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register data will be shifted serially through the Write Data (WL) output. Interlaced with each bit of data is a positive clock pulse of 0.5 µsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in table 2.

COMMAND SUMMARY*

						BITS			
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2

* = Shown in true form.

FLAG SUMMARY

TYPE 1

h = Head Load Flag (Bit 3)
  h=1, Load head at beginning
  h=0, Do not load head at beginning

V = Verify flag (Bit 2)
  V=1, Verify on last track
  V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
  Refer to Table 1 for rate summary

u = Update flag (Bit 4)
  u=1, Update Track register
  u=0, No update

TABLE 3

TYPE II

m = Multiple Record flag (Bit 4)
  m =0, Single Record
  m =1, Multiple Records

b = Block length flag (Bit 3)
  b =1, IBM format (128 to 1024 bytes)
  b =0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)
  a_1a_0 =00, FB (Data Mark)
  a_1a_0 =01, FA (User defined)
  a_1a_0 =10, F9 (User defined)
  a_1a_0 =11, F8 (Deleted Data Mark)

TABLE 4

TYPE III

s = Synchronize flag (Bit 0)
  s=0, Synchronize to AM
  $\bar{s}$=1, Do Not Synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)
  I_0=1, Not Ready to Ready Transition
  I_1=1, Ready to Not Ready Transition
  I_2=1, Index Pulse
  I_3=1, Immedate interrupt
E = Enable HLD and 10 msec Delay
  E=1, Enable HLD, HLT and 10 msec Delay
  E=0, Head is assumed Engaged and there is no 10 msec Delay.

TABLE 5

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK STEP, STEP-IN, AND STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

The type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt, (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U = 1, the track register is updated by one for each step. When U = o, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 (TROO) input is sampled. If TROO is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TROO is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r1r0 field are issued until the TROO input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the
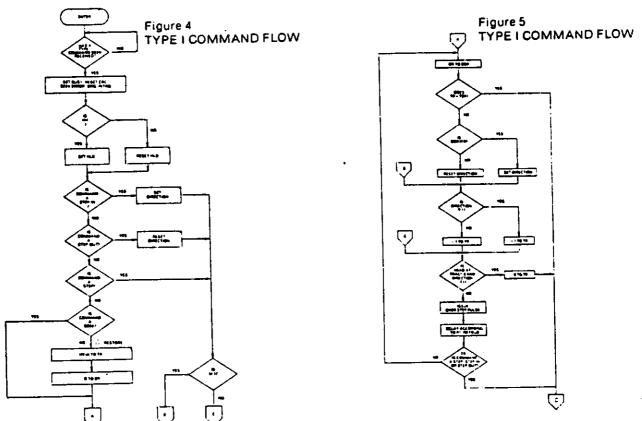
TROO input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Figure 4
TYPE I COMMAND FLOW

Figure 5
TYPE I COMMAND FLOW
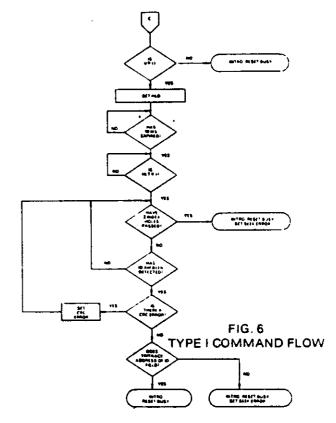
STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on the Track Register is incremented by one. After a delay determined by the r₁ r₀ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

FIG. 6
TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1771 compares the Track Number of the ID field with the Track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1771 must find an Id field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
			ID FIELD						DATA	FIELD		

IDAM = ID Address Mark — DATA=(FE)₁₆ CLK = (C7)₁₆
Data AM = Data Address Mark — DATA=(FB, F9, FA, or FB), CLK = (C7)₁₆

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128 x 2^n where n - 0,1,2,3.

For b = 1
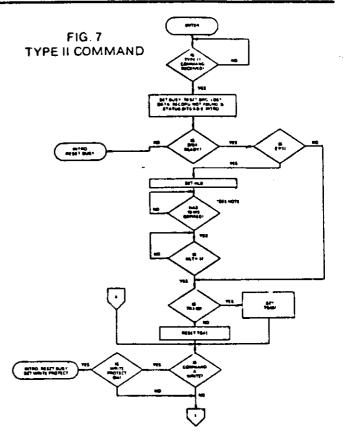
Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:
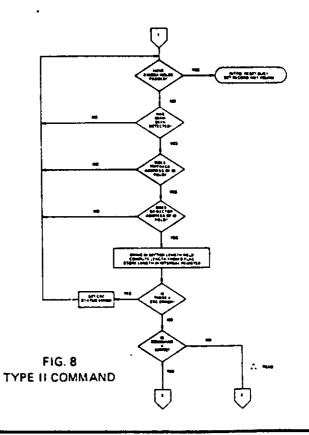
For b = 0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the type II commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = o a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1 , multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

FIG. 7
TYPE II COMMAND

FIG. 8
TYPE II COMMAND
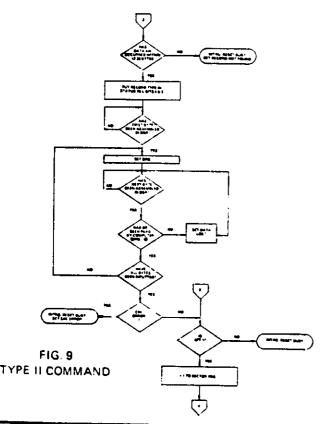
READ COMMAND

Upon receipt of the Read command, the head Is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been Inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

FIG. 9
TYPE II COMMAND
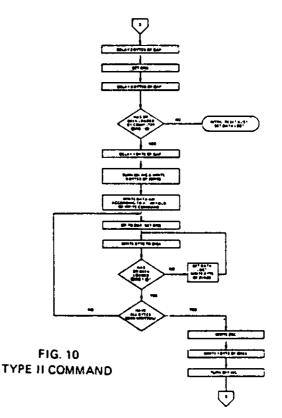
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a1a0field of the command as shown below:

a1	a0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The FD1771 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

FIG. 10
TYPE II COMMAND

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the BUSY Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit O (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon recieving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR When needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command will not execute if the $\overline{DINT}$ input is grounded; instead the Write Protect Status bit is set and the interrupt is activated. Note that one F7 pattern generates 2 CRC characters.
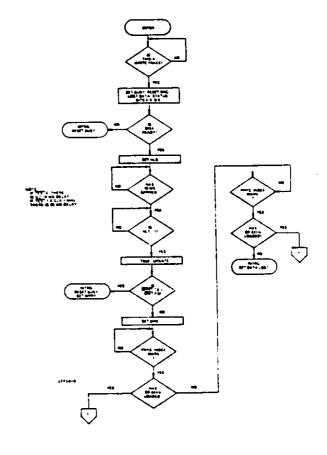
FIG. 11
TYPE III COMMAND
WRITE TRACK

FIG. 12
TYPE III COMMAND
WRITE TRACK

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt
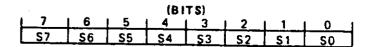
NOTE: If $I_0I_3=0$, there is no Interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the BUSY Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the BUSY Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

			(BITS)				
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

STATUS REGISTER SUMMARY
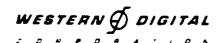
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 6

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: In indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK
Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD 1771 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS · 128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
6	00
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	00 or FF
247**	00 or FF

*   Write bracketed field 26 times
** Continue writing until FD1771 interrupts out. Approx. 247 bytes.
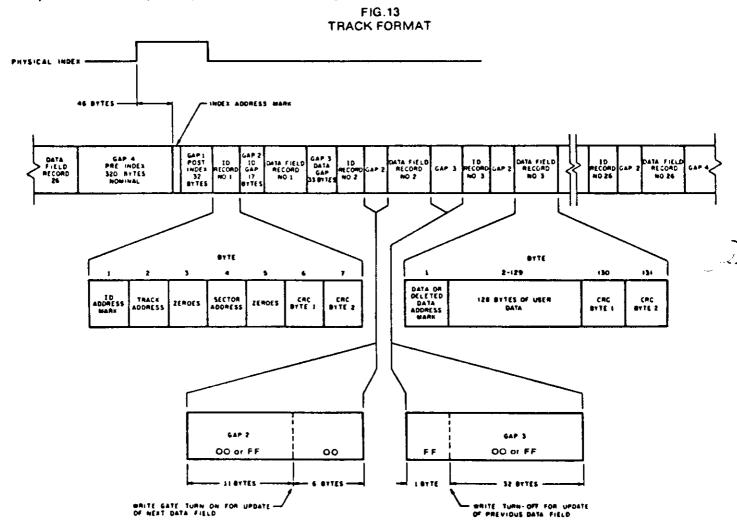
NON-IBM FORMATS

Non IBM Formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to section V, Type II commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field)must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:
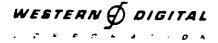
1) IBM Diskette OEM Information GA21-9190-1
2) SA900 IBM Compatibility Reference Manual - Shugart Associates.

FIG.13
TRACK FORMAT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V$_{DD}$ With Respect to V$_{BB}$ (Ground)	+ 20 to – 0.3V
Max Voltage to Any Input With Respect to V$_{BB}$	+ 20 to – 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	– 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

$T_A = 0^oC$ to 70^oC, $V_{DD} = +12.0V \pm .6V$, $V_{BB}^* = -5.0 \pm .5V$, $V_{SS} = 0V$, $V_{CC} = +5V \pm .25V$

$V_{DD} = 10$ ma Nominal, $V_{CC} = 30$ ma Nominal, $V_{BB}^* = 0.4$ µa Nominal

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leagage			10	µA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	µA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_0 = -100$ uA
V_{OL}	Output Low Voltage			0.45**	V	$I_0 = 1.6$ mA

NOTE: Vol ≤ .4V when interfacing with low Power Schottky parts ($I_0 < 1$ ma)   **Write Gate $V_{OL} \leq 0.5V$
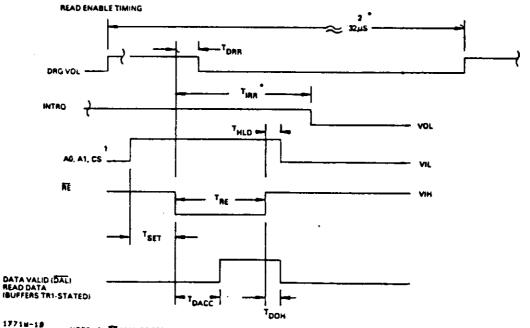
TIMING CHARACTERISTICS

$T_A = 0^oC$ to 70^oC, $V_{DD} = +12V \pm .6V$, $V_{BB}^* = -5 \pm .25V$, $V_{SS} = 0V$, $V_{CC} = +5 \pm .25V$

NOTE: Timings are given for 2 MHZ Clock. For those timings noted, values will double when chip is operated at 1 MHZ. Use 1 MHZ when using mini-floppy.

*V_{BB} required for −01 version only. Pin 1 (V_{BB}) is left open on −11 version.

Read Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	$C_L = 25$ pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	$C_L = 25$ pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	$C_L = 25$ pf

READ ENABLE TIMING

1771M-19
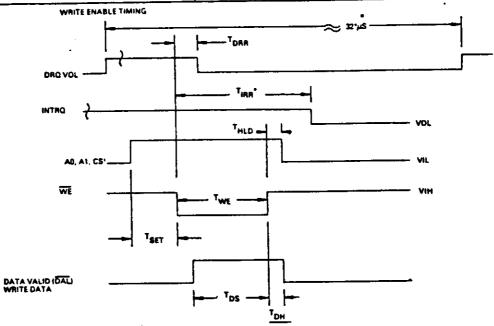
NOTE: 1. CS MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12° TO 32°µSEC WHEN S = 0.
*TIME DOUBLES WHEN CLK - 1MHz

Write Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	See Note
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

WRITE ENABLE TIMING

NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8μSEC AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12μSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1MHz.
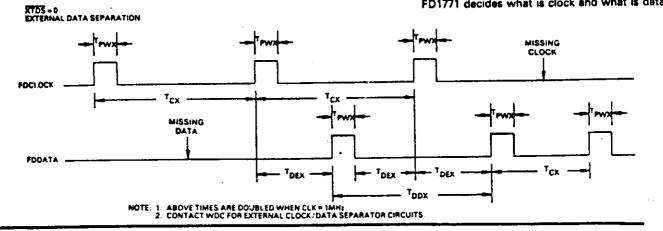
* = TIME DOUBLES WHEN CLK = 1 MHz.

External Data Separation ($\overline{XTDS}$ = 0)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWX	Pulse Width Rd Data & Rd Clock	150		350	nsec	
TCX	Clock Cycle Ext	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	

READ TIMING

$\overline{XTDS}$ = 0
EXTERNAL DATA SEPARATION

NOTE: FDCLK & FDDATA may be reversed
FD1771 decides what is clock and what is data

NOTE: 1. ABOVE TIMES ARE DOUBLED WHEN CLK = 1MHz.
2. CONTACT WDC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.
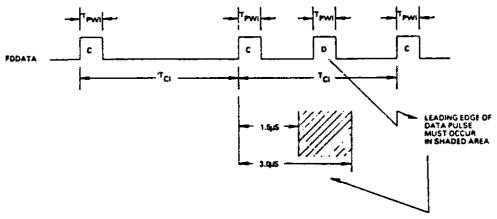
Internal Data Separation ($\overline{XTDS}$ = 1)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWI	Pulse Width Data & Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

READ TIMING

$\overline{XTDS}$ = 1
INTERNAL DATA SEPARATION
FDCLOCK MUST BE TIED HIGH
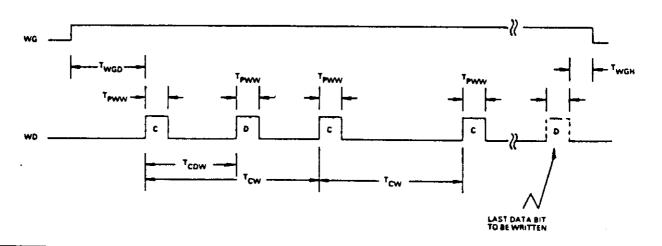
NOTE: INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATE RECOVERY RELIABILITY, WDC RECOMMENDS EXTERNAL DATA SEPARATION BE USED.

Write Data Timing:
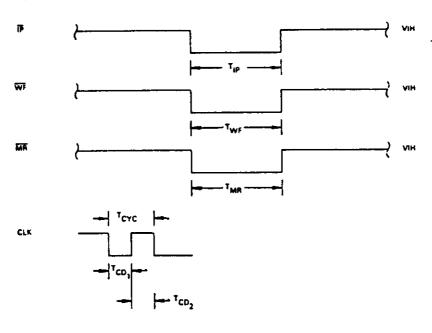
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	±0.5%± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	±0.5%± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	
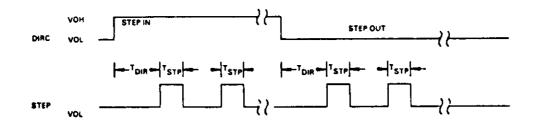
WRITE DATA TIMING

Miscellaneous Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD$_1$	Clock Duty	175			nsec	2MHZ ± 1% See Note
TCD$_2$	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	
TDIR	Dir Setup to Step	24			µsec	These times doubled
TMR	Master Reset Pulse Width	10			µsec	when CLK = 1 MHZ
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	10			µsec	

MISCELLANEOUS TIMING

PIN OUTS

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	Power Supplies	V$_{BB}$/NC	− 5V for − 01 version/open for − 11 version
20		V$_{SS}$	Ground
21		V$_{CC}$	+5V
40		$\overline{V_{DD}}$	+12V
19	MASTER RESET	$\overline{MR}$	• A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.

PIN NO	PIN NAME	SYMBOL	FUNCTION
Computer Interface:			
7-14	DATA ACCESS LINES	DALØ-DAL7	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{\text{WE}}$ or a transmitter enabled by $\overline{\text{RE}}$.
3	CHIP SELECT	$\overline{\text{CS}}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0, A1	• These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: A1 A0 $\overline{\text{RE}}$ $\overline{\text{WE}}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{\text{RE}}$	• A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
2	WRITE ENABLE	$\overline{\text{WE}}$	• A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
38	DATA REQUEST	DRQ	• This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	• This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	• This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
Floppy Disk Interface:			
25	EXTERNAL DATA SEPARATION	$\overline{\text{XTDS}}$	• A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	• This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	• This input receives the raw read disk data if $\overline{\text{XTDS}}$ = 1, or the externally separated data if $\overline{\text{XTDS}}$ = 0.
31	WRITE DATA	WD	• This output contains both clock and data bits of 500 ns duration.
28	HEAD LOAD	HLD	• The HLD output controls the loading of the Read-Write head against the media. The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	$\overline{\text{Phase 1}}$/Step	$\overline{\text{PH1}}$/STEP	• If the $\overline{\text{3PM}}$ input is a logic low the three phase motor control is selected and $\overline{\text{PH1}}$, $\overline{\text{PH2}}$, and PH3 outputs form a one active low signal out of three. $\overline{\text{PH1}}$ is active low after $\overline{\text{MR}}$. If the $\overline{\text{3PM}}$ input is a logic high the step and direction motor control is selected. The step output contains a 4μsec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
16	$\overline{\text{Phase 2}}$/Direction	$\overline{\text{PH2}}$/DIRC	
17	Phase 3	PH3	
18	$\overline{\text{3 Phase Motor Select}}$	$\overline{\text{3PM}}$	

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PIN NO.;	PIN NAME;	SYMBOL;	FUNCTION
29	Track Greater Than 43	TG43	• This output informs the drive that the Read-W head is positioned between track 44-76. This output valid only during Read and Write Commands.
30	WRITE GATE	WG	• This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	• This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT	$\overline{\text{WF}}$	• This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	TRACK 00	$\overline{\text{TR00}}$	• This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	INDEX PULSE	$\overline{\text{IP}}$	• Input, when low for a minimum of 10 µsec, informs the FD1771 when an index mark is encountered on the diskette.
36	WRITE PROTECT	$\overline{\text{WPRT}}$	• This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DISK INTIALIZATION	$\overline{\text{DINT}}$	• The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$ = 0, the operation is terminated and the Write Protect Status bit is set.
22	TEST	$\overline{\text{TEST}}$	• This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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C O R P O R A T I O N

TMS 5501 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080 CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080 and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080 microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.
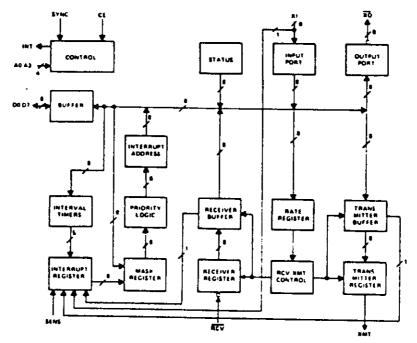
FIGURE 1—TMS 5501 BLOCK DIAGRAM

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080 uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

- read the receiver buffer
- read the input port
- read the interrupt address
- read TMS 5501 status
- issue discrete commands
- load baud rate register
- load the transmitter buffer
- load the output port
- load the mask register
- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5501

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080 is not required.

Communications Functions

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate — A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection — The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission — The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals — Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5501 provides a TMS 8080 system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, XI7, if selected by a discrete command from the TMS 8080 (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080 only if there is no higher priority interrupt that has not been accepted by the TMS 8080. The TMS 5501 prioritizes interrupts in the order shown below:

1st	—	Interval Timer #1
2nd	—	Interval Timer #2
3rd	—	External Sensor
4th	—	Interval Timer #3
5th	—	Receiver Buffer Loaded
6th	—	Transmitter Buffer Emptied
7th	—	Interval Timer #4
8th	—	Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080 that an interrupt has occured. (3) If the TMS 8080 is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080 polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080 will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080.

1.3   APPLICATIONS

Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080 and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080 and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080 to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080 when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080 with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS — a definition of each of the circuit's external connections

COMMANDS — the address required to select each of the TMS 5501 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080 via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
CE	18	Chip enable—When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands.
A3	17	Address bus—A3 through A0 are the lines that are addressed by the TMS 8080 to select a particular
A2	16	TMS 5501 function.
A1	15	
A0	14	
SYNC	19	Synchronizing signal—The SYNC signal is issued by the TMS 8080 and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits DO (interrupt acknowledge) and D1 ($\overline{WO}$, data output function).
$\overline{RCV}$	5	Receiver serial data input line—$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued)
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION

INPUTS

SIGNATURE	PIN	DESCRIPTION
XI 0	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs
XI 1	38	function is addressed. External input n is gated to data bus bit n without conversion.
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing – A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080.

OUTPUTS

SIGNATURE	PIN	DESCRIPTION
$\overline{XO}$ 0	24	External outputs—These eight external outputs are driven by the complement of the output
$\overline{XO}$ 1	25	register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load
$\overline{XO}$ 2	26	output register command, the external output n will be a low (high). The external outputs change
$\overline{XO}$ 3	27	only when a load-output-register function is addressed.
$\overline{XO}$ 4	28	
$\overline{XO}$ 5	29	
$\overline{XO}$ 6	30	
$\overline{XO}$ 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting

DATA BUS INPUT/OUTPUT

SIGNATURE	PIN	DESCRIPTION
D0	13	Data bus – Data transfers between the TMS 5501 and the TMS 8080 are made via the 8-bit
D1	12	bidirectional data bus. D0 is the LSB. D7 is the MSB.
D2	11	
D3	10	
D4	9	
D5	8	
D6	7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.

POWER AND CLOCKS

SIGNATURE	PIN	DESCRIPTION
V_{SS}	4	Ground reference
V_{BB}	1	Supply voltage (−5 V nominal)
V_{CC}	2	Supply voltage (5 V nominal)
V_{DD}	3	Supply voltage (12 V nominal)
ϕ1	20	Phase 1 clock
ϕ2	21	Phase 2 clock

2.2 TMS 5501 COMMANDS

The TMS 5501 operates as input/output device for the TMS 8080. Functions are initiated via the TMS 8080 address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

5501 PORT NO.	A3	A2	A1	A0	COMMAND	FUNCTION	PARAGRAPH
0	L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1
1	L	L	L	H	Read external inputs	XIn → Dn	2.2.2
2	L	L	H	L	Read interrupt address	RST → Dn	2.2.3
3	L	L	H	H	Read TMS 5501 status	(Status) → Dn	2.2.4
4	L	H	L	L	Issue discrete commands	See Fig.4	2.2.5
5	L	H	L	H	Load rate register	See Fig.4	2.2.6
6	L	H	H	L	Load transmitter buffer	Dn → TBn	2.2.7
7	L	H	H	H	Load Output port	Dn → XOn	2.2.8
8	H	L	L	L	Load mask register	Dn → MRn	2.2.9
9	H	L	L	H	Load interval timer 1	Dn → Timer 1	2.2.10
10	H	L	H	L	Load interval timer 2	Dn → Timer 2	2.2.10
11	H	L	H	H	Load interval timer 3	Dn → Timer 3	2.2.10
12	H	H	L	L	Load interval timer 4	Dn → Timer 4	2.2.10
13	H	H	L	H	Load interval timer 5	Dn → Timer 5	2.2.10
14	H	H	H	L	No function		
15	H	H	H	H	No function		

RBn Receiver buffer bit n
Dn Data bus I/O terminal n
XIn External input terminal n
RST 11 $(1A_5)$ $(1A_4)$ $(1A_3)$ 1 1 1 (see Table 3)
TBn Transmit buffer bit n
XOn Output register bit n
MRn Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT								INTERRUPT CAUSED BY
0	1	2	3	4	5	6	7	
H	H	H	L	L	L	H	H	Interval Timer 1
H	H	H	H	L	L	H	H	Interval Timer 2
H	H	H	L	H	L	H	H	External Sensor
H	H	H	H	H	L	H	H	Interval Timer 3
H	H	H	L	L	H	H	H	Receiver Buffer
H	H	H	H	L	H	H	H	Transmitter Buffer
H	H	H	L	H	H	H	H	Interval Timer 4
H	H	H	H	H	H	H	H	Interval Timer 5

The following paragraphs define the functions of the TMS 5501 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080 and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5501 status

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START BIT DETECT	FULL BIT DETECT	INTRPT PENDING	XMIT BUFFER EMPTY	RCV BUFFER LOADED	SERIAL RCVD	OVERRUN ERROR	FRAME ERROR

FIGURE 3—DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indiciates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty

A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending

A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected

A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected

A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

NORMALLY LOW

BIT:	7	6	5	4	3	2	1	0
	NOT USED	NOT USED	TEST BIT	TEST BIT	INT. ACK. ENABLE	INT. 7 SELECT	BREAK	RESET

H. Enables interrupt acknowledge —
L: Inhibits interrupt acknowledge —

H: Selects XI 7 —
L: Selects interval timer 5 —

H: Reset
L: No action

H: L Sets XMT output low
L: H Sets XMT output high
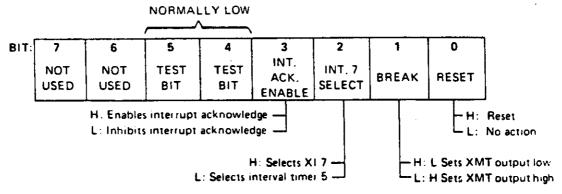
FIGURE 4—DISCRETE COMMAND FORMAT

Bit 0, reset

A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.

2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080.

3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.

4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5501 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

BIT:	7	6	5	4	3	2	1	0
	STOP BIT(s)	9600 baud	4800 baud	2400 baud	1200 baud	300 baud	150 baud	110 baud

├─H: One stop bit
└─L: Two stop bits
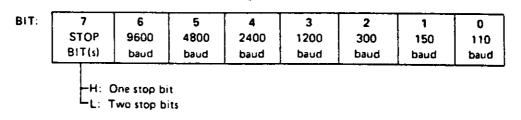
FIGURE 5—DATA BUS ASSIGNMENTS FOR RATE COMMANDS

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0   110 baud
Bit 1   150 baud
Bit 2   300 baud
Bit 3   1200 baud
Bit 4   2400 baud
Bit 5   4800 baud
Bit 6   9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO\ 0}$ through $\overline{XO\ 7}$ as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1) . . . . −0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1 . . . . −0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . −0.3 V to 20 V
All input and output voltages (see Note 1) . . . . −0.3 V to 20 V
Continuous power dissipation . . . . 1.1 W
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	3.3		$V_{CC}+1$	V
High-level clock input voltage, $V_{IH(\phi)}$	$V_{DD}-1$		$V_{DD}+1$	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 2)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)	−1		0.6	V
Operating free-air temperature, T_A	0		70	°C
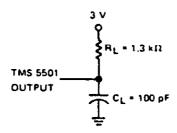
NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only

3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PZX}	Data bus output enable time	$C_L = 100$ pF, $R_L = 1.3$ kΩ		200	ns
t_{PXZ}	Data bus output disable time to high-impedance state			180	ns
t_{PD}	External data output propagation delay time from φ2			200	ns
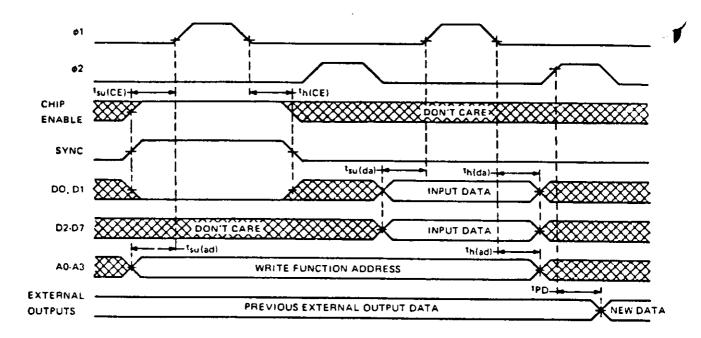
C_L includes probe and jig capacitance

LOAD CIRCUIT
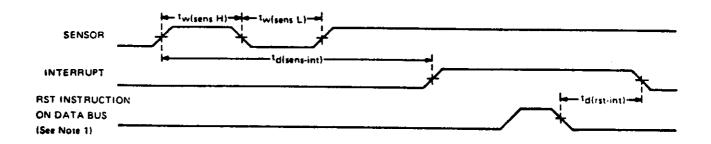
NOTE For φ1 or φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(φ)}$ All other timing points are the 50% level.

FIGURE 6—READ CYCLE TIMING

NOTE   For φ1 and φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(o)}$. All other timing points are the 50% level.

FIGURE 7—WRITE CYCLE TIMING

NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.
         2. All timing points are 50% of V_{IH}.

FIGURE 8—SENSOR/INTERRUPT TIMING

intel®
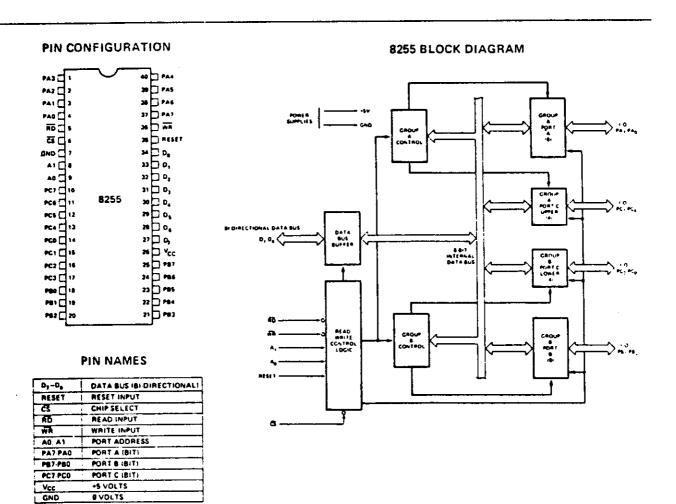
Silicon Gate MOS 8255

PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS™-8 and MCS™-80 Microprocessor Families**

- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual In-Line Package**
- **Reduces System Package Count**

The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bidirectional Bus mode which uses 8 lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

PIN CONFIGURATION

8255 BLOCK DIAGRAM

PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	0 VOLTS

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)
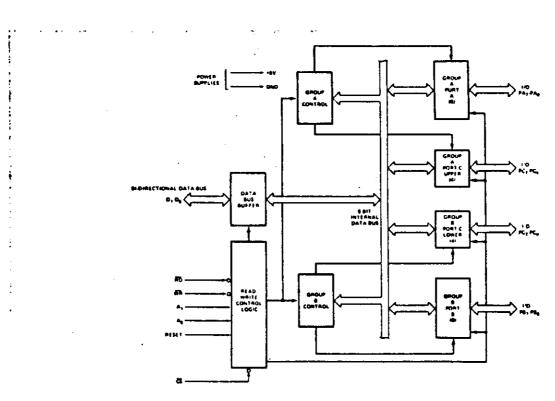
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION

8255 Block Diagram

(RESET)

Reset: A "high" on this input clears all internal registers in-cluding the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the 8080 CPU "out-puts" a control word to the 8255. The control word con-tains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

    Control Group A — Port A and Port C upper (C7-C4)
    Control Group B — Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C
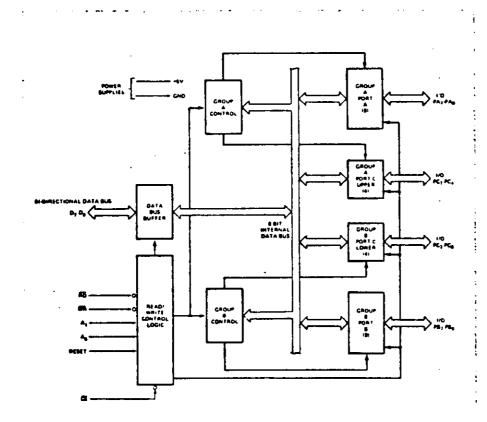
The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexi-bility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.
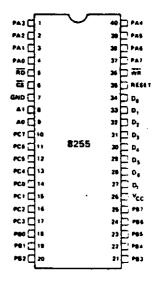
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be di-vided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunc-tion with Ports A and B.

8255 BLOCK DIAGRAM

PIN CONFIGURATION

PIN NAMES

D₇–D₀	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	0 VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:
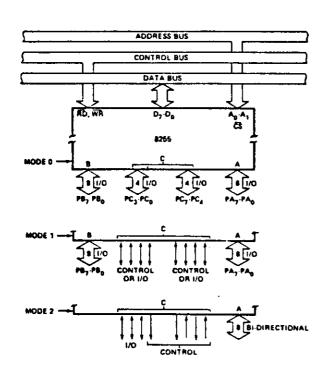
    Mode 0 — Basic Input/Output
    Mode 1 — Strobed Input/Output
    Mode 2 — Bi-Directional Bus
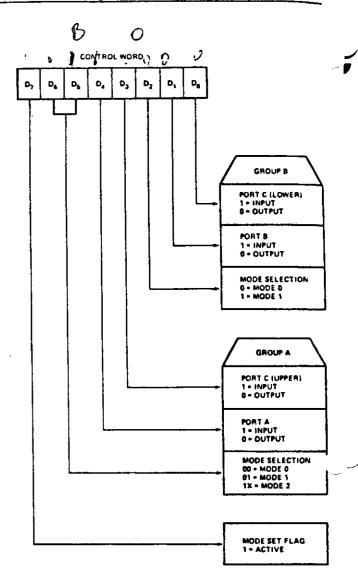
When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

Basic Mode Definitions and Bus Interface

CONTROL WORD

BIT SET/RESET
1 = SET
0 = RESET

BIT SELECT

BIT SET/RESET FLAG
0 = ACTIVE

Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without effecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.
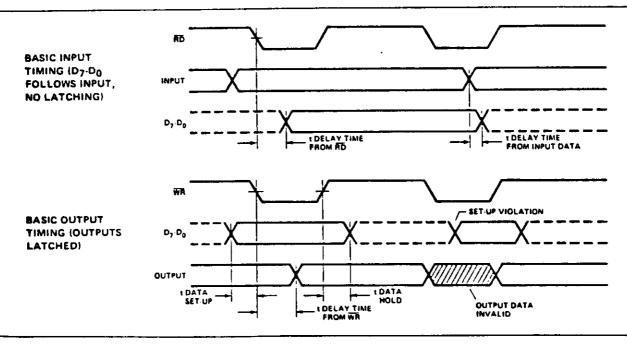
Operating Modes
Mode 0 (Basic Input/Output)

This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:
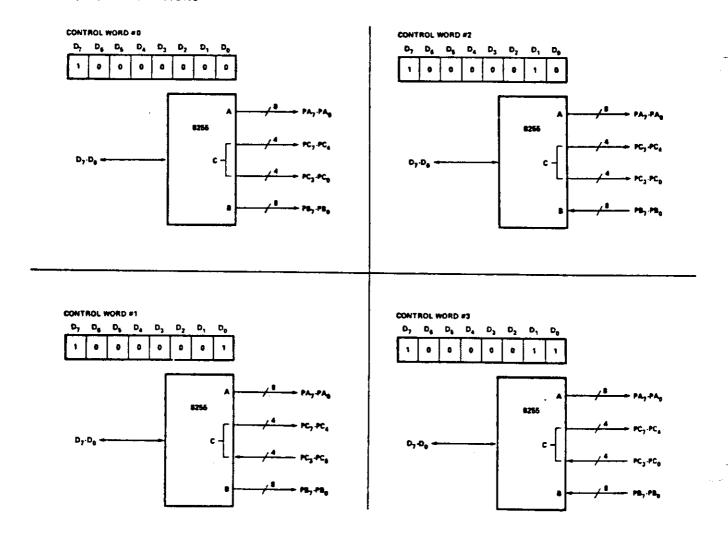
* Two 8-bit ports and two 4-bit ports.
* Any port can be input or output.
* Outputs are latched.
* Inputs are not latched.
* 16 different Input/Output configurations are possible in this Mode.

BASIC INPUT TIMING (D_7-D_0 FOLLOWS INPUT, NO LATCHING)

BASIC OUTPUT TIMING (OUTPUTS LATCHED)

Mode 0 Timing
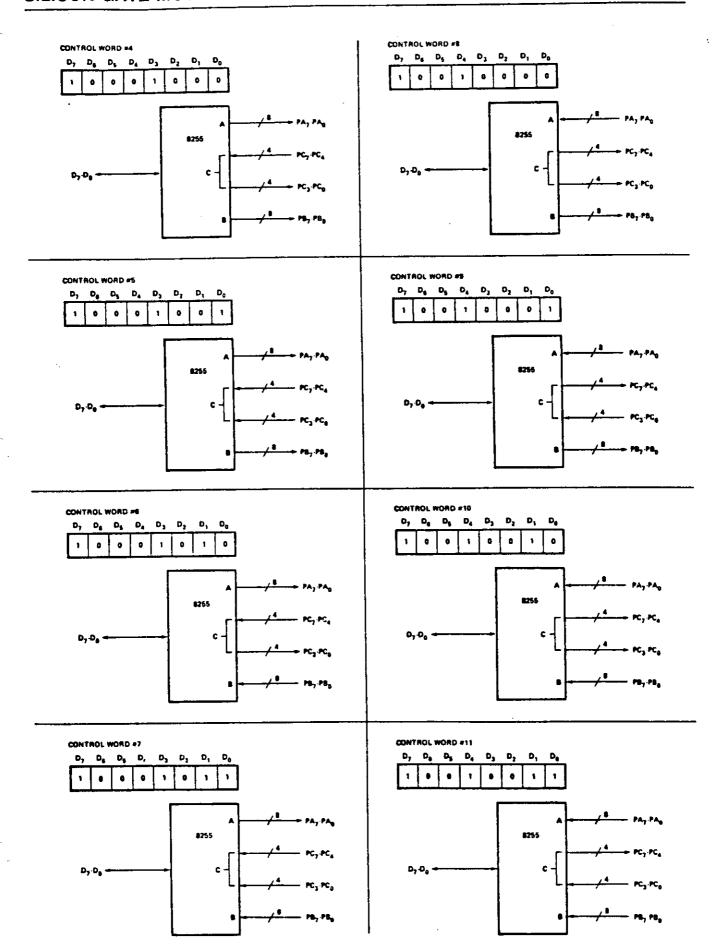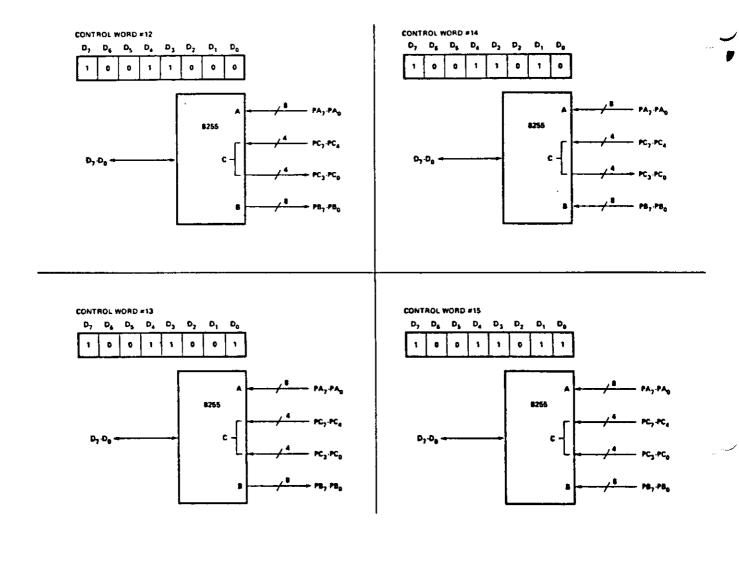
MODE 0 PORT DEFINITION CHART

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 CONFIGURATIONS

CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0

CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0

CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1

CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1

CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0

8255

$D_7 \cdot D_0 \rightarrow$

A $\rightarrow$ /8 $\rightarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\rightarrow$ /8 $\rightarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #5

D7	D6	D5	D4	D3	D7	D1	D0
1	0	0	0	1	0	0	1

8255

$D_7 \cdot D_0 \rightarrow$

A $\rightarrow$ /8 $\rightarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\rightarrow$ /8 $\rightarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0

8255

$D_7 \cdot D_0 \rightarrow$

A $\rightarrow$ /8 $\rightarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\rightarrow$ /8 $\rightarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1

8255

$D_7 \cdot D_0 \rightarrow$

A $\rightarrow$ /8 $\rightarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\rightarrow$ /8 $\rightarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0

8255

$D_7 \cdot D_0 \leftarrow$

A $\leftarrow$ /8 $\leftarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\leftarrow$ /8 $\leftarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1

8255

$D_7 \cdot D_0 \leftarrow$

A $\leftarrow$ /8 $\leftarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\leftarrow$ /8 $\leftarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0

8255

$D_7 \cdot D_0 \leftarrow$

A $\leftarrow$ /8 $\leftarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\leftarrow$ /8 $\leftarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

8255

$D_7 \cdot D_0 \leftarrow$

A $\leftarrow$ /8 $\leftarrow$ $PA_7 \cdot PA_0$
C $\rightarrow$ /4 $\rightarrow$ $PC_7 \cdot PC_4$
C $\rightarrow$ /4 $\rightarrow$ $PC_3 \cdot PC_0$
B $\leftarrow$ /8 $\leftarrow$ $PB_7 \cdot PB_0$

CONTROL WORD #12

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	1	1	0	0	0

CONTROL WORD #14

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	1	1	0	1	0

CONTROL WORD #13

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	1	1	0	0	1

CONTROL WORD #15

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	1	1	0	1	1

Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)
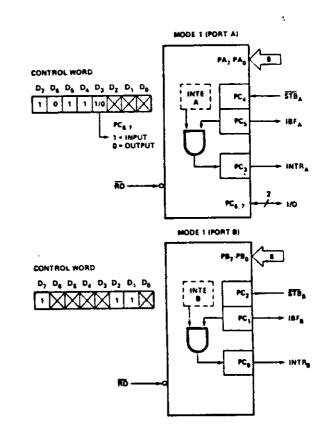
A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by the falling edge of the STB input and is reset by the rising edge of the RD input.

INTR (Interrupt Request)
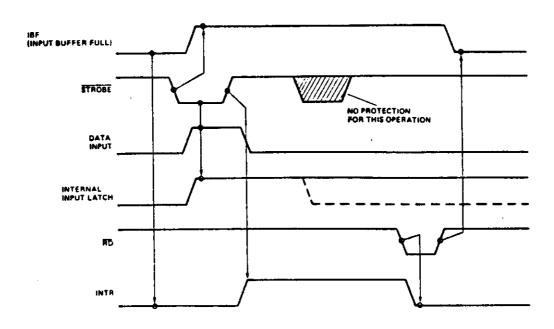
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ if IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

Mode 1 Input

Basic Timing Input

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by the falling edge of the $\overline{ACK}$ input signal.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

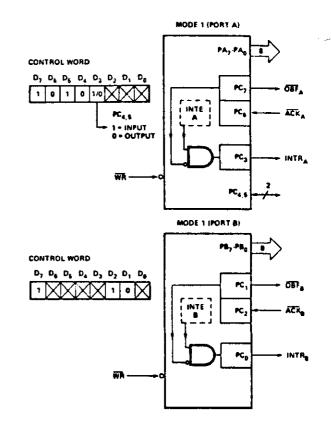A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{ACK}$ if $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.
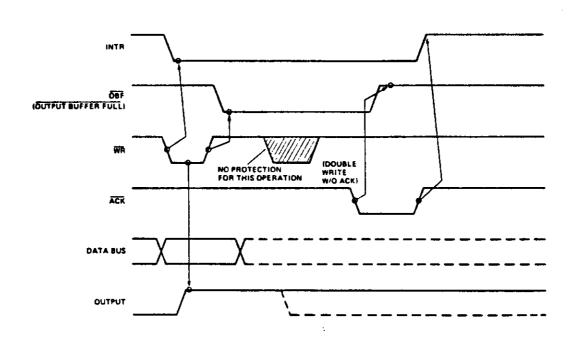
   INTE A

   Controlled by bit set/reset of PC_6.

   INTE B

   Controlled by bit set/reset of PC_2.

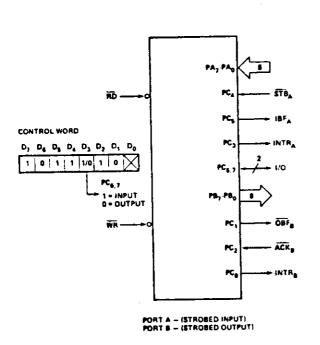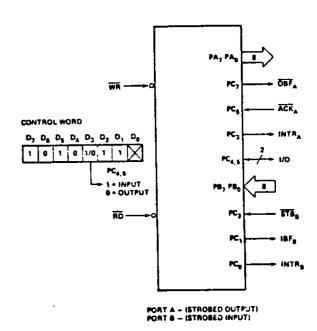
Mode 1 Output

Basic Timing Output

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

CONTROL WORD

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |

1 | 0 | 1 | 1 | 1 | 1/0 | 1 | 0

PC₆,₇
1 = INPUT
0 = OUTPUT

$\overline{RD}$, $\overline{WR}$

PA₇-PA₀ (8)
PC₄ — $\overline{STB_A}$
PC₅ — IBF_A
PC₃ — $INTR_A$
PC₆,₇ — 2 — I/O
PB₇-PB₀ (8)
PC₁ — $\overline{OBF_B}$
PC₂ — $\overline{ACK_B}$
PC₀ — $INTR_B$

PORT A — (STROBED INPUT)
PORT B — (STROBED OUTPUT)

CONTROL WORD

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |

1 | 0 | 1 | 0 | 1/0 | 1 | 1

PC₄,₅
1 = INPUT
0 = OUTPUT

$\overline{WR}$, $\overline{RD}$

PA₇-PA₀ (8)
PC₇ — $\overline{OBF_A}$
PC₆ — $\overline{ACK_A}$
PC₃ — $INTR_A$
PC₄,₅ — 2 — I/O
PB₇-PB₀ (8)
PC₂ — $\overline{STB_B}$
PC₁ — IBF_B
PC₀ — $INTR_B$

PORT A — (STROBED OUTPUT)
PORT B — (STROBED INPUT)

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:
● Used in Group A only.
● One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
● Both inputs and outputs are latched.
● The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC₆.

Input Operations

$\overline{STB}$ (Strobe Input)
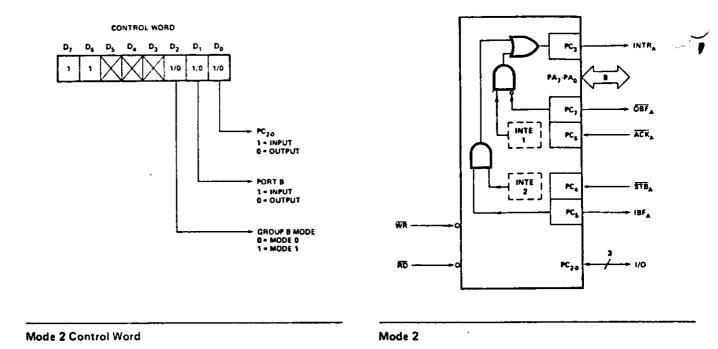
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)
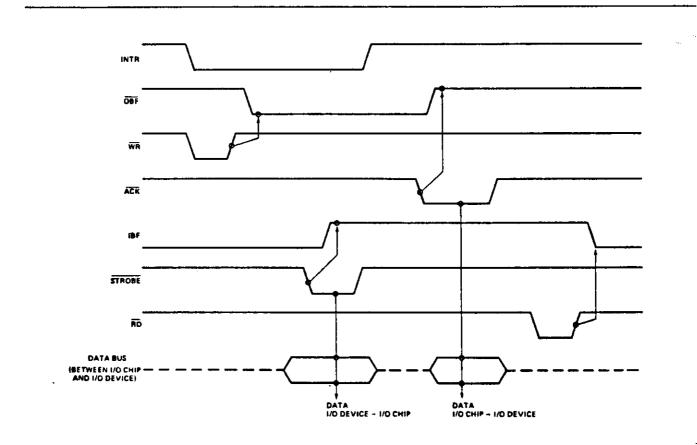
A "high" on this output indicates that data has been loaded into the input latch.
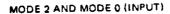
INTE 2 (The INTE Flip-Flop associated with IBF)

Controlled by bit set/reset of PC₄.

CONTROL WORD

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	✕	✕	✕	I/O	I/O	I/O

PC_{2-0}
1 = INPUT
0 = OUTPUT

PORT B
1 = INPUT
0 = OUTPUT

GROUP B MODE
0 = MODE 0
1 = MODE 1

Mode 2 Control Word

Mode 2
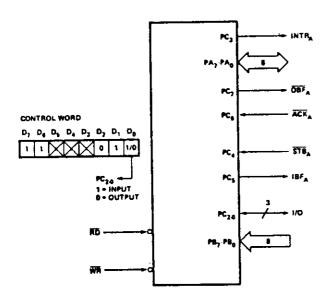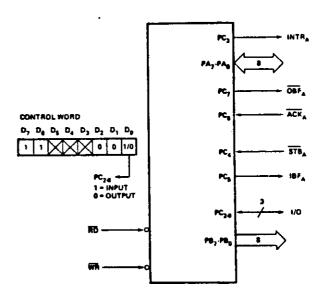
Mode 2 (Bi-directional) Timing

MODE 2 AND MODE 0 (INPUT)

CONTROL WORD

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	1	╳	╳	╳	0	1	I/O

PC₂₋₀
1 = INPUT
0 = OUTPUT

MODE 2 AND MODE 0 (OUTPUT)

CONTROL WORD

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	1	╳	╳	╳	0	0	I/O
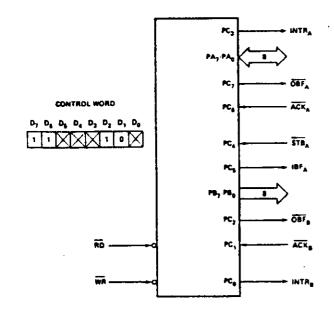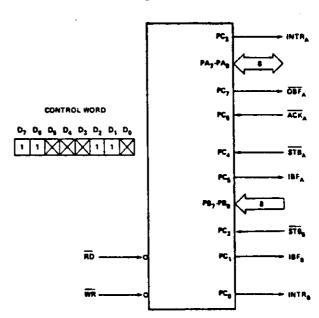
PC₂₋₀
1 = INPUT
0 = OUTPUT

MODE 2 AND MODE 1 (OUTPUT)

CONTROL WORD

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	1	╳	╳	╳	╳	1	0	╳

MODE 2 AND MODE 1 (INPUT)

CONTROL WORD

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	1	╳	╳	╳	╳	1	1	╳

Mode 2 Combinations
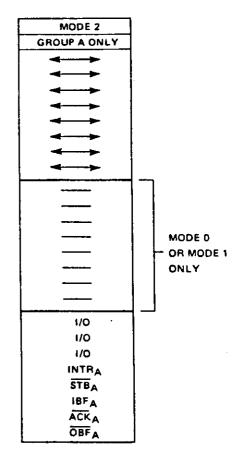
MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA$_0$	IN	OUT	IN	OUT	← →
PA$_1$	IN	OUT	IN	OUT	← →
PA$_2$	IN	OUT	IN	OUT	← →
PA$_3$	IN	OUT	IN	OUT	← →
PA$_4$	IN	OUT	IN	OUT	← →
PA$_5$	IN	OUT	IN	OUT	← →
PA$_6$	IN	OUT	IN	OUT	← →
PA$_7$	IN	OUT	IN	OUT	← →
PB$_0$	IN	OUT	IN	OUT	—
PB$_1$	IN	OUT	IN	OUT	—
PB$_2$	IN	OUT	IN	OUT	—
PB$_3$	IN	OUT	IN	OUT	—
PB$_4$	IN	OUT	IN	OUT	—
PB$_5$	IN	OUT	IN	OUT	—
PB$_6$	IN	OUT	IN	OUT	—
PB$_7$	IN	OUT	IN	OUT	—
PC$_0$	IN	OUT	INTR$_B$	INTR$_B$	I/O
PC$_1$	IN	OUT	IBF$_B$	$\overline{OBF}_B$	I/O
PC$_2$	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC$_3$	IN	OUT	INTR$_A$	INTR$_A$	INTR$_A$
PC$_4$	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC$_5$	IN	OUT	IBF$_A$	I/O	IBF$_A$
PC$_6$	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC$_7$	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs —
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs —
Bits in C upper (PC$_7$-PC$_4$) must be individually accessed using the bit set/reset function.

Bits in C lower (PC$_3$-PC$_0$) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

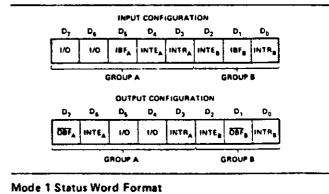### Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C

allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INPUT CONFIGURATION

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
I/O	I/O	IBF$_A$	INTE$_A$	INTR$_A$	INTE$_B$	IBF$_B$	INTR$_B$

GROUP A   GROUP B

OUTPUT CONFIGURATION

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
$\overline{OBF}_A$	INTE$_A$	I/O	I/O	INTR$_A$	INTE$_B$	$\overline{OBF}_B$	INTR$_B$

GROUP A   GROUP B

Mode 1 Status Word Format

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
$\overline{OBF}_A$	INTE$_1$	IBF$_A$	INTE$_2$	INTR$_A$	✕	✕	✕

GROUP A   GROUP B
(DEFINED BY MODE 0 OR MODE 1 SELECTION)

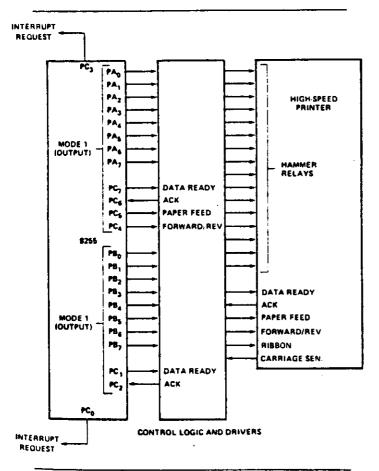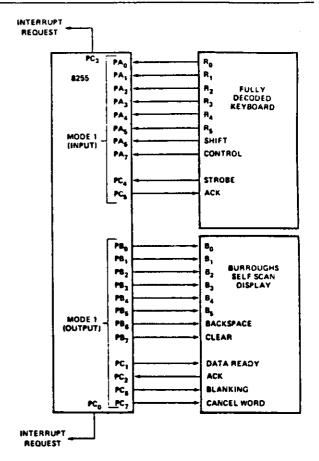### Mode 2 Status Word Format

APPLICATIONS OF THE 8255

The 8255 is a very powerful tool for interfacing peripheral equipment to the 8080 microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.
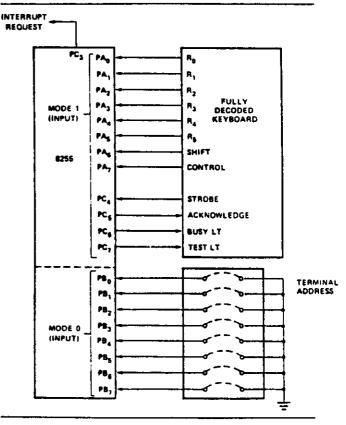
Each peripheral device in a Microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255 is programmed by the I/O service routine and becomes an extension of the systems software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the Detailed Operational Description, a control word can easily be developed to initialize the 8255 to exactly "fit" the application. Here are a few examples of typical applications of the 8255.

Printer Interface

Keyboard and Display Interface

Keyboard and Terminal Address Interface

Digital to Analog, Analog to Digital

MODE 0 (OUTPUT)

8255

BIT SET/RESET

MODE 0 (INPUT)

PA₀, PA₁, PA₂, PA₃, PA₄, PA₅, PA₆, PA₇, PC₄, PC₅, PC₆, PC₇

12-BIT D-A CONVERTER (DAC) — LSB ... MSB — ANALOG OUTPUT

PC₀ — STB DATA
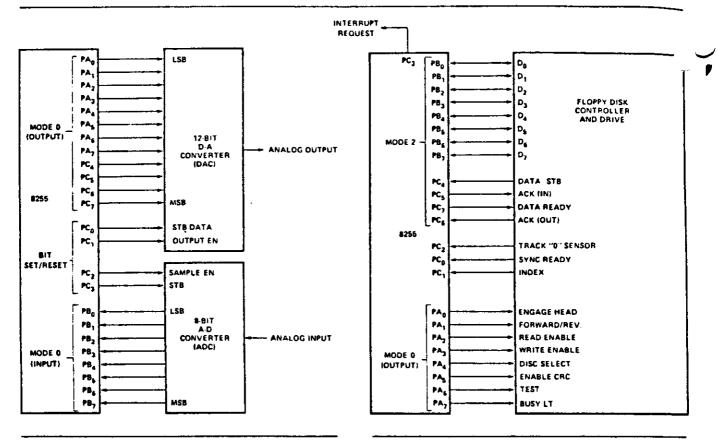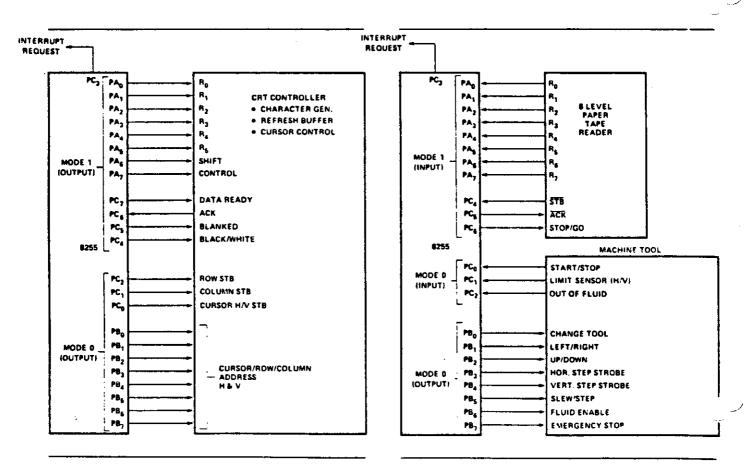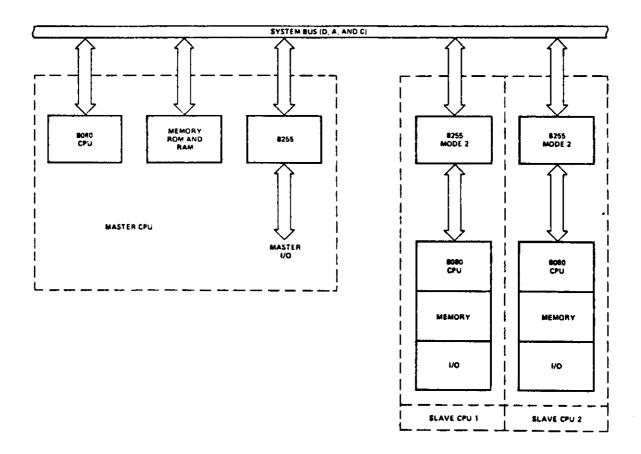PC₁ — OUTPUT EN

PC₂ — SAMPLE EN
PC₃ — STB

PB₀, PB₁, PB₂, PB₃, PB₄, PB₅, PB₆, PB₇ — 8-BIT A-D CONVERTER (ADC) — LSB ... MSB — ANALOG INPUT

Basic Floppy Disc Interface

INTERRUPT REQUEST

PC₃

MODE 2

8255

MODE 0 (OUTPUT)

PB₀, PB₁, PB₂, PB₃, PB₄, PB₅, PB₆, PB₇ — D₀, D₁, D₂, D₃, D₄, D₅, D₆, D₇ — FLOPPY DISK CONTROLLER AND DRIVE

PC₄ — DATA STB
PC₅ — ACK (IN)
PC₇ — DATA READY
PC₆ — ACK (OUT)

PC₂ — TRACK "0" SENSOR
PC₀ — SYNC READY
PC₁ — INDEX

PA₀ — ENGAGE HEAD
PA₁ — FORWARD/REV.
PA₂ — READ ENABLE
PA₃ — WRITE ENABLE
PA₄ — DISC SELECT
PA₅ — ENABLE CRC
PA₆ — TEST
PA₇ — BUSY LT

Basic CRT Controller Interface

INTERRUPT REQUEST

PC₃

MODE 1 (OUTPUT)

8255

MODE 0 (OUTPUT)

PA₀, PA₁, PA₂, PA₃, PA₄, PA₅, PA₆, PA₇ — R₀, R₁, R₂, R₃, R₄, R₅, SHIFT, CONTROL — CRT CONTROLLER • CHARACTER GEN. • REFRESH BUFFER • CURSOR CONTROL

PC₇ — DATA READY
PC₆ — ACK
PC₅ — BLANKED
PC₄ — BLACK/WHITE

PC₂ — ROW STB
PC₁ — COLUMN STB
PC₀ — CURSOR H/V STB

PB₀, PB₁, PB₂, PB₃, PB₄, PB₅, PB₆, PB₇ — CURSOR/ROW/COLUMN ADDRESS H & V

Machine Tool Controller Interface

INTERRUPT REQUEST

PC₃

MODE 1 (INPUT)

8255

MODE 0 (INPUT)

MODE 0 (OUTPUT)

PA₀, PA₁, PA₂, PA₃, PA₄, PA₅, PA₆, PA₇ — R₀, R₁, R₂, R₃, R₄, R₅, R₆, R₇ — 8 LEVEL PAPER TAPE READER

PC₄ — STB
PC₅ — ACK
PC₆ — STOP/GO

MACHINE TOOL

PC₀ — START/STOP
PC₁ — LIMIT SENSOR (H/V)
PC₂ — OUT OF FLUID

PB₀ — CHANGE TOOL
PB₁ — LEFT/RIGHT
PB₂ — UP/DOWN
PB₃ — HOR. STEP STROBE
PB₄ — VERT. STEP STROBE
PB₅ — SLEW/STEP
PB₆ — FLUID ENABLE
PB₇ — EMERGENCY STOP

Distributed Intelligence Multi-Processor Interface
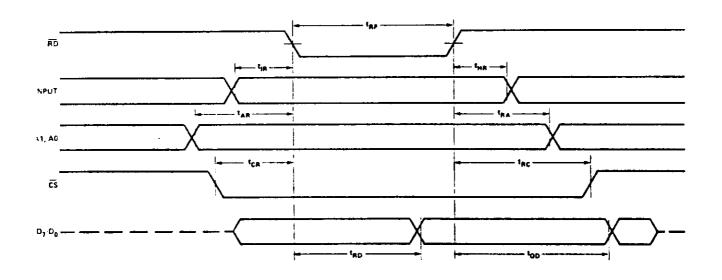
D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

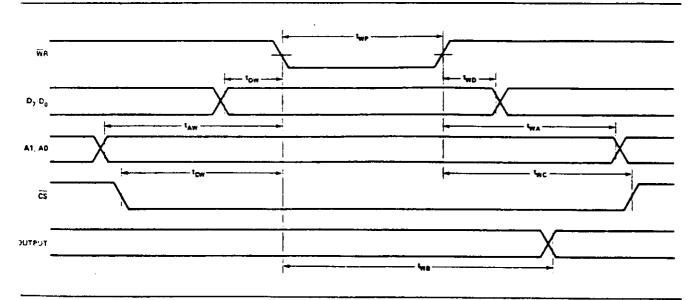| Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\mu A$ ($-100\mu A$ for D.B. Port)
I_{OH}[1]	Darlington Drive Current		2.0		mA	$V_{OH} = 1.5V$, $R_{EXT} = 390\Omega$
I_{CC}	Power Supply Current		40		mA	

NOTE:
1. Available on 8 pins only.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

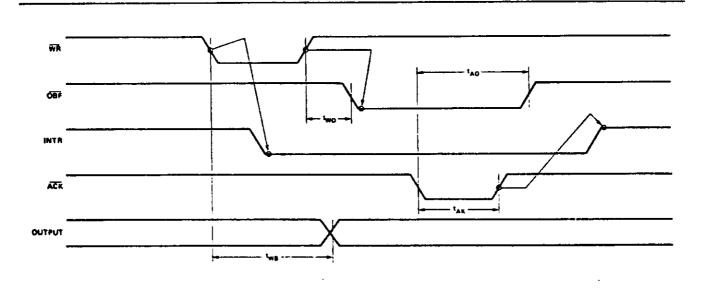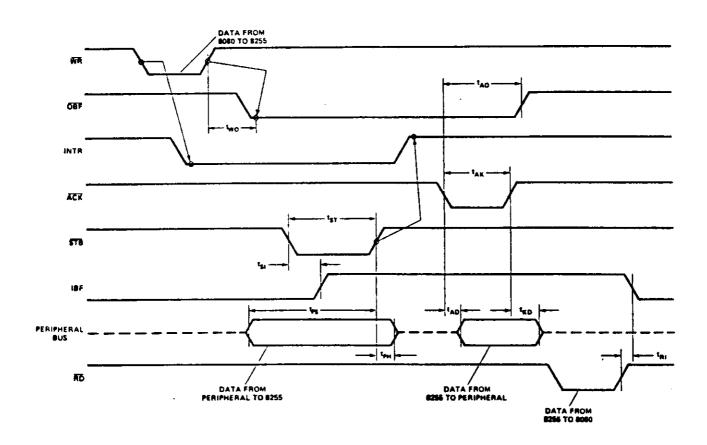| Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			430	ns	
t_{DW}	Time D.B. Stable Before $\overline{WR}$	10			ns	
t_{WD}	Time D.B. Stable After $\overline{WR}$	65			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	35			ns	
t_{CW}	Time CS Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time CS Stable After $\overline{WR}$	35			ns	
t_{WB}	Delay From $\overline{WR}$ To Output			500	ns	
t_{RP}	Pulse Width of $\overline{RD}$	430			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	50			ns	
t_{HR}	Input Hold Time	50			ns	
t_{RD}	Delay From $\overline{RD} = 0$ To System Bus	350			ns	
t_{OD}	Delay From $\overline{RD} = 1$ To System Bus	150			ns	
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time $\overline{CS}$ Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width Of $\overline{STB}$ Pulse	350			ns	
t_{PS}	Set-Up Time For Peripheral	150			ns	
t_{PH}	Hold Time For Peripheral	150			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD} = 1$	379			ns	
t_{RC}	Hold Time For CS After $\overline{RD} = 1$	5			ns	
t_{AD}	Time From $\overline{ACK} = 0$ To Output (Mode 2)			500	ns	
t_{KD}	Time From $\overline{ACK} = 1$ To Output Floating			300	ns	
t_{WO}	Time From $\overline{WR} = 1$ To $\overline{OBF} = 0$			300	ns	
t_{AO}	Time From $\overline{ACK} = 0$ To $\overline{OBF} = 1$			500	ns	
t_{SI}	Time From $\overline{STB} = 0$ To IBF			600	ns	
t_{RI}	Time From $\overline{RD} = 1$ To IBF = 0			300	ns	

Mode 0 (Basic Input)

Mode 0 (Basic Output)

Mode 1 (Strobed Input)

Mode 1 (Strobed Output)

Mode 2 (Bi-directional)

intel

2716
16K (2K × 8) UV ERASABLE PROM

- **Fast Access Time**
  - **350 ns Max. 2716-1**
  - **390 ns Max. 2716-2**
  - **450 ns Max. 2716**

- **Single + 5V Power Supply**

- **Low Power Dissipation**
  - **525 mW Max. Active Power**
  - **132 mW Max. Standby Power**

- **Pin Compatible to Intel® 5V ROMs (2316E, 2332A, and 2364A) and 2732 EPROM**

- **Simple Programming Requirements**
  - **Single Location Programming**
  - **Programs with One 50 ms Pulse**

- **Inputs and Outputs TTL Compatible during Read and Program**

- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332A and 2364A respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time–either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION

2716

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	Vpp
A3	5	20	OE
A2	6	19	A10
A1	7	18	CE
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

16K

2732†

A7	1	24	Vcc
A6	2	23	A8
A5	3	22	A9
A4	4	21	A11
A3	5	20	OE/Vpp
A2	6	19	A10
A1	7	18	CE
A0	8	17	O7
O0	9	16	O6
O1	10	15	O5
O2	11	14	O4
GND	12	13	O3

32K

†Refer to 2732
data sheet for
specifications
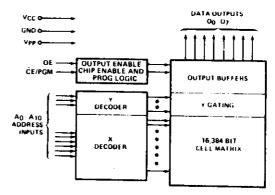
PIN NAMES

A_0 A_{10}	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

PINS / MODE	CE/PGM (18)	OE (20)	Vpp (21)	Vcc (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias . . . . –10°C to +80°C
Storage Temperature . . . . –65°C to +125°C
All Input or Output Voltages with
   Respect to Ground . . . . +6V to –0.3V
V$_{PP}$ Supply Voltage with Respect
   to Ground During Program . . . . +26.5V to –0.3V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V$_{CC}$ Power Supply[1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V$_{PP}$ Power Supply [2]	V$_{CC}$	V$_{CC}$	V$_{CC}$

READ OPERATION
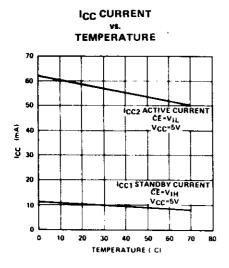
D.C. and Operating Characteristics
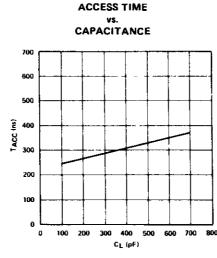
| Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I$_{LI}$	Input Load Current			10	μA	V$_{IN}$ = 5.25V
I$_{LO}$	Output Leakage Current			10	μA	V$_{OUT}$ = 5.25V
I$_{PP1}$[2]	V$_{PP}$ Current			5	mA	V$_{PP}$ = 5.25V
I$_{CC1}$[2]	V$_{CC}$ Current (Standby)		10	25	mA	$\overline{CE}$ = V$_{IH}$, $\overline{OE}$ = V$_{IL}$
I$_{CC2}$[2]	V$_{CC}$ Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V$_{IL}$
V$_{IL}$	Input Low Voltage	–0.1		0.8	V	
V$_{IH}$	Input High Voltage	2.0		V$_{CC}$+1	V	
V$_{OL}$	Output Low Voltage			0.45	V	I$_{OL}$ = 2.1 mA
V$_{OH}$	Output High Voltage	2.4			V	I$_{OH}$ = –400 μA
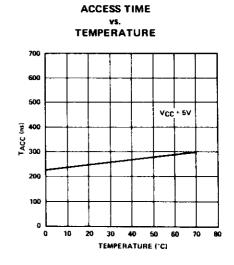
NOTES: 1. V$_{CC}$ must be applied simultaneously or before V$_{PP}$ and removed simultaneously or after V$_{PP}$.

     2. V$_{PP}$ may be connected directly to V$_{CC}$ except during programming. The supply current would then be the sum of I$_{CC}$ and I$_{PP1}$.

     3. Typical values are for T$_A$ = 25°C and nominal supply voltages.

     4. This parameter is only sampled and is not 100% tested.

Typical Characteristics

I$_{CC}$ CURRENT
vs.
TEMPERATURE

ACCESS TIME
vs.
CAPACITANCE

ACCESS TIME
vs.
TEMPERATURE

A.C. Characteristics

Symbol	Parameter	2716 Limits			2716-1 Limits			2716-2 Limits			Unit	Test Conditions
		Min	Typ[3]	Max	Min	Typ[3]	Max	Min	Typ[3]	Max		
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Capacitance[4] $T_A = 25°C$, f = 1 MHz
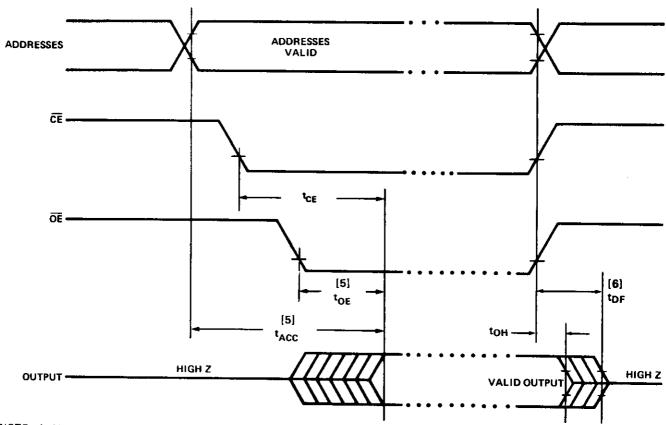
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
    Inputs   1V and 2V
    Outputs 0.8V and 2V

A. C. Waveforms [1]

NOTE: 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
    2. Vpp may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
    3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
    4. This parameter is only sampled and is not 100% tested.
    5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
    6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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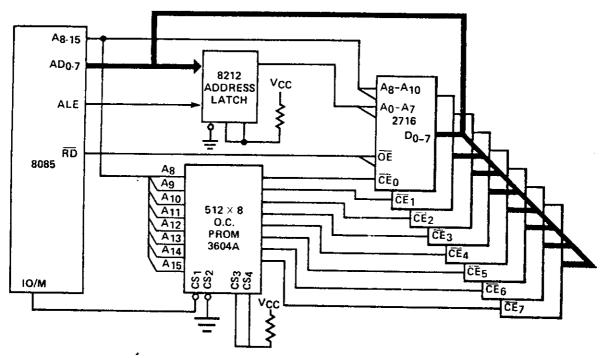Colonial Beach 22443
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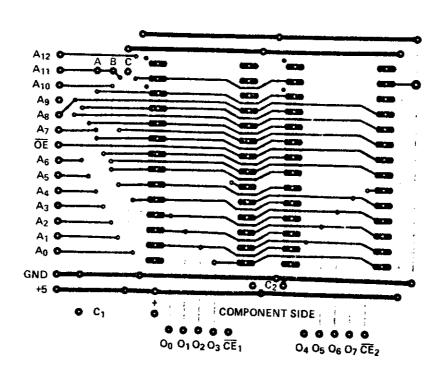4369 S. Howell Ave.
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- This scheme accomplished by using $\overline{CE}$ (PD) as the primary decode. $\overline{OE}$ (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{OE}$.
- A selected 2716 is available for systems which require $\overline{CE}$ access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:

  a) Compatibility with upward (and downward) memory expansion.

  b) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY PRINTED CIRCUIT BOARD LAYOUT

4

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W·sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

PINS / MODE	CE/PGM (18)	OE (20)	V$_{PP}$ (21)	V$_{CC}$ (24)	OUTPUTS (9-11, 13-17)
Read	V$_{IL}$	V$_{IL}$	+5	+5	D$_{OUT}$
Standby	V$_{IH}$	Don't Care	+5	+5	High Z
Program	Pulsed V$_{IL}$ to V$_{IH}$	V$_{IH}$	+25	+5	D$_{IN}$
Program Verify	V$_{IL}$	V$_{IL}$	+25	+5	D$_{OUT}$
Program Inhibit	V$_{IL}$	V$_{IH}$	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE (pin 18) be decoded and used as the primary device selecting function, while OE (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and OE is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the CE/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the CE/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including OE) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's CE/PGM input with V_{PP} at 25V will program that 2716. A low level CE/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

intel®

2114A
1024 X 4 BIT STATIC RAM

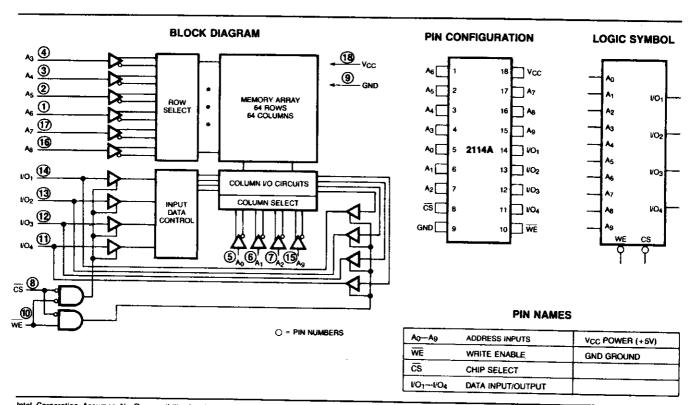|	2114AL-1	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	100	120	150	200	200	250
Max. Current (mA)	40	40	40	40	70	70

- HMOS Technology

- Low Power, High Speed

- Identical Cycle and Access Times

- Single +5V Supply ±10%

- High Density 18 Pin Package

- Completely Static Memory — No Clock or Timing Strobe Required

- Directly TTL Compatible: All Inputs and Outputs

- Common Data Input and Output Using Three-State Outputs

- 2114 Upgrade

The Intel® 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

BLOCK DIAGRAM

O = PIN NUMBERS

PIN CONFIGURATION

LOGIC SYMBOL

PIN NAMES

A_0—A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1—I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to 80°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin
  With Respect to Ground .... −3.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 5mA

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

SYMBOL	PARAMETER	2114AL-1/L-2/L-3/L-4			2114A-4/-5			UNIT	CONDITIONS
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	$V_{IN} = 0$ to 5.5V
$|I_{LO}|$	I/O Leakage Current			10			10	μA	$\overline{CS} = V_{IH}$, $V_{I/O}$ = GND to VCC
I_{CC}	Power Supply Current		25	40		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, $T_A = 0°C$
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	9.0		2.1	9.0		mA	$V_{OL} = 0.4V$
I_{OH}	Output High Current	−1.0	−2.5		−1.0	−2.5		mA	$V_{OH} = 2.4V$
I_{OS}[2]	Output Short Circuit Current			40			40	mA	$V_{OUT} = GND$

NOTE: 1. Typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.
 2. Duration not to exceed 30 seconds.

CAPACITANCE

$T_A = 25°C$, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O} = 0V$
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels .... 0.8 Volt to 2.0 Volt
Input Rise and Fall Times .... 10 nsec
Input and Output Timing Levels .... 1.5 Volts
Output Load .... 1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114AL-1 Min.	2114AL-1 Max.	2114AL-2 Min.	2114AL-2 Max.	2114AL-3 Min.	2114AL-3 Max.	2114A-4/L-4 Min.	2114A-4/L-4 Max.	2114A-5 Min.	2114A-5 Max.	UNIT
t_{RC}	Read Cycle Time	100		120		150		200		250		ns
t_A	Access Time		100		120		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		70		70		65	ns
t_{CX}	Chip Selection to Output Active	10		10		10		10		10		ns
t_{OTD}	Output 3-state from Deselection		30		35		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		15		15		ns
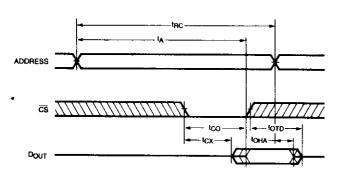
WRITE CYCLE [2]

SYMBOL	PARAMETER	2114AL-1 Min.	2114AL-1 Max.	2114AL-2 Min.	2114AL-2 Max.	2114AL-3 Min.	2114AL-3 Max.	2114A-4/L-4 Min.	2114A-4/L-4 Max.	2114A-5 Min.	2114A-5 Max.	UNIT
t_{WC}	Write Cycle Time	100		120		150		200		250		ns
t_W	Write Time	75		75		90		120		135		ns
t_{WR}	Write Release Time	0		0		0		0		0		ns
t_{OTW}	Output 3-state from Write		30		35		40		50		60	ns
t_{DW}	Data to Write Time Overlap	70		70		90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

WAVEFORMS

READ CYCLE③   WRITE CYCLE
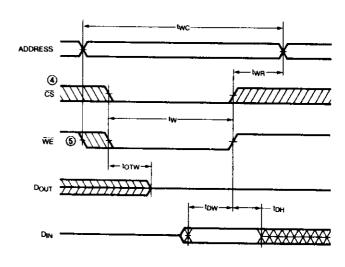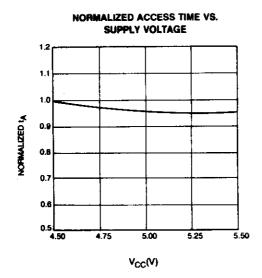

NOTES:
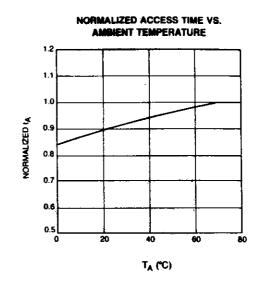3. $\overline{WE}$ is high for a Read Cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
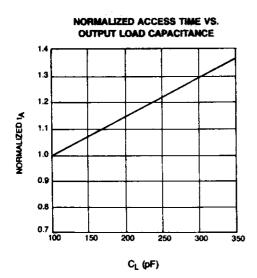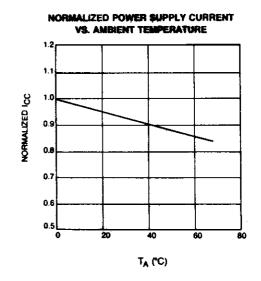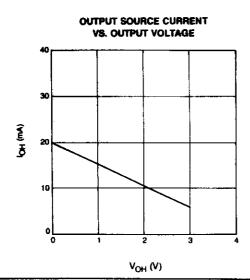5. $\overline{WE}$ must be high during all address transitions.
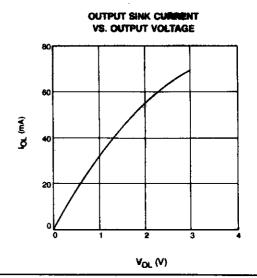
TYPICAL D.C. AND A.C. CHARACTERISTICS

NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE

NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE

NORMALIZED ACCESS TIME VS.
OUTPUT LOAD CAPACITANCE

NORMALIZED POWER SUPPLY CURRENT
VS. AMBIENT TEMPERATURE

OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE

OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE