ENGINEERING SPECIFICATION

Processor - Main Logic Board

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1. SCOPE

This specification describes the NABU 1600 main logic board from a block diagram point of view. It also provides programming information and describes the external interfaces. The internal function and organization of the large scale integrated components are not described in detail. The applicable documents listed in Section 2 will give additional detailed information about these components.

2. APPLICABLE DOCUMENTS

90000430 - 02	NABU 1600 Memory Management Unit Logic Board Engineering Specification
90000440 - 02	NABU 1600 Memory Expansion Board Engineering Specification

WD1001 Winchester Disk Controller OEM Manual

Intel iAPX86 Product Description

Intel iAPX86,88 User's Manual

Intel Component Data Catalog

WD279X-02 Floppy Disk Formatter/Controller Family - Western Digital

3. GENERAL DESCRIPTION

The NABU 1600 main logic board is a 16-bit, general purpose, single-board computer based upon the Intel 8086 family. The board is designed to be mounted in the horizontal plane and is 35.5 cm (14") wide by 30.5 cm (12") deep. All external interface connectors and the reset switch are mounted along the rear edge of the board.

The main logic board contains the following:

a) 8086 micro-processor (clocked at 4.9152 MHZ)
b) Socket for 8087 numeric data processor option
c) Bus arbitration and control logic
d) 256K bytes of dynamic RAM with byte parity
e) Sockets for 8K bytes or 16K bytes of ROM
f) 15 maskable, hardware-vectored interrupts
g) 4-channel DMA controller
h) 2 Interval timer devices providing 6 programmable timers
i) 4 serial I/O ports
j) Floppy disk controller
k) Interface to a hard-disk controller
l) 8-bit parallel expansion interface
m) Connector to accept an optional Memory Management Unit (MMU)
n) Connector to accept an optional Memory Expansion Unit (MEU) which adds 256K bytes of RAM with byte parity.

The on-board ROM is provided to permit self-testing of the board and bootstrapping following a power-on or reset operation.

4. BLOCK DIAGRAM

Figure 1 is a block diagram of the main logic board. The block diagram consists of two sheets. The first shows the processors, controllers and address formation logic. The second shows the memory and I/O data paths. Although some

The main logic board is organized around five busses as follows:

a) AD(15-0) - a 16-bit, bi-directional, multiplexed address and data bus interfacing the processor chip(s) to the rest of the board.

b) A(19-0), BHE/ - the system address bus. Along with the address lines, a control signal BHE/ is used during byte operations to indicate which byte of the 16-bit data bus is carrying valid data.

c) D(16-0) - the bi-directional, system data bus.

d) DB(7-0) - the bi-directional, 8-bit, I/O data bus.

e) DAL(7-0) - the external bidirectional, 8-bit I/O bus for the hard disk and expansion interfaces.

4.1 Conventions

The following conventions are used on the block diagram, and in the following sections:

a) If a slash (/) appears after a signal name, the signal is active in the low state.

b) Signal bit numbers are specified in brackets, most significant first, separated by a dash (-) to indicate all bits inclusive. A list of bits will be separated by a comma (,). For example, (7-4,2) means bits 7 to 4 inclusive, and bit 2.

c) Each block is labelled. The same label is used for the headings in this section and will appear on the schematic drawing where the actual circuitry is shown. (The schematic is not included as part of this specification). The lower right corner of each block contains the sheet number where the labelled function will be found on the schematic.

d) If a hexadecimal number is used, the number will be appended by H. For example, FFH means the hex number FF. Decimal numbers are in conventional form.

e) In references to memory size, the notation K means 1024 decimal. For example, 8K means 8192 (8 x 1024).

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REPLACE WITH BLOCK DIAGRAM SHEET 2

4.2 The Multiplexed Address And Data Bus (AD(15-0))

The 8086 and 8087 chips multiplex this bus so that during the T1 portion of any memory or I/O reference these lines contain the least significant 16 address bits (of a full 20-bit address). The Bus Controller decodes the processor status lines to produce an Address Latch Enable signal (ALE) which causes the Processor Page and Address Latches to be loaded with the address information at the end of the T1 cycle.

During T2, T3, TW and T4 cycles the AD bus is used to carry bi-directioal data. The direction is determined by whether the processor is performing a read or write cycle.

4.3 System Address Bus (A(19-0), BHE/)

The System Address Bus is used to address all of memory and I/O space. Conceptually physical memory may be thought of as being composed of 4K pages. Pages are selected by address bits A(19-12) and addresses within the pages are selected by bits A(11-0) and BHE/.

Sheet 1 of the block diagram shows these two groupings of bits as sub-busses running vertically at the right side of the sheet. One can see that bits A(11-0), BHE/ come from two sources: the Processor Address Latch or the DMA Address Latch/DMA Address Driver. Therefore, either one of the two co-processors (CPU or NDP) can supply the address or the DMA controller can depending on which device controls the bus.

Address bits A(19-12) come from three sources: the Processor Page Latch, the DMA Page Driver or the Memory Management Unit (MMU). As with bits A(11-0), BHE/ when the Memory Management Unit is not installed or is disabled, either of the co-processors or the DMA controller can supply A(19-12).

When the Memory Management Unit is enabled, it supplies bits A(19-12) on behalf of the co-processors or DMA controller. See the MMU engineering specification for details.

4.3.1 Processor Mapping, Page And Address Latches

These three latches are transparent and sample the 20 address bits A19/S7-A16/S3 and AD(15-0) during cycle T1 under control of the Bus Controller signal ALE. They latch the address on the falling edge of ALE near the end of T1.

Processor Page Address Latch outputs AD(19-12) may also be disabled when the MMU is active. In this case, for processor cycles, the Processor Mapping Latch outputs PMA(16-12) are used by the MMU to address its mapping RAM to produce mapped system address bits AD(19-12).

4.3.2 DMA Address Formation

The DMA Controller has an internal 16-bit address register for each of the 4 DMA channels. When it performs a bus cycle it outputs the most significant 8 bits of appropriate address register on its I/O lines DB(7-0) and latches them in the DMA Address Latch by issuing ADSTB. It outputs the least significant 8 bits of the address on its address lines DMAD(7-0) and holds them stable for the entire bus cycle.

The DMA Address Driver drives DMAD(7-0) along with inverted DMAD0 to produce AD(7-0) and BHE/. The DMA Page Driver drives bits 11-8 of the DMA Address Latch to produce AD(11-8).

The DMA Page Address Latch bits (15-12) are sent to the MMU via the DMA mapping driver as MMA(3-0). When the MMU is enabled, these bits are used by the MMU to address its mapping RAM to produce mapped system address bits AD(19-12).

When the MMU is not in use, the DMA Page Driver drives DMA Address Latch bits 15-12 to the System Address Bus AD(15-12).

If the MMU is inactive and DMA channel 0 (Floppy Disk) or 3 (Expansion Interface) is active, the DMA channel 0, 3 Page Driver produces System Address Bus signals AD(19-16). If DMA channel 1 (Hard Disk) is active, the DMA channel 1 Page Driver supplies AD(19-16). The Programmable Parallel Interface Controller port A is used to supply the address

bits to the DMA Channel Page Drivers.

4.4 System Data Bus D(15-0)

The Multiplexed Address and Data Bus AD(15-0) carries addresses during any T1 cycle. During T2, T3, TW and T4 this bus is used to carry data.

Data Bus Transceiver

The Data Bus Transceiver is used to buffer data between the AD bus and the System Data Bus D(15-0). Its direction is controlled by the Processor depending on whether a read or write transfer is being performed by the Processor.

4.5 I/O Data Bus DB(7-0)

This bus carries 8-bit bi-directional I/O data between the System Data Bus and I/O devices.

The two I/O Transceivers are used to interconnect the 16-bit D-bus and the 8-bit DB bus. One transceiver buffers data for the low byte of the D bus; the other is for the high byte. This is necessary because the data is transferred on the high byte for odd addresses (BHE/=0, A0=1) and on the low byte for even address (BHE/=1, A0=0).

4.6 External I/O Data Bus DAL(7-0)

This bus carries 8-bit bidirectional I/O data for the external I/O connectors for the Hard Disk Interface and the Expansion Interface.

The two External Transceivers are used to interconnect the 16-bit D bus and the DAL bus in the same fashion as the I/O Transceivers do for the I/O bus (see section 4.5).

4.7 Direct Memory Access Controller (DMA)

The programmable Direct Memory Access controller has four independent channels to support high-speed data transfer between memory and input-output devices without CPU intervention. The channel assignments, in decreasing order of priority, are:

0 Floppy disk controller
1 Hard disk controller
2 Dynamic RAM Refresh
3 Expansion interface

The DMA asynchronous channel request lines are sampled every clock cycle to determine a request for service. The four channels are initialized to single-transfer mode, ensuring one full CPU machine cycle execution between DMA transfer cycles.

Every 16us a RAM refresh cycle is entered, and the DMA controller channel 2 provides the address. (All row address lines MA(7-0) are refreshed every 2ms). The address is incremented by one after each row refresh, until all 256 rows have been refreshed. The address is then reset, and the cycle repeats. (WARNING: DMA channel 2 must be started before the RAM is used).

The DMA controller addresses 64K bytes of memory. In order to address up to 1 megabyte, four additional high-order bits are supplied by a programmable parallel interface controller.

4.8 Clock Generators

There are two clock generators on the board. The main clock is stabilized by a 14.7456 MHz crystal. The circuit provides a 4.9152 MHz, 33% duty cycle clock signal (CK5MHZ) for the central processor (CPU,8086), the Numeric Data Processor (NDP, 8087), the Bus Arbiter (8289), and the Bus Controller (8288). It is also buffered to the Memory Management Unit. This clock is modified to a 50% duty cycle for the Direct Memory Access Controller (DMA, 8237). A peripheral clock signal (CK2.5MHZ) is generated at 2.4576 MHz, 50% duty cycle for the Serial Interfaces (USART) and the Interval Timers (8253).

A second clock generator stabilized by an 8 MHZ crystal provides the Floppy Disk Controller with a 1 MHZ timing reference for 5 1/4 inch drives or a 2 MHZ reference for 8 inch drives. It also provides, in conjunction with other logic, one clock pulse every 16 microseconds to DMA controller channel 2 for memory refresh.

4.9 Central Processor (8086 CPU)

The main logic board is based on the Intel 8086 16-bit microprocessor, configured in maximum mode to extend system architecture for multiprocessor configurations and instruction set extension co-processors. Its addressable memory capacity is one megabyte, with locations byte or word addressable. The instruction length is variable in byte increments. Processor status signals (S2, S1, S0) are sent to the NDP, Bus Arbiter and Bus Controller to co-ordinate bus activity.

The signals AD(15-0) are the multiplexed address/data lines containing, along with A(19-16) the address bits in the first clock period of a bus cycle, and data bits during the other clock periods.

4.10 Numeric Data Processor (8087 NDP)

The main logic board has provision for an optional Numeric Data Processor, Intel 8087, which provides a full set of floating-point arithmetic functions, as well as exponential, logarithmic and trigonometric functions. It is a co-processor extension to the CPU in terms of architecture and software. It interfaces with the CPU and the system via the Local Address/Data Bus.

4.11 Bus Controller (8288)

The bus controller is configured in system bus mode to provide the system bus control signals. It decodes the processor status lines (S(2-0)/) to determine the command being issued as follows:

S2/	S1/	S0/	Processor State	Command Signal Name
0	0	0	Interrupt Acknowledge	INTA/
0	0	1	I/O Read Command	IORC/
0	1	0	I/O Write Command	IOWC/,AIOWC/
0	1	1	Halt	none
1	0	0	Code Access (Memory read)	MRDC/
1	0	1	Memory read command	MRDC/
1	1	0	Memory write command	MWTC/
1	1	1	Passive	none

In the case of the I/O write decode, two outputs are provided: IOWC/ for normal I/O timing and the Advanced I/O Write Command (AIOWC/) which is issued earlier in the machine cycle to give an I/O device an advanced indication of a write instruction.

In addition to decoding the command, the bus controller provides three other bus control signals as follows:

Signal Name	Description
ALE	Address Latch Enable is used to strobe the address from the processor into a latch. This is necessary to demultiplex addresses from the AD bus (see section 4.3.1).
DEN	Data Enable is used to enable the Data Bus Transceiver.
DATA OUT	Data Output determines the direction of the Data Bus Transceiver. A high indicates data output from the processor; a low indicates data input.

The Bus Controller is enabled by the Bus Arbiter when the processor has control of the system busses. If the DMA controller is granted the bus by the arbiter, the Bus Controller is disabled.

4.12 Bus Arbiter (8289)

The Bus Arbiter is configured in single-bus mode, and coordinates use of the buses by the processors and the DMA controller on a priority basis. The DMA controller has higher priority than the processors.

The active processor issues commands which are decoded by the Bus Arbiter and Bus Controller and is unaware of the existence of the Arbiter. If the Arbiter has granted the use of the system busses to the DMA controller, the Arbiter deactivates its Address Enable (AEN/) output which in turn disables the Bus Controller and causes the Clock Generator to remove the READY indication to the processor. This causes the processor to insert "wait" states until it

is given access to the system bus and the READY signal is again made active.

If the DMA controller requests the system busses, it will be granted access whenever the processor's status lines indicate that it is in an idle or halt state and the processor is not issuing a "Lock" signal.

4.13 Read-Only Memory (ROM)

The board contains 8K bytes of ROM, and has provision for expansion to 16K of ROM. The memory locations are addressed from FEOOOH to FFFFFH. (If the 16K ROM is utilized, the lowest address is FCOOOH). The CPU branches to FFFFOH on a reset or power-up. The ROM is used for self-test and boot strapping. ROM output data is driven onto the D-bus by the ROM Output Driver when the ROM is selected.

4.14 Random Access Memory (RAM)

The read-write memory (RAM) capacity is 256K bytes on the main board, expandable to 512K bytes by addition of the Memory Expansion Unit (MEU).

RAM is organized as two banks of 64K words X 18 bits (two 8-bit bytes with byte parity).

4.15 Parity Logic

The parity generator/checker circuit as active only on RAM data and uses even-parity. When the data byte is written, the generator will provide the parity bit to make the number of one's even. When the data is read, the parity is checked. If the number of one's is odd (including the parity bit), an error interrupt is generated (signal IRPARITY).

4.16 Programmable Interval Timers

Six programmable counters are implemented by two interval timer devices, operating in a square-wave generator mode. One counter is used for the real-time clock, one for diagnostics (error indication), and four as baudrate

generators for the serial interface ports. (See also section 5.2).

4.17 Interrupt Controllers

Two interrupt controller chips provide fifteen maskable vectored interrupt levels. They are listed in decreasing priority as follows:

Master Controller

Level	Source
0	NDP (8087)
1	RAM parity error
2	System call MMU
3	Expansion interface
4	Hard disk
5	Floppy disk
6	Real time clock
7	Slave controller

Slave Controller

Level	Source
0	I/O port 0 receiver ready
1	I/O port 0 transmitter ready
2	I/O port 1 receiver ready
3	I/O port 1 transmitter ready
4	I/O port 2 receiver ready
5	I/O port 2 transmitter ready
6	I/O port 3 receiver ready
7	I/O port 3 transmitter ready

4.18 Serial Interface Ports

There are four serial RS-232C I/O ports. Two are asynchronous; the other two can be configured as synchronous or asynchronous via a jumper strip (J8,J9) for Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). The baudrate is software programmable for each port, in conjunction with an interval timer. One port is normally used for the console, one for the printer, and two for additional terminals or RS-232C

devices.

4.19 Floppy Controller

The floppy disk controller provides the interface signals to the floppy disk drive for 5 1/4" or 8" single-density or double density drives. The logic supports up to four floppy drives. (See also section 5.5).

4.20 Hard Disk Interface

The main logic board interfaces to the hard disk controller (located in the Mass Storage Unit) via an eight-bit bidirectional bus interface transceiver (signals DAL(7-0), the control bus, and the system address bus signals A(2-0) for controller task file address selection.

4.21 Programmable Parallel Interface Controller

The programmable peripheral interface is set to run in basic input/output mode, and has three 8-bit ports. Port A is used to extend the DMA addressing range, Port B is for verifying machine identifier (when implemented), and Port C is used for floppy disk drive select, side select, drive size and double-density select signals.

The Port A output PA(7-0) is driven onto the system address bus through the PA buffer (signals A(19-16), under control of the DMA ontroller (see also Section 5.7).

4.22 Reset

The reset input to the clock circuit will be active for approximately 26 ms following the release of the reset switch or restoration of power. A system reset signal is output from the clock circuit, synchronized with CK5MHZ. This causes the CPU to commence program execution at address FFFFOH. The NDP initializes itself when RESET subsequently becomes inactive. Both the CPU and NDP terminate all activities on detection of the reset signal. The reset also sets the serial interfaces and DMA controller into idle states, sets the peripheral interface ports to input mode, and initializes the Floppy Disk Controller, the Hard Disk Controller, the expansion interface, and the Memory Management Unit.

There is provision on the board for connection of a remote reset switch for testing (J14).

5. PROGRAMMING INFORMATION

Detailed programming information for the following devices will be found in the applicable documents listed in section 2: Intel 8086 CPU, 8087 NDP, 8237 DMA Controller, 8251A Serial Interface, 8253 Interval Timer, 8255 Peripheral Interface, and the 8259 Interrupt Controller, literature. The interface to the Hard Disk Controller board is described in the WD1001 Controller OEM manual from Western Digital.

5.1 Direct Memory Access Controller (8237)

The DMA controller register I/O address assignments are as follows:

Register	Function
60H	floppy disk current address
61H	floppy disk current transfer count
62H	hard disk current address
63H	hard disk current transfer count
64H	RAM refresh current address
65H	RAM refresh current transfer count
66H	expansion interface current address
67H	expansion interface current transfer count
68H	command status
69H	request (write only)
6AH	mask set/reset (write only)
6BH	mode (write only)
6DH	temporary
6FH	write all mask

5.2 Programmable Interval Timer (8253)

The timer register I/O address assignment is as follows:

	Register	Controls
Timer 1:	10H	Real time clock
	11H	Diagnostic LED
	12H	Console port baudrate
	13H	Control register
Timer 2:	1CH	Printer port baudrate
	1DH	I/O spare 1 port baudrate
	1EH	I/O spare 2 port baudrate
	1FH	Control register

After a reset, the counter control only needs to be set up once. The counter rate can be changed anytime afterward by loading the appropriate parameter into the counter register, lower byte first, then the upper byte.

Real Time Clock

The real time clock parameter is determined by the equation:

Decimal parameter = 4915200 / 2 / clock rate in cycles/second.

For 60cps rate this is 40960. Select the interval timer counter 0 in mode 3, binary (timer control register 13H; 00111110), convert 40960 to hex (A000H) and put this value into the counter register 10H.

Baud Rate Generators

The port baudrate can be set from 50 to 19200 baud. The rate parameter is determined by the equation:

rate parameter = 4915200 / 2 / 16 / baudrate

5.3 Interrupt Controller (8251A)

The Interrupt Controller accépts two types of command words (8-bits long); initialization and operation (interrupt modes). Operation words can be written to the controller anytime after initialization.

The register I/O address assignment is:

Master Controller	Slave Controller	Function
40H	50H	initialization word 1 operation word 2
42H	52H	initialization word 2 initialization word 3 initialization word 4 operation word 1

5.4 Serial Interface Ports

The I/O addresses of the ports are:

Port	Function	Status/ Command Register	Data Register
0	console	01H	00H
1	printer	05H	04H
2	I/O port	09H	08H
3	I/O port	0DH	0CH

A set of control words define the complete functional definition of the interface. The control words are in two formats, mode instruction and command instruction. The latter can be written into the interface anytime in the data block during operation.

A status word can be read from the interface anytime during functional operation.

5.5 Floppy Disk Controller

The floppy disk register assignments are as follows:

16H drive select byte
18H data
19H sector
1AH track
1BH command (write only)
1BH status (read only)

The drive select byte format is:

Bits	7	6	5	4	3	2	1	0
	A	B	C	D	E	F	G	0

where A=1 to select drive 0
or B=1 to select drive 1
or C=1 to select drive 2
or D=1 to select drive 3

E=0 side 0
E=1 side 1

F=0 5 1/4" floppy,
F=1 8" floppy,

G=0 double density G=1 single density

The floppy controller accepts eleven commands, reference Western Digital FD279X-02 Floppy Disk Formatter/Controller Family data sheets.

Note: The following must be done to ensure successful read/write operations:

a) Minimum delay of 21 msec performed following a track seek operation.

b) Minimum delay of 2 msec performed following a read/write operation.

c) Minimum delay of 200 usc performed following a change of side select.

5.6 Hard Disk Controller

The hard disk controller is located in the MSU chassis. The CPU can access it as follows:

Register I/O Address	Function
70H	data
71H	error
71H	write-precompensation
72H	sector count
73H	sector number
74H	cylinder low byte
75H	cylinder high byte
76H	sector size; drive; head
77H	status
77H	command

The controller performs disk functions through the task file registers. After the tasks are set, the commands are loaded. After command execution, the status register is loaded, to be read by the host to determine successful execution. Implied track seek is performed in the read/write operation.

5.7 Programmable Parallel Interface Controller

The register I/O address assignment for this peripheral controller is as follows:

14H	Port A	output	the four most significant bits of 20-bit DMA transfer address for hard disk (input bits 7-4) and floppy disk (input bits 3-0).
15H	Port B	input	machine identifier
16H	Port C	output	floppy disk drive selection (see section 5.5)
17H			mode selection

The mode word format is as follows:

Bits	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	1	0

which specifies active mode, basic input/output, port A output, port C(upper) output, mode 0, port B input, and port C (lower) output.

6. INTERFACES

This section has two sub-sections; one describes the external interfaces (accessible without opening the CPU cabinet), the other describes internal interfaces to the main logic board.

Connector identifications on PCB:

J1	Console port
J2	Printer port
J3	Spare (3) port
J4	Spare (2) port
J5	Hard disk interface
J6	Floppy disk interface
J7	Expansion interface
J8	Spare 3 configuration
J9	Spare 2 configuration
J10	Memory Expansion Unit
J11	Memory Management Unit
J12	Power-on LED
J13	Power supply
J14	Remote reset

6.1 External Interfaces

This section describes the user accessible external connectors. They are located along the rear edge of the board.

6.1.1 Input/Output Ports

The board input/output ports are connected to 25-pin D-type female connectors (RS-232C).

The ports for the console and printer are wired for DCE (Data Communications Equipment) as follows:

Pin	Signal	Direction	Description
1	GND	-	Chassis ground
2	TXD	to DCE	Transmit data
3	RXD	from DCE	Receive data
4	RTS	to DCE	Request to send
5	CTS	from DCE	Clear to send
6	DSR	from DCE	Data set ready
7	GND	-	Logic ground
8	DCD	from DCE	Data carrier detect
9-19	-	-	not used
20	DTR	to DCE	Data terminal ready
21-25	-	-	not used

Spare ports are nominally connected as follows:

Pin	Several	Direction	Description
1	GND	-	Chassis ground
2	TXD	to DCE	Transmit data
3	RXD	from DCE	Receive data
4	RTS	to DCE	Request to send
5	CTS	from DCE	Clear to send
6	DSR	from DCE	Data set ready
7	GND	-	Logic ground
8	DCD	from DCE	Data carrier detect
9-19	-	-	not used
> 15	TXC	from DCE	Transmit clock (DCE source)
16	-	-	not used
> 17	RXC	from DCE	Receive clock (DCE source)
18,19	-	-	not used
20	DTR	to DCE	Data terminal ready
21-23	-	-	not used
> 24	TXC	to DCE	Transmit clock (DTE source)
25	-	-	not used

6.1.2 Hard Disk

A 37-pin female D-type connector is used as follows:

Pin	Signal	Direction	Description
2	DAL1	in/out	Data bit 1
3	DAL2	in/out	Data bit 2
4	DAL3	in/out	Data bit 3
5	DAL4	in/out	Data bit 4
6	DAL5	in/out	Data bit 5
7	DAL6	in/out	Data bit 6
8	DAL7	in/out	Data bit 7
9	HDA0	out	Address bit 0
10	HDA1	out	Address bit 1
11	HDA2	out	Address bit 2
12	ENHDISK/	out	Device select
13	EXAIOWC/	out	I/O write command
14	EXIORC/	out	I/O read command
15	HDWAIT/	in	Wait signal
16	EXRESET/	out	Reset signal
17	-	-	not used
18	HDIR	in	Interrupt request signal
19	HDDREQ	in	Data request
20-36	GND	-	Logic ground
37	-	-	Not used

6.1.3 Floppy Disk

A 37-pin female D-type connector is used as follows:

Pin	Signal	Direction	Description
1-19	GND	-	logic ground
20,21	-	-	not used
22	DS4/	out	Drive select 4
23	IP/	in	Index
24	DS1/	out	Drive select 1
25	DS2/	out	Drive select 2
26	DS3/	out	Drive select 3
27	Motor On/	out	Start motor or load head
28	DIR	out	R/W head direction (0 in, 1 out)
29	STEP/	out	Step pulse
30	WD/	out	Data to be written
31	WG/	out	Write gate enable
32	TK00/	in	Active when head at track 0
33	WP/	in	Active when write protected
34	RD/	in	Data read from diskette
35	SS	out	Side Select
36,37	-	-	not used

6.1.4 Expansion Interface

A 37-pin female D-type connector is used as follows (identified as EXPANSION on cabinet):

Pin	Signal	Direction	Description
1	DAL0	in/out	Data bit 0
3	DAL1	in/out	Data bit 1
5	DAL2	in/out	Data bit 2
7	DAL3	in/out	Data bit 3
9	DAL4	in/out	Data bit 4
11	DAL5	in/out	Data bit 5
13	DAL6	in/out	Data bit 6
15	DAL7	in/out	Data bit 7
17	EXA0	out	Address bit 0
19	EXA1	out	Address bit 1
21	EXA2	out	Address bit 2
23	ENEXPAN/	out	Device select
25	EXAIOWC/	out	I/O write command
27	EXIORC/	out	I/O read command
29	EXWAIT/	in	wait request signal
31	EXRESET/	out	reset signal
33	-	-	not used
35	EXIR	in	interrupt request signal
37	EXDREQ	in	data request
39	-	-	not used

All even-numbered pins (2-40) are signal ground.

6.1.5 Reset Switch

The user-accessable reset switch, mounted on the rear edge of the board, is used to initialize the system. Internal connector J14 provides for a remote reset switch for testing purposes.

6.2 Internal Interfaces

This section describes the connector interfaces on the main board for the piggy-back mounted option boards, and the power connections.

6.2.1 Memory Expansion Unit (J10)

The 56-pin connector assignment is as follows:

Pin	Signal	Direction	Description
1	VCC	----	+5v
2	GND	----	Logic Ground
3	BHE/	OUT	----
4	VCC	----	+5v
5	D8	IN/OUT	Data bit 8
6	D0	IN/OUT	Data bit 0
7	D7	IN/OUT	Data bit 7
8	D15	IN/OUT	Data bit 15
9	D9	IN/OUT	Data bit 9
10	D1	IN/OUT	Data bit 1
11	D6	IN/OUT	Data bit 6
12	D14	IN/OUT	Data bit 14
13	D10	IN/OUT	Data bit 10
14	D2	IN/OUT	Data bit 2
15	D5	IN/OUT	Data bit 5
16	D13	IN/OUT	Data bit 13
17	D11	IN/OUT	Data bit 11
18	D3	IN/OUT	Data bit 3
19	D4	IN/OUT	Data bit 4
20	D12	IN/OUT	Data bit 12
21	GND	----	Logic ground
22	VCC	----	+5v
23	A18	OUT	Address bit 18
24	A17	OUT	Address bit 17
25	A19	OUT	Address bit 19
26	MEUSEL	OUT	Row/Col address select
27	MEUDINPH	OUT	Parity bit to be written to the high bank
28	MEUCAS/	OUT	Column address strobe
29	MRDC/	OUT	Memory read command
30	MWTC/	OUT	Memory write command
31	REFRESH/	OUT	Memory refresh

Pin	Signal	Direction	Description
32	MEUDINPL	OUT	Parity bit to be written to the low bank
33	VCC	---	+5V
34	GND	---	Logic ground
35	AO	OUT	Address bit 0
36	DOUTPL	OUT	Parity bit to be read from the low bank
37	A9	OUT	Address bit 9
38	A7	OUT	Address bit 7
39	A11	OUT	Address bit 11
40	A16	OUT	Address bit 16
41	A13	OUT	Address bit 13
42	A8	OUT	Address bit 8
43	DOUTPH	OUT	Parity bit to be read from the high bank
44	GND	---	Logic ground
45	A15	OUT	Address bit 15
46	A6	OUT	Address bit 6
47	A1	OUT	Address bit 1
48	A14	OUT	Address bit 14
49	A10	OUT	Address bit 10
50	A5	OUT	Address bit 5
51	A2	OUT	Address bit 2
52	A4	OUT	Address bit 4
53	A12	OUT	Address bit 12
54	A3	OUT	Address bit 3
55	VCC	---	+5V
56	GND	---	Logic ground

6.2.2 Memory Management Unit (J11)

The 86-pin connector assignment is as follows:

Pin	Signal	Direction	Description
1	VCC	----	+5V
2	VCC	----	+5V
3	---	----	Not used
4	IRMMU	IN	Interrupt request from MMU
5	DO	IN/OUT	Data bit 0
6	D7	IN/OUT	Data bit 7
7	GND	----	Logic ground
8	RESET/	OUT	Reset
9	D1	IN/OUT	Data bit 1
10	D6	IN/OUT	Data bit 6
11	GND	----	Logic ground
12	GND	----	Logic ground
13	D2	IN/OUT	Data bit 2
14	D5	IN/OUT	Data bit 5
15	GND	----	Logic ground
16	GND	----	Logic ground
17	D3	IN/OUT	Data bit 3
18	D4	IN/OUT	Data bit 4
19	GND	----	Logic ground
20	GND	----	Logic ground
21	VCC	----	+5V
22	VCC	----	+5V
23	MWDIS/	IN	Memory write disable
24	DACKHD/	OUT	Channel 1 data acknowledge
25	---	----	Not used
26	INTA/	OUT	Interrupt acknowledge
27	---	----	Not used
28	NMI	IN	Non-maskable interrupt from MMU

Pin	Signal	Direction	Description
29	---	----	Not used
30	---	----	Not used
31	IODIS/	IN	I/O disable
32	---	----	
33	GND	----	Logic ground
34	GND	----	Logic ground
35	AO	OUT	Address bit 0
36	DACKFD/	OUT	Channel 0 data acknowledge
37	A9	OUT	Address bit 9
38	A7	OUT	Address bit 7
39	A11	OUT	Address bit 11
40	A16	OUT	Address bit 16
41	A13	OUT	Address bit 13
42	A8	OUT	Address bit 8
43	GND	---	Logic ground
44	GND	---	Logic ground
45	A15	OUT	Address bit 15
46	A6	OUT	Address bit 6
47	A1	OUT	Address bit 1
48	A14	OUT	Address bit 14
49	A10	OUT	Address bit 10
50	A5	OUT	Address bit 5
51	A2	OUT	Address bit 2
52	A4	OUT	Address bit 4
53	A12	OUT	Address bit 12
54	A3	OUT	Address bit 3
55	GND	---	Logic ground
56	GND	---	Logic ground
57	A19	OUT	Address bit 19
58	DMA12	OUT	Buffered address bit 12
59	A18	OUT	Address bit 18
60	DMA14	OUT	Buffered address bit 14
61	A17	OUT	Address bit 17
62	DMA13	OUT	Buffered address bit 13
63	DMA15	OUT	Buffered address bit 15
64	DACKEXP/	OUT	Channel 3 data acknowledge
65	DMA16	OUT	Buffered address bit 16
66	ADRDIS/	IN	Address disable

Pin	Signal	Direction	Description
67	MMUS6	OUT	Multiplexed address bit 19 and status bit 6
68	MMUIOWC/	OUT	I/O write command
69	---	---	NC
70	MMUAEN	OUT	Address enable
71	MMU5MHZ	OUT	Buffered 5MHz system clock
72	MMUS2/	OUT	CPU status bit 2
73	MMUAIOW	OUT	Advanced I/O write command
74	MMUS1	OUT	CPU status bit 1
75	MMUSO/	OUT	CPU status bit 0
76	MMUS5	OUT	Multiplexed address 18 and status bit 5
77	MMUIORC/	OUT	I/O read command
78	MMUALE	OUT	Address latch enable
79	VCC	---	+5V
80	VCC	---	+5V
81	MMA1	OUT	Address bit 1 for MMU address translator
82	MMAO	OUT	Address bit 0 for MMU address translator
83	MMA3	OUT	Address bit 3 for MMU address translator
84	MMA2	OUT	Address bit 2 for MMU address translator
85	GND	---	Logic ground
86	GND	---	Logic ground

6.2.3 Power Supply

The OEM power supply connector pin assignment is as follows:

Pin	Voltage	Current (excl.MMU & MEU)
1	+12	350 ma
2	-12	300 ma
3	GND	
4	+5	