VISUAL TECHNOLOGY INCORPORATED, 540 MAIN STREET, TEWKSBURY, MA 01876

V1050
PERSONAL COMPUTER
MAINTENANCE MANUAL

March 1984

SAFETY WARNING

Hazardous voltages 115, 220 VAC and 15 KV DC are present when the terminal is on, and may remain after power is removed. Use caution when working on internal circuits, and do not work alone.

Caution is required when handling the cathode ray tube as the internal phosphor is toxic. Safety goggles and gloves must be used whenever the CRT tube is handled. If the tube should break, and skin or eyes are exposed to the phosphor, rinse the affected area with cold water and consult a physician.

This terminal is supplied with a cord set which includes a safety ground. Do not use this terminal with an ungrounded outlet, or a missing ground pin, or use any adaptor which will defeat the safety ground.

Insure that the power is turned off before connecting or disconnecting the keyboard cable.

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1. ARCHITECTURE

The Visual 1050 is a user programmable personal computer with graphics display capability.

The standard system includes a computer with a 12 inch display screen, a keyboard, an RS-232 serial asynchronous interface, and two 400 KB mini-diskette drives with a total storage capacity of 800 KB plus a Parallel and Winchester interfaces.

Optional equipment is available to expand the capacity of the system. The standard mini-diskette drives can be supplemented by a Winchester hard disk drive which provides an additional 10MB of storage. The V1050 can interface to parallel matrix printers, to letter quality printers, and graphic printers to produce both graphic and letter quality reports. An intelligent asynchronous/synchronous communication card will be available for interfacing to other computer.

The following sections of the manual describe the computer portion of the system and its interface to the video monitor, the keyboard, RS232 port, printer, mini-diskette drives and Winchester drive. The computer is described in technical detail at the system programmer's level.

When speaking of large numbers which are binary related the symbol "K" is used to represent the number 1024. A hexadecimal number will be denoted by the letter H.

The Visual 1050 is a Z80 microprocessor based computer composed SSI, MSI, and LSI logic elements and 6502 for the video.

The program memory consists of 128K bytes of RAM controlled by the Z80. It is organized as 16-64Kx1 devices.

The video memory consists of 32K x 10 of RAM controlled by the 6502. It is organized as 20-16Kx1.

The system ports of the V1050 are the following, RS-232 for interfacing to systems or modems, a Centronics Parallel port for printers or other parallel devices, and Winchester Disc port.

The V1050 features a standard display of 25 lines x 80 columns, green phosphor, high resolution, programmable character set, 640 x 300 bit mapped graphics display, and a tilt swivel display.

2. THEORY OF OPERATION

2.1 TIMING

The video timing is generated by a crystal oscillator operating at 15.36 MHz, shown as location Y1, on sheet 8 combined with U17 on sheet 8 to form the 15.36 MHz oscillator circuit. The symmetrical clock from this circuit drives the binary counter (U19 on sheet 8) to form the 6502CLK (.96MHz), SYSTEMCLK (.96MHz), CHARCLK (1.92MHz). Also operating from the symmetrical clock is the DOTCLK (15.36MHz).

The real time clock time base is derived from a crystal operating at 32.768 kHz (Y2 on sheet 4 of the schematics).

The timing for the Z80 CPU is derived from the crystal Y3 operating at 16 MHz, (on sheet 2), which combined with U66 page 2 forms the 16 MHz oscillator circuit. The symmetrical clock from this circuit drives the binary counter (U47 sheet 2) to form the, 1 MHz, 2 MHz, 4 MHz and 8 MHz clocks. All the clocks from U47 and U46 (sheet 2) are cleaned up by ferrite beads F2 thru F6 on sheet 2. U46 is used to invert, 1 MHz, 2 MHz, and 4 MHz clocks.

The 1 MHz clock is used by U13 (sheet 6) to control the floppy disc interface.

The 2 MHz clock is used by the serial interface U9 on (sheet 5), the keyboard interface U85 (sheet 4) and U40, (sheet 6), which uses it in combination with the 4 MHz to form the window signal used by the floppy disc precomp circuit.

The 4 MHz clock is used by the Z80, (U80 sheet 2), and by U38, (sheet 2) which controls the interrupts to the Z80 and U73 (sheet 2) to generate a wait state during ROM access.

The 8 MHz clock is used for data separation by U25 (sheet 6) for the floppy disc interface.

2.2 CENTRAL PROCESSOR UNIT

The central processor unit performs the control, arithmetic, and logic functions for the processing section. An eight-bit Z80A microproccessor is used because of the large base of software written for this chip.

The Z-80, U80 (sheet 2), running at 4 megahertz from U46, (sheet 2), provides both a 16 bit address bus and a bi-direction 8-bit data bus for communication with the memory and input/output (I/O) devices.

The instructional set of the Z80 is summarized in the IC Data Section 5. A more elaborate description of each instruction can be found in any of the numerous books on the Z-80.

The RESET signal for the Z-80 and the 6502 is provided by the circuit R62, C78, CR6, and U50 which provides a positive going signal which is inverted by U7, (sheet 20), before being presented to the Z80 (U80, sheet 2) and the 6502, (U76, sheet 9).

A Wait command is generated by U73, (sheet 2), by the following conditions: first, with the boot enabled, any access of the boot ROM will cause a wait state;

second, the expansion connectors (J7 & J8) may cause wait states depending on which option boards are installed: third, the Winchester interface may cause wait delays, depending on its own needs.

The control signals from the Z-8Ø (U80 sheet 2) are combined by U68, U69 and U70 (sheet 2) into memory read and write, I/O read and write, and also the interrupt acknowledge for use throughout the Z8Ø section.

The data bus from the Z8Ø is pulled high to decrease noise and to guarantee a float high condition needed by the interrupt controller. The two most significant bits of the address bus are latched every memory request cycle by U84. This insures that any bank switching will not change state unless only the address is changed.

The demultiplexers U81 and U82 (sheet 2) provide address decoding for most of the devices on the Z8Ø bus. U81 decodes the addresses for I/O only, where as U82 decodes to both I/O and memory mapped (devices using these decodes also perform I/O read and write separately). The address and functions of the I/O map may be found on page 6 of the V1050 block diagrams. A complete breakdown of the I/O map is contained in the V1050 system I/O map section of this manual.

Interrupts are handled by U38, (sheet 2), an interrupt priority encoder, and gates U37, U42, and U48, acting as an interrupt mask ANDing with the mask data from port B of the PIO U36 (sheet 4). Interrupts are received on pins 15 thru 22 of U38 from the interrupting device, and ANDed with the mask. On receiving an interrupt, assuming U38 is initialized, INT (pin 5) goes low setting flip-flop U21. The output of the flop goes to the Z8Ø INT input. If interrupts are enabled, the Z8Ø, at the appropriate time, will issue an interrupt acknowledge to the interrupt encoder U38 and clears. This causes U38 to place on the bus three bits indicating which interrupt has occurred. These bits are augmented by U51 which causes bit zero to be read as a zero on every interrupt acknowledge. In addition, the upper nybble of data is guaranteed to be all ones by the pull-ups on the data bus.

2.3 DYNAMIC RAM MEMORY

The Dynamic Ram Memory of the V1050 consists of U1Ø3 thru U11Ø and U126 thru U133, (sheet 3), for a total memory of 128K x 8 bits. The addresses for these devices are multiplexed by U102 and U125 on (sheet 3). The multiplexers U102 and U125 are controlled by the flip-flop U34 (sheet 3). U34 also provides all of the timing for the memory CAS (Column Address Strobe). The hardware for the 128K array is broken into two sections. Both sections are refreshed at the same time, but only one section is accessed at one time. The octal buffer U111 puts the RAM data on the bus when enabled by U70 (sheet 3). On Board and Memory Read signals are ANDed. Selection, of the RAM section, is controlled by the RAM

bank switch circuitry. In this circuit, U87, (sheet 3), acts as an I/O port latching a byte which is demuxed by U61, (sheet 3). The outputs of U61 represents logical RAM Pages, 0, 1, and 2. The other half of U61 demuxes the two most significant bits of the address bus 14 and 15. Its output represents the four separate 16K parts that make up the 64K of RAM. Two gates of U71, (sheet 3), are used to modify the two most significant bits of address going to the RAM multiplexers. All together, these provides a method of switching between three logical pages using two physical pages of RAM. This is done because the operating system requires that some of the physical memory be shared as command address space in all banks (refer to the block diagram figure 2.3).

2.4 BOOT ROM

The Boot ROM, U86 (sheet 3), receives its address directly from the Z8Ø and puts its data directly on the data bus. It is enabled by the least significant bit of the bank switch port U87 (sheet 3), and Memory Read.

2.5 REAL TIME CLOCK

The Real Time Clock (RTC) and interrupt mask are both a function of (U36 sheet 4), which is an 8255 IC. Port B of the 8255 is the latched interrupt that goes to the bank of gates and banks discussesd in section 2.3. Port C of U36 bits 0,1,2, are jumpered to ground and are reserved for future use. The remainder of the bits (3 thru 7) of port C are used by U26, (sheet 4), which is the real time clock. All lines of U26 are pulled up to VCC except pin 1. This is done to prevent accidental writing to the RCT registers before the 8255 U36 is initialized. The timing for U36 and U26 is provided by crystal Y2 operating at 32.768 kHz. When the power is turned off the lithium battery provides power for the real time clock. The expected battery life is 5 years.

2.6 KEYBOARD

The keyboard of the V1050 operates in a serial fashion over a telephone type modular cable. The V1050 issues scanning commands and bell commands to the keyboard. Scanning and code generation, and serialization are accomplished on the keyboard by the use of a microprocessor (8039) and a firmware PROM. The keyboard interface is accomplished by the USART U85, (sheet 4) which takes the parallel data and converts it to serial format to send to the keyboard. The Keytronics part number for the keyboard is 6502616-052.

2.7 WINCHESTER INTERFACE

The data bus for the Winchester Interface goes through the bidirectional transceiver U3 (sheet 4), to the connector J4, pins 1 through 8. The address bus bits Ø thru 3 go through U4 (sheet 4) to J4 pins 9 through 12. Reset is on J4, pin 18: Write Data is on pin 15, Read Data is on pin 14; and Write Select is on pin 13. An Interrupt is on pin 17, and Wait is on pin 16 from the drive.

2.8 SERIAL INTERFACE

The Serial Interface, J6, is the RS232 interface to computers or modems. U9 (sheet 5), which is an 8251, converts the parallel data from the data bus to serial data thru the 1488, U8 (sheet 5), to pin 2 of J6 the communication port. Serial data comes from a host device through pin 3 of J6 to the 1489 U22, (sheet 5), to U9 which converts the serial data to parallel.

2.9 PARALLEL INTERFACE

The parallel interface J5 (pins 1-9) is used for interfacing to printers. Port B, of the 8255 controls (U10 sheet 5), the data to the printer. Port C pin controls the printer stobe. Ports A and C also provide control signals for the floppy disk interface, which is discussed in the Section 2.10.

2.10 FLOPPY DISK INTERFACE

The Floppy Disk Interface is controlled by U13, (sheet 6), which is 1793 IC. This IC is explained further in the IC data section of the manual. U13 provides two interrupts which are enabled and disabled by U1Ø, which is an 8255 IC (sheet 5). One interrupt goes directly to NMI of the Z8Ø and the other goes to U79. The clock rate for the U13 is set at 1 MHz for operation with 5-1/4 inch drives only. Write Data is ANDed with window, from U40 before going to the shift register pin 1Ø of U23, (sheet 6). The window insures that data will fall within the proper clock transistions to the floppy disk. The early and late signals from U13 plus the precomp enable from U1Ø (sheet 5) go to U23 (sheet 6) to select the precomp on and off. The shift register U24 is clocked at 4 MHz. The output data to the floppy disk is buffered through U12 (sheet 6) to J3. The output pins of J3 are 6, 1Ø, 12, and 14. When reading data from the floppy disk, the input pins are 26, 28, 3Ø and 34, through U50 to U25 which acts as a data separator. This data is clocked at 8 MHz to U13 which converts the data to the data bus. The motor control is turned off and on by U10 (sheet 5), which is controlled by firmware.

2.11 VIDEO SECTION

The 6502 U76, (sheet 9), controls the video section of the V1050. The 6502 operating at 0.96 MHz, with no wait states, provides both an 16-bit address bus and a 8-bit bidirectional data bus for communication with the memory and I/O devices. Since the 6502 has no unique I/O instructions, all I/O devices are memory mapped, between location ØØØØ and 3FFF memory locations.

The video memory consists of sixteen 4116 dynamic RAM chips which yield 32K bytes of memory. The location of these IC's are U92 through U97 and U114 through U123 on sheet 10. Four of the IC's are used for attributes. These four IC's are U96, U97, U121, and U123. The display interface is implemented with an 8255 (U101 sheet 9). Port B of U1Ø1 sends data to the CRT, while port A receives data from the CRT. Port C of U1Ø1 provides the handshake between data being sent to and from the CRT. U21 (sheet 7) and U6 (sheet 9) provides the interrupts for enabling the 6502 and the Z8Ø.

The 6502 controls the CRT controller U75 (sheet 9), which is a 6845. The 6845 controls the following to the CRT: raster, vertical sync, line count and horizontal sync.

2.12 SELF TEST

Every time the V1050 is powered up a self test is performed. The boot ROM U86 (sheet 3), checks ROM, RAM, and initializes the hardware. There are two different diagnostics, one for I/O operation and the other for screen alignment.

When the V1050 is powered on, the Z8Ø will start executing at location 0000. Once the stack has been set the display interface U101, (sheet 9), is initialized and resets the display. A hash total test is performed: if the hash total test fails, at this point the system is halted and there is no display on the CRT section of the CRT. If the V1050 passes the hash test then the dynamic RAM is tested. If the RAM test fails, it will attempt to display the error message on the screen.

Then the floppy disc controller, keyboard interface, and the auxilary interface are initialized; by this process eight temporary interrupt service routines are built. The floppy controller default values are set up, which will initialize the interrupt controller and enable the interrupts. At this point a message is sent to the display to insert the disk into the floppy drive.

When the left drive, Ø, is selected, the firmware will attempt to read the first sector of the disc. The system will check the drive again for a floppy disc. The firmware will check drive Ø for a floppy disc until the counter reaches a certain number. Then the drive will stop spinning and a message will appear on the screen telling the operator, to "depress any key once a disc is installed in the drive."

2.13 V1050 SYSTEM I/O MAP

Address	Function	LSI Device
84H | 87H	Display Interface	8255
88H | 8BH	Keyboard Interface	8251
8CH | 8FH	Serial Interface (RS-232)	8251
90H | 93H	Parallel Interface/Misc.	8255
94H | 97H	Floppy Interface	1793
9CH | 9FH	Real-Time Clock/Interrupt Mask	8255
AOH | AFH	Vert. Interrupt Clear	74LS74
BOH | BFH	Display Interrupt Clear	74LS74
COH | CFH	Interrupt Register	8214
DOH | DFH	Boot/Memory Bank Select	74LS175
EOH | EFH	Winchester Interface	74LS245

Address: 84H — 87H
Function: Display Interface (8255)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

PORT A (input)
Received data from display

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

PORT B (output)
Transmitted data to display

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

PORT C
- 1 = Display Ready
- INTE B (must be 1)
- 1 = Received data from display
- INTE A (must be 1)
- Read Acknowledge strobe to display (high-low-high)
- Write strobe to display (high-low-high)

****NOTE: bits are modified using the bit set/reset function in the control port

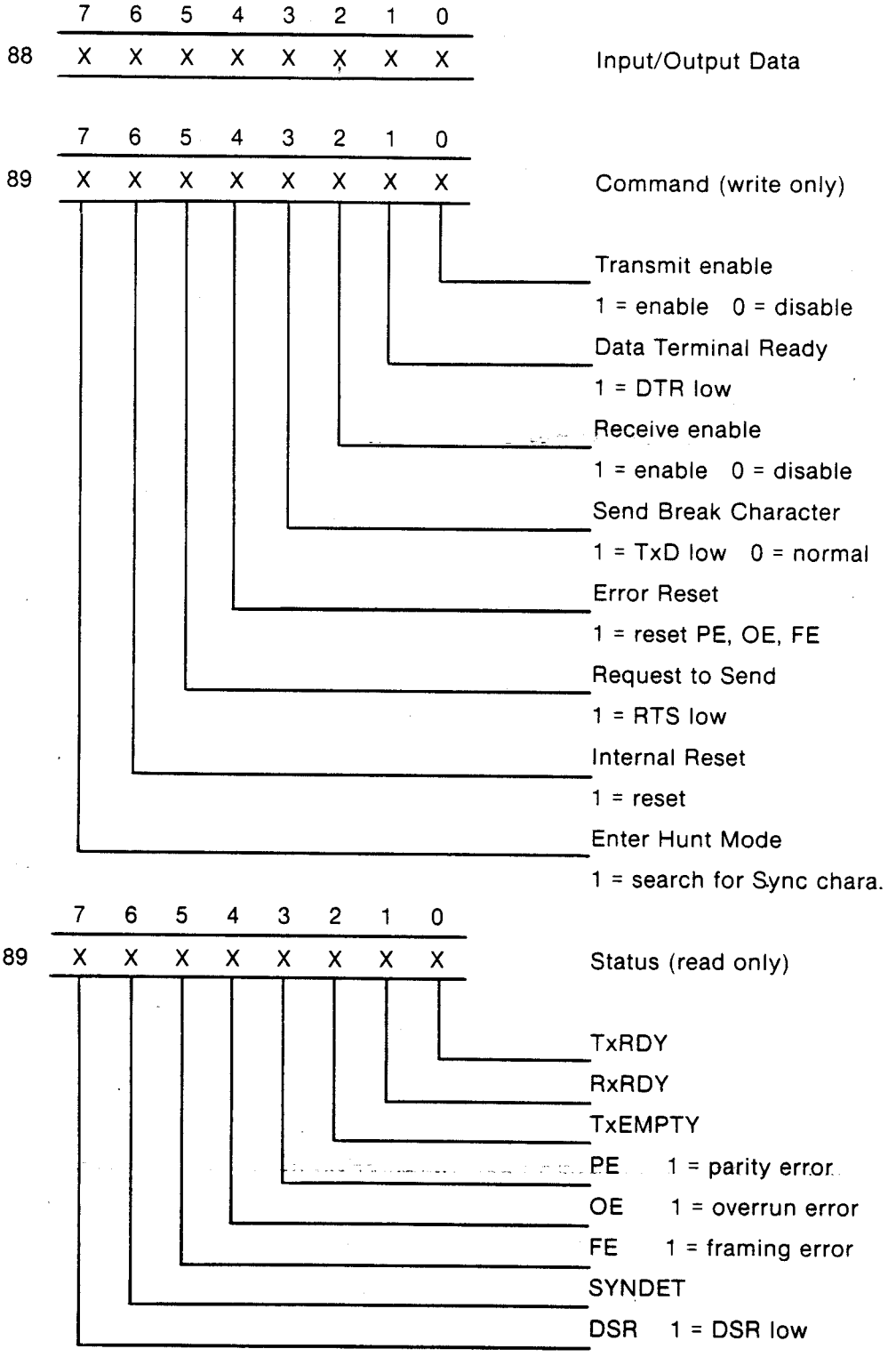
7	6	5	4	3	2	1	0

CONTROL
- 1 = set / 0 = reset
- x (don't care)
- bit set/reset flag
  0 = active

3	2	1	
0	0	0	port c bit 0
0	0	1	port c bit 1
0	1	0	port c bit 2
0	1	1	port c bit 3
1	0	0	port c bit 4
1	0	1	port c bit 5
1	1	0	port c bit 6
1	1	1	port c bit 7

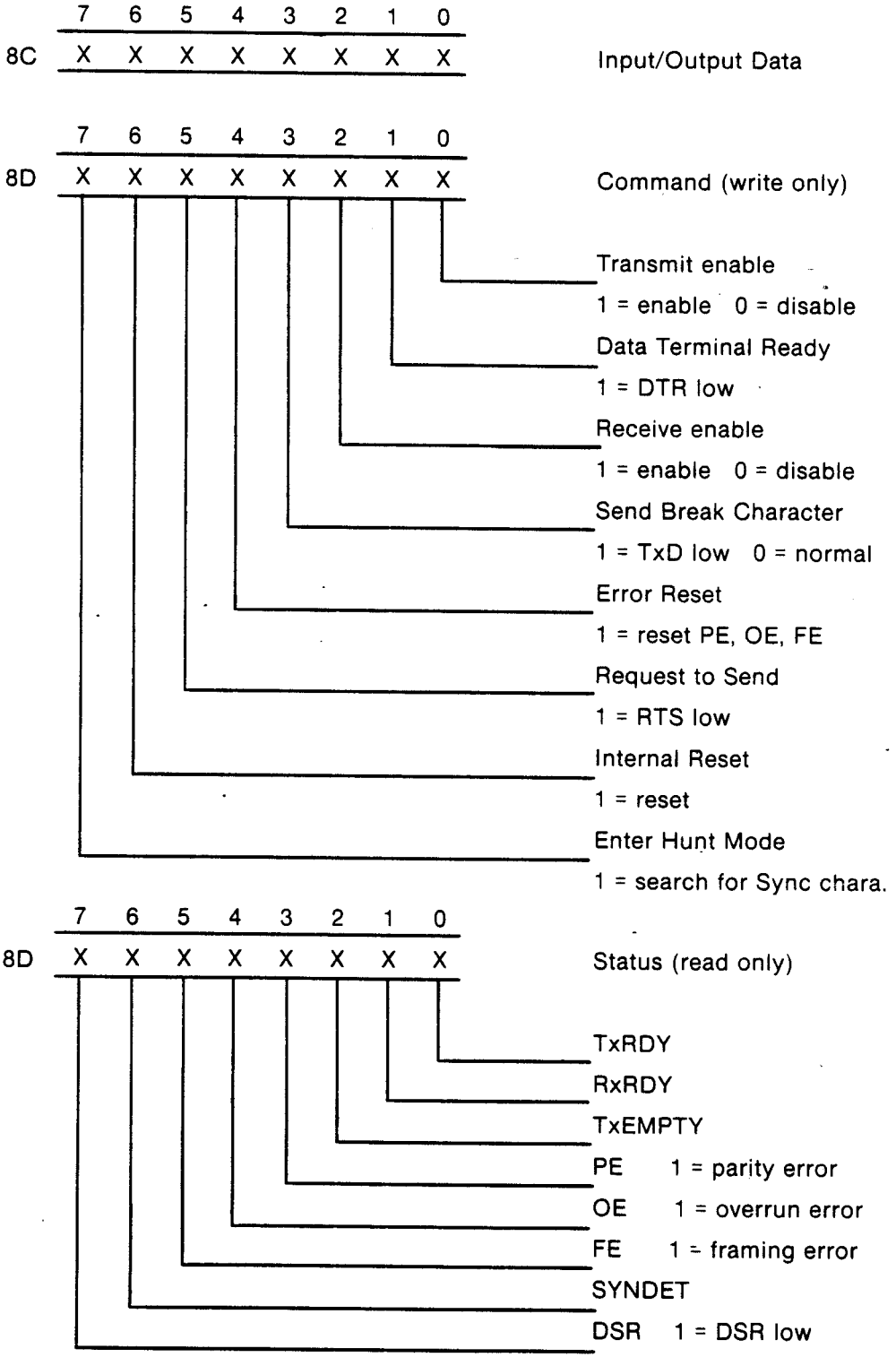
CONTROL must be initialized to B4H for selection of mode 1 of both groups, port A as input, port B as output, and port C handshake.

Address: 88H — 8BH
Function: Display Interface (8251A)



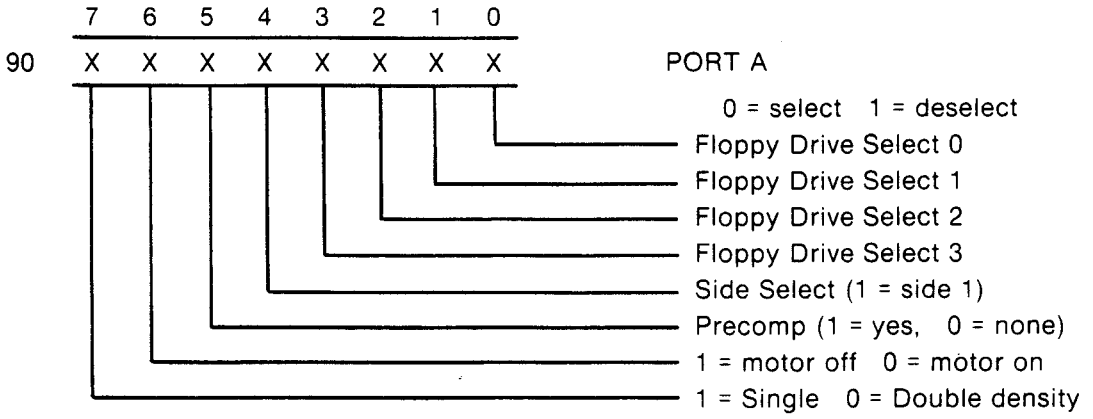
8A and 8B should not be used

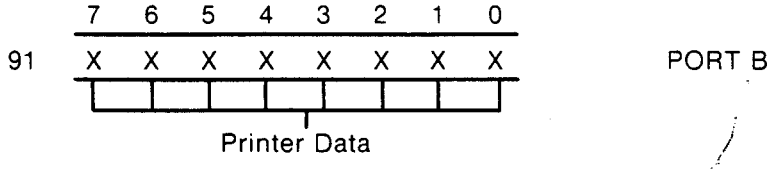
Address: 8CH — 8FH
Function: Serial (RS-232) Interface (8251A)

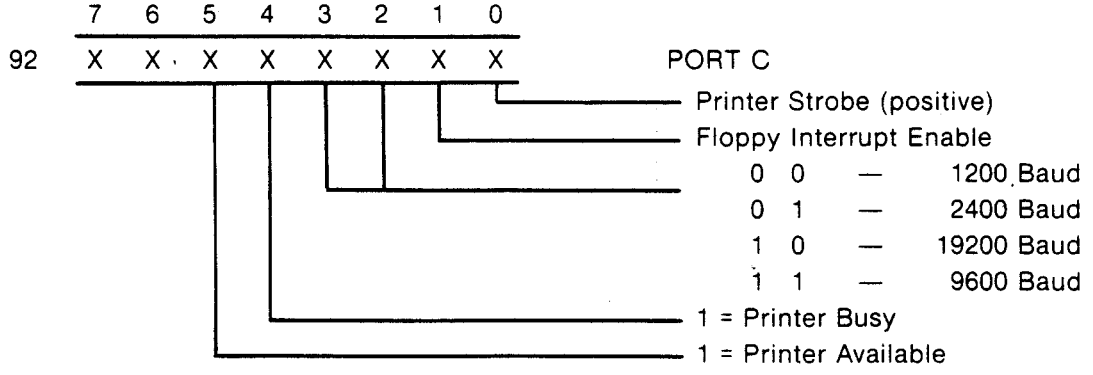


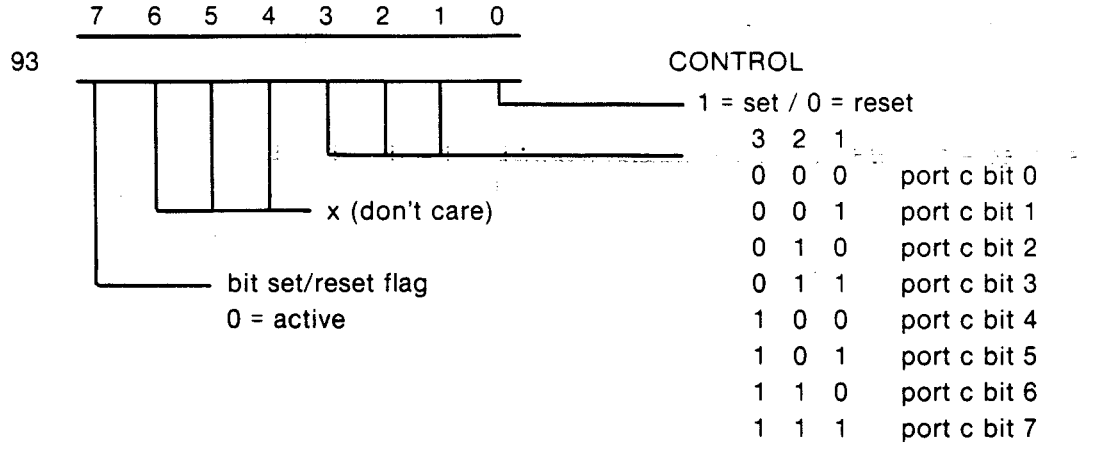
8C and 8F should not be used

Address: 90H — 93H
Function: Printer/Floppy Control









Address: 94H — 97H
Function: Floppy Disc Interface

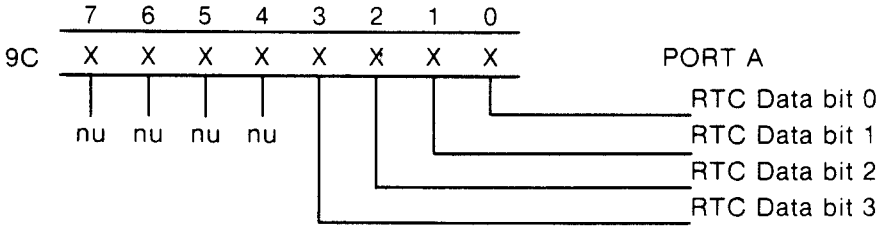
	7	6	5	4	3	2	1	0	
94	X	X	X	X	X	X	X	X	STATUS/COMMAND

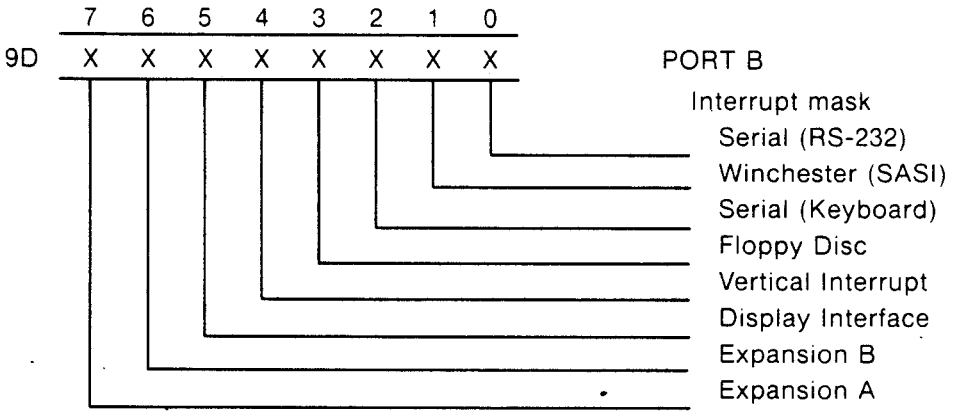
	7	6	5	4	3	2	1	0	
95	X	X	X	X	X	X	X	X	TRACK/TRACK

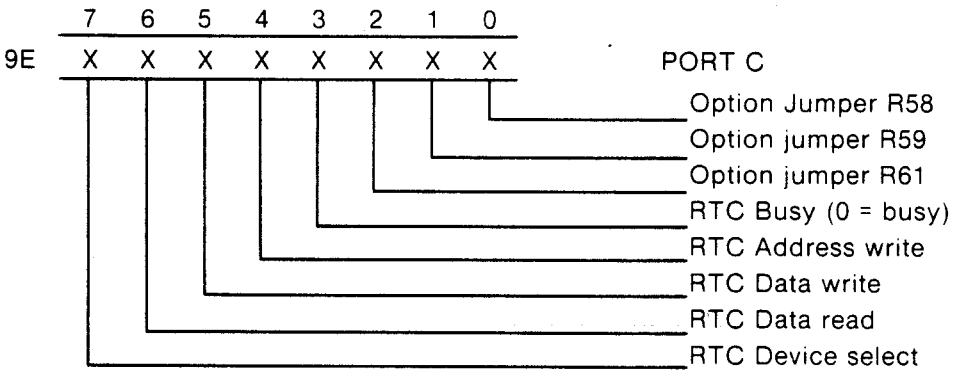
	7	6	5	4	3	2	1	0	
96	X	X	X	X	X	X	X	X	SECTOR/SECTOR

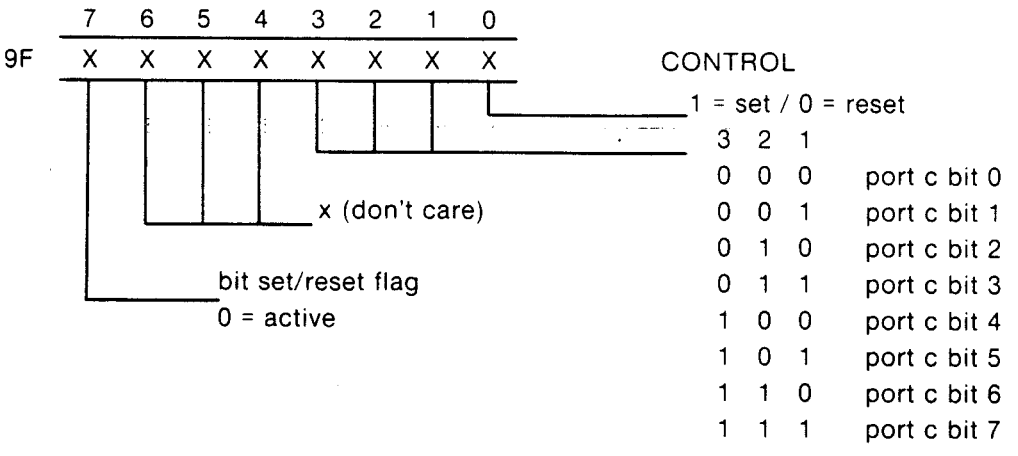
	7	6	5	4	3	2	1	0	
97	X	X	X	X	X	X	X	X	DATA/DATA

Address: 9CH — 9FH
Function: Real Time Clock/Interrupt Mask









Address: AOH — AFH
Function: Vertical Interrupt Clear

	7	6	5	4	3	2	1	0
A0	X	X	X	X	X	X	X	X

Any read or write to this address will clear the Vertical Interrupt.

A1 — AF should not be used

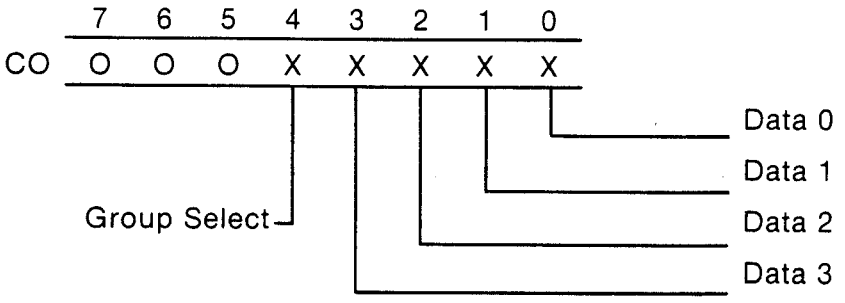
Address: BOH — BFH
Function: Display Interrupt

	7	6	5	4	3	2	1	0
B0	X	X	X	X	X	X	X	X

Any read or write to this address will clear the Display Interrupt.

B1 — BF should not be used

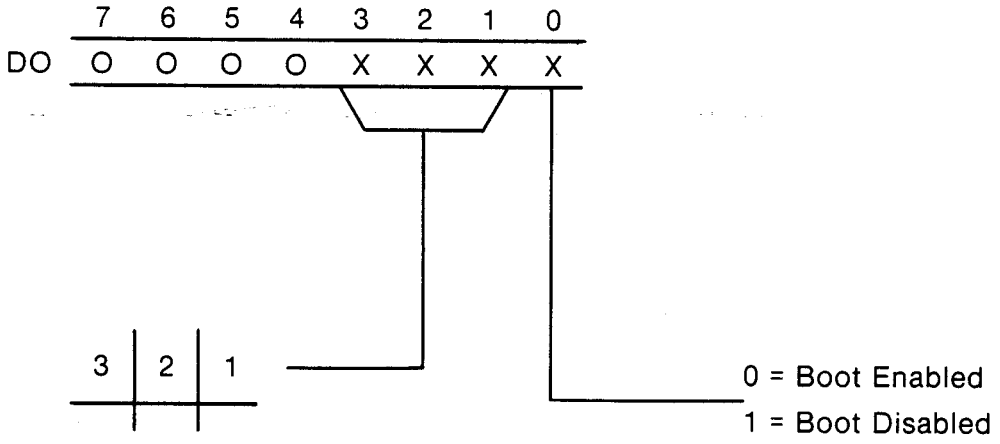
Address: COH — CFH
Function: Interrupt Register



C1 — CF should not be used

Address: DOH
Function: Select or de-select Boot ROM overlay.
Select one of five RAM banks or pages.

The system memory is divided into three pages. Page 0 consists of a full 64K byte RAM. The upper 16K of page 1 is identical to the upper 16K of page 2 in both size and location. Page 1 has a unique 48K bytes of RAM located from 0000H for a total of 64K bytes. Page 2 has a unique 16K bytes of RAM located from location 0000H for a total of 32K bytes of RAM.



0	0	0	=	RAM page 0
0	0	1	=	RAM page 1
0	1	0	=	RAM page 2
0	1	1	=	RAM page 3 (reserved for expansion)
1	0	0	=	RAM page 4 (reserved for expansion)

Address: EOH — EFH

Function: Winchester/SASI Interface

7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	X	DATA/DATA

7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	X	STATUS/CONTROL

3. SPARE PARTS AND TOOLS

3.1 SPARE PARTS

Each Visual 1050 is composed of five major subassemblies designed to be serviced on site by replacement of the appropriate subassembly.

3.1.1 TV Monitor Subassembly

The Tatung model MN1213P31AU monitor is provided in the V1050

Description	Tatung PN	Visual PN
Monitor Kit (total)	CPJ310 Z 1U	MN103-010
TV & Flyback	5727120091	MN103-012
Yoke	DBC 4048	MN103-013
CRT	MN1213P31AU	MN103-014

3.1.2 Keyboard Assembly

The Visual 1050 keyboard is manufactured by the Keytronic corp. and the standard configuration is US version. The Keytronic part number for the keyboard is 65-02335 and the Visual part number is KB01-012.

3.1.3 Main PCB

The main logic board contains all of the active components for the memory and the video presentation to the screen. The part number for the main PCB is PA030-A01.

3.1.4 Power Supply

The power supply for the Visual 1050 is a 75W switching power supply. The part number is PA029-001.

3.1.5 Disk Drive

The floppy disk drive for the Visual is manufactured by Teac Corporation which is 5 1/4 inch 96 TPI drive. The part number for the disc drive is DD001-001.

3.2 SPARE SUBASSEMBLY RECOMMENDATIONS

To service 100 Visual 1050's by subassembly exchange, the following subassemblies should be stocked in the quantities shown:

Part Number	Description	Recommended Spare/100
PA030-A01	V1050 PCB	5
KB010-012	Keyboard	3
PA029-001	Power Supply	3
MN103-012	TV PCB	3
DD001-001	Floppy Disc Drives	6

3.2.1 Active Components Recommendations

The following list contains the active components on the main PCB. The recommendations are based on one depot repairing subassemblies for approximately 100 units. Components which are unique so that they are not found on distribution shelves are indicated with an *

Part Number	Description	Qty/Un	Recommended Spare/100
BT000-034	BATTERY 3.4V	1	5
CC013-015	15 POS 90 deg PC MNT	1	2
CC013-025	25 POS 90 deg PC MNT	1	2
CP100-101	CAP 100 PF	4	2
CP100-220	CAP 22 PF	3	5
CP100-680	CAP 68 PF	2	5
CP220-226	CAP 22uf 16v AXIAL	4	5
CP232-476	CAP 47 UF ELECTRO AXIL	9	5
CP240-103	CAP .01uf Ceramic	153	5
CP240-391	CAP 390 pf Ceramic	6	5
CR001-008	8 PIN HEADER	1	2
CR002-034	HEADER 34 PIN DBL	1	2
CR004-006	6 PIN HEADER SNGL ROW	2	2
CR004-040	40 PIN HEADER SNGL ROW	2	2
CR005-036	36 POS PC MNT 90 deg	1	2
CR005-050	50 POS PC MNT 90 deg	1	2
DA000-001	DIODE 1N914	6	5
DA230-051	DIODE IN4733A	1	5
FB001-001	FERRITE BEAD	5	2

Part Number	Description	Qty/Un	Recommended Spare/100
IC000-001	74LS00	7	10
IC000-002	74LS02	1	10
IC000-004	74LS04	5	15
IC000-008	74LS08	2	15
IC000-010	74LS10	1	10
IC000-014	74LS14	2	15
IC000-020	74LS20	1	10
IC000-032	74LS32	7	15
IC000-074	74LS74	7	15
IC000-075	74LS75	1	10
IC000-086	74LS86	1	10
IC000-138	74LS138	3	20
IC000-139	74LS139	1	10
IC000-163	74LS163	2	15
IC000-164	74LS164	1	10
IC000-166	74LS166	2	15
IC000-174	74LS174	1	10
IC000-175	74LS175	2	15
IC000-195	74LS195	1	10
IC000-244	74LS244	3	20
IC000-245	74LS245	1	10
IC000-253	74LS253	5	20
IC000-257	74LS257	6	20
IC000-273	74LS273	1	10
IC000-367	74LS367	1	10
IC000-393	74LS393	2	15
IC000-399	74LS399	1	10
IC010-006	7406	3	20
IC010-007	7407	2	15
IC010-026	7426	1	10
IC020-004	74S04	4	25
IC140-008	16K DYNAMIC RAM	20	20
IC140-014	64Kx1 DYN RAM	20	20
IC340-001	1488	1	10
IC340-002	1489	1	10

Part Number	Description	Qty/Un	Recommended Spare/100
IC340-015	DATA SEPARATOR 9216B	1	20
IC440-002	8255	2	15
IC440-005	8251	1	10
IC440-006	8214 INT CONT	1	10
IC440-023	REAL TIME CLOCK 5832	1	10
RB000-000	JUMPER	3	2
RB000-102	1K OHM 1/4 W RES	1	5
RB000-103	10K OHM 1/4 W RES	19	5
RB000-121	120 OHM 1/4 W RES	1	5
RB000-122	1.2K OHM 1/4 W RES	1	5
RB000-151	150 OHM 1/4 W RES	1	5
RB000-181	180 OHM 1/4 W RES	1	5
RB000-201	200 OHM 1/4 W RES	1	5
RB000-220	22 OHM 1/4 W RES	4	5
RB000-271	270 OHM 1/4 W RES	1	5
RB000-330	33 OHM 1/4 W RES	12	5
RB000-431	430 OHM 1/4 W RES	2	5
RB000-471	470 OHM 1/4 W RES	11	5
RB000-821	820 OHM 1/4 W RES	1	5
SC000-028	28 PIN SOCKET	2	5
TB009-001	GND TAB	2	5
TR000-001	PN3644	1	5
XT020-005	15.36 MHZ CRYSTAL	1	5
XU001-001	32.768 MHZ CRYSTAL	1	5
RB000-221	220 OHM 1/4 W RES	12	5
RB000-331	330 OHM 1/4 W RES	5	5
RB000-472	4.7K OHM 1/4 W RES	27	5
SC000-040	40 PIN SOCKET	4	5
CP000-101	CAP 100 PF	2	5
IC244-032	FIRMWR V1050	1	
IC244-033	FIRMWR V1050	1	
IC440-009	46505 CRT CONTROLLER	1	10
IC440-017	Z-80 CPU 4.0 MHZ	1	5
IC440-021	6502-2 MICROPROCESSOR	1	10
IC440-022	FLOPPY DISC CONTR 1793	1	10

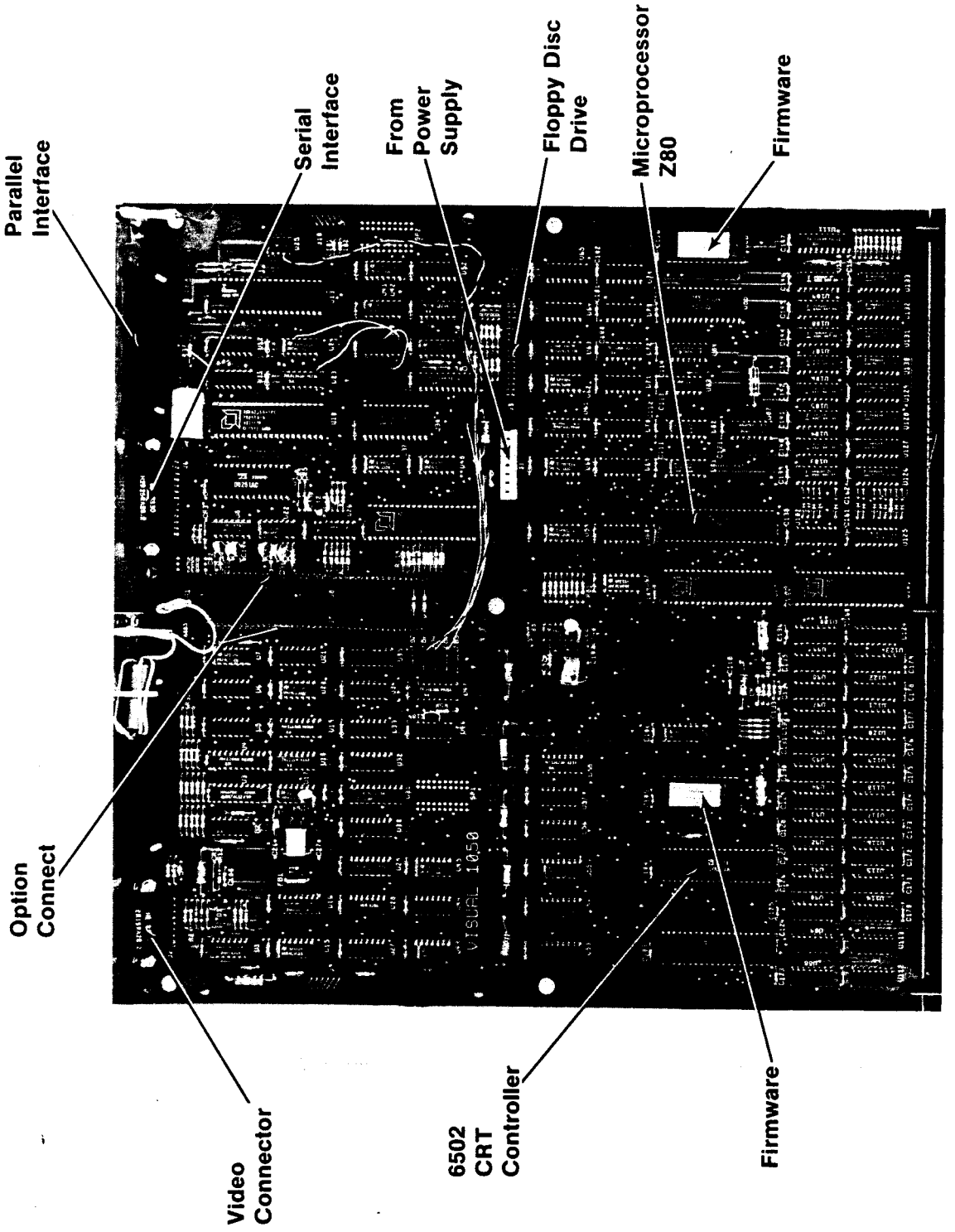


Figure 3-1. Main PCB

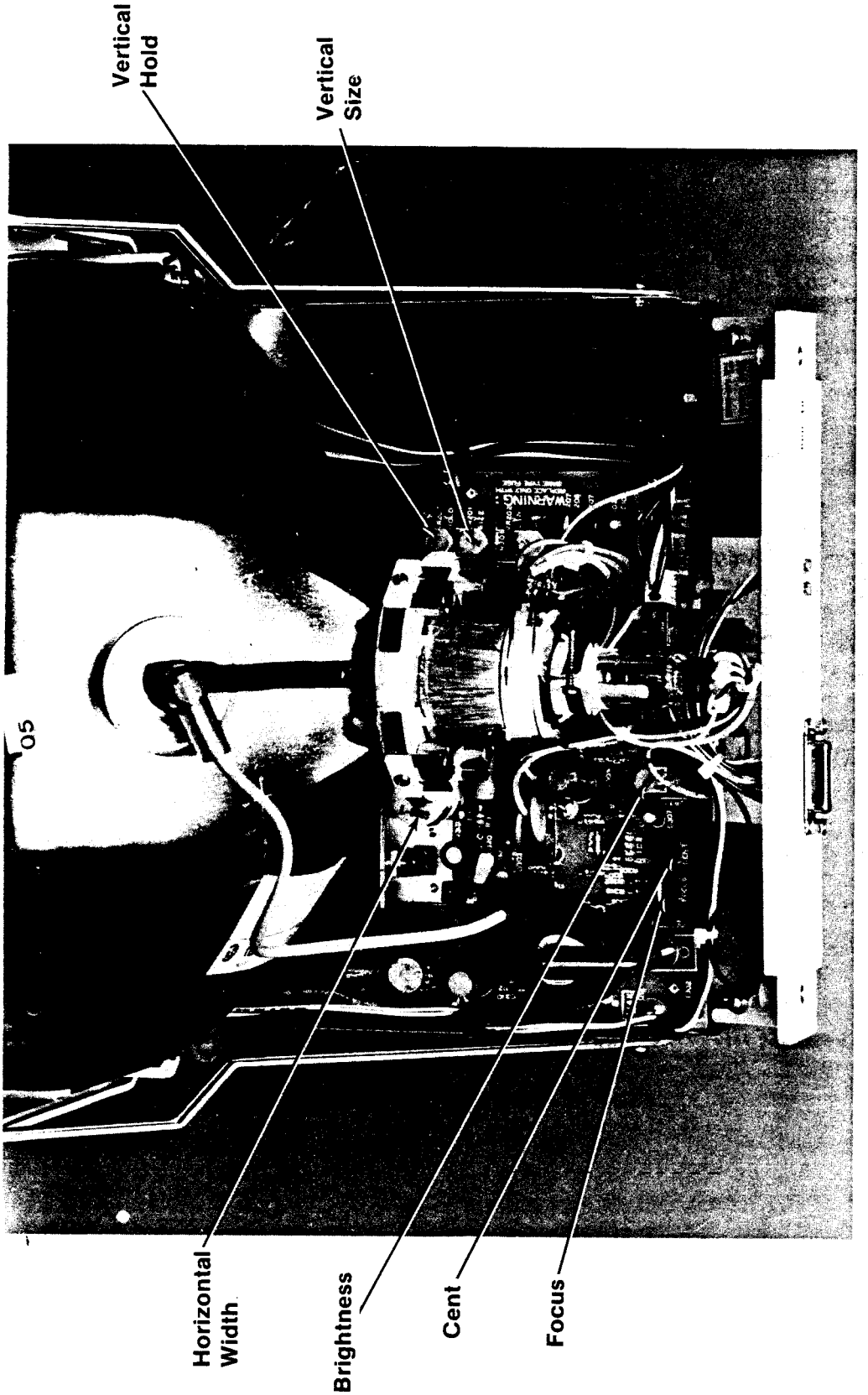


Figure 3-2. Monitor PCB

4. MNEMONIC LIST

Name	Sheet	IC	Definition
1MHz	2	FB2	1 MHz
2MHz	2	FB3	2 MHz
4MHz	2	FB4	4 MHz
4MHzL	2	FB5	4 MHz
8MHz	2	FB6	8 MHz
6502 CLK	8	U78	Ø.96 MHz
ACK From CRT	7	U79	Acknowledge From CRT
ACK To CRT	7	U79	Acknowledge To CRT
ATTCLK	9	U57	Attribute Clock
ATTEN	10	U32	Attribute Enable
ATTRD	9	U57	Attribute Read
BAUDSELA	5	U10	Baud Select A
BAUDSELB	5	U10	Baud Select B
BDØ	11	U31	Buffered Data 0
BD1	11	U31	Buffered Data 1
BLINKTIME	11	U31	Blink time
BOLDCTRL	11	U31	Bold Control
BOOT	3	U87	Enable ROM
BPROMOE	3	U71	Boot PROM Output Enable
CAS	8	U78	Column Address Strobe
CHARCLK	8	U20	Character Clock (1.92 MHz)
CMAØ-CMA13	9	U75	Character Memory Address
DATA from CRT Ø-7	9	U101	Display Data bits 0 thru 7
DATA to CRT	9	U101	Processor Data bits 0 thru 7
DAØ to DA15	9	U76	6502 Address Bits 0 thru 15
DDØ to DD3	10	U100	6502 Data 0 thru 3
DD4 to DD4	10	U124	6502 Data 4 thru 7
DISPLAYBLANK	11	U31	Display Blank
DISPLAY-RAM-RD	10	U56	Display RAM Read
DOTCLK	8	U17	Dot Clock (15.36 MHz)
DVINT	9	U6	Display Video Interrupt
EMØ	10	U93	Display Even Memory Bit 0
EM1	10	U92	Display Even Memory Bit 1

Mnemonic List

Name	Sheet	IC	Definition
EM2	10	U91	Even Memory Bit 2
EM3	10	U90	Even Memory Bit 3
EM4	10	U99	Even Memory Bit 4
EM5	10	U98	Even Memory Bit 5
EM6	10	U96	Even Memory Bit 6
EM7	10	U94	Even Memory Bit 7
ERAS	8	U78	Even Row Address Strobe
EXTINT	7	J7	External interrupt
EXTWAIT	7	J7	External wait
FDDEN	5	U10	Floppy Double Densisty Enable
FDIRC	6	U13	Floppy Direction
FDSØ-FDS3	5	U10	Floppy Data 0 thru 4
FINTEN	5	U10	Floppy Interrupt
FMOTORON	5	U10	Floppy Motor On
FPRECOMP	5	U10	Floppy Precom Enable
FSEL	2	U82	Floppy Controller Select
FSIDE1	5	U10	Floppy Side 1 Select
FSTEP	6	U13	Floppy Step
FWRTDATA	6	U13	Floppy Write Data
FWRTGATE	6	U13	Floppy Write Gate
HSYNC	9	U2	Horizontal Sync
I/O	2	U80	Z80 I/O Request
KBDSEL	2	U82	Keyboard Select
MAD14	3	U71	Modified Address
MAD15	3	U71	Modified Address
MEMREQ	2	U80	Memory Request
MISCSEL	2	U82	Parallel Interface Select
M1	2	U80	Z80 Machine Cycle One
MUXA	8	U44	Multiplex Address Select A
MUXB	8	U44	Multiplex Address Select B
OMØ	10	U115	Odd Memory Bit 0
OM1	10	U114	Odd Memory Bit 1
OM2	10	U122	Odd Memory Bit 2
OM3	10	U120	Odd Memory Bit 3
OM4	10	U119	Odd Memory Bit 4
OM5	10	U118	Odd Memory Bit 5
OM6	10	U117	Odd Memory Bit 6
OM7	10	U116	Odd Memory Bit 7

Mnemonic List

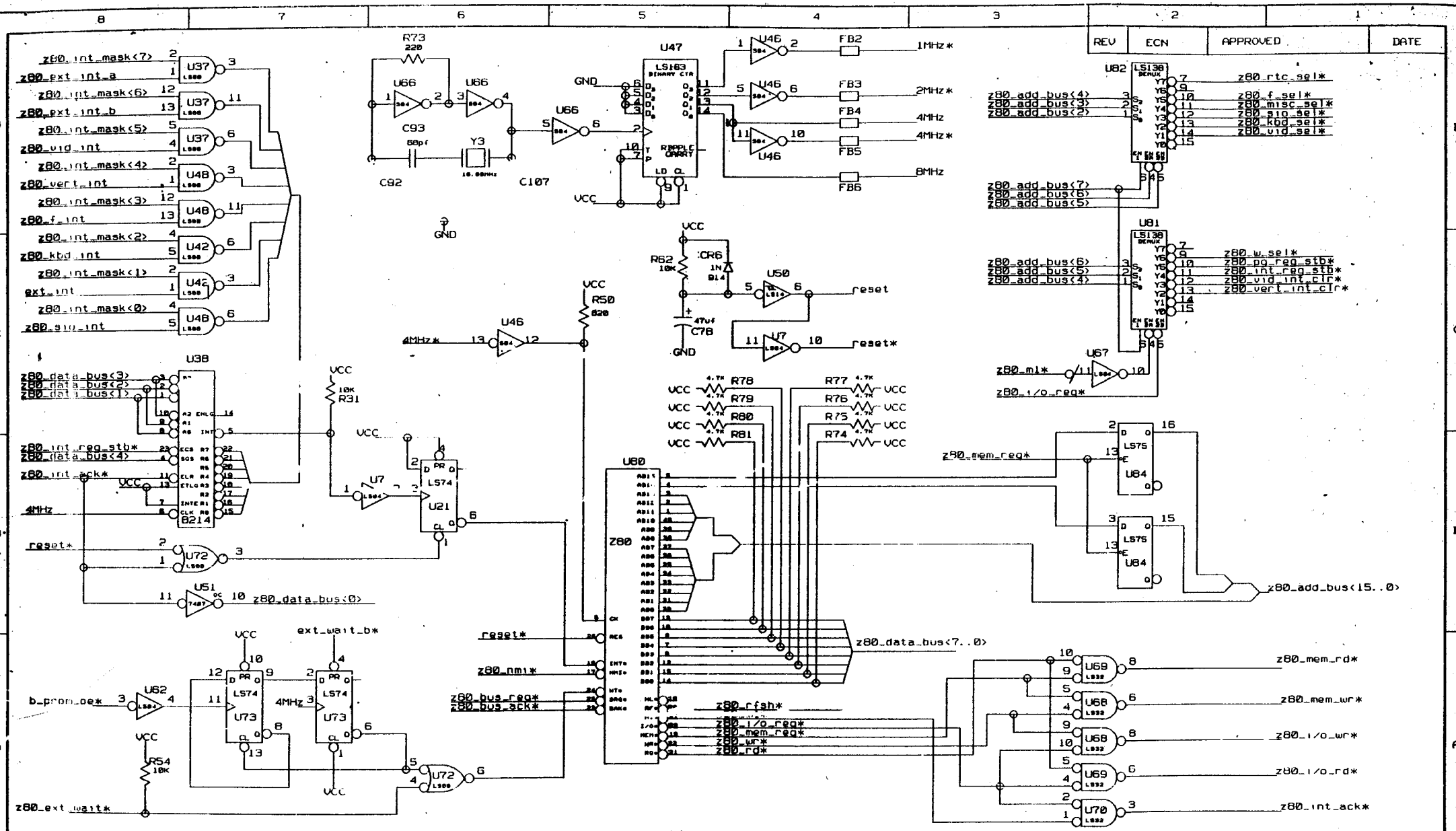
Name	Sheet	IC	Definition
ORAS	8	U78	Odd Row Address Stobe
PAGEREVERSE	11	U31	Page Reverse Video
PRPE	5	J5	Paper Empty
PRSTROBE	5	U10	Printer Strobe
P1RD	9	U57	6502 Read
P1WR	9	U7	6502 Write
RAØ	10	U113	Row Address 0
RA1	10	U112	Row Address 1
RA2	10	U112	Row Address 2
RA3	10	U89	Row Address 3
RA4	10	U89	Row Address 4
RA5	10	U88	Row Address 5
RA6	10	U88	Row Address 6
REATTØ	10	U97	Read Even Attribute Bit 0
REATT1	10	U95	Read Even Attribute Bit 1
RTCSEL	2	U82	Real Time Clock Select
RD	2	U80	Read
RFSH	2	U80	Refresh
RESET	2	U50	Reset
RESETL	2	U7	Reset Low
ROATT0	10	U123	Read Odd Attribute Bit 0
ROATT1	10	U121	Read Odd Attribute Bit 1
SHIFTCLK	8	U20	Video Shift Clock
SIOCLK	5	U65	Serial In and Out Clock
SIOSEL	2	U82	Serial Interface Select
STBFROMCRT	7	U79	Strobe From CRT
STBTOCRT	7	U79	Strobe to CRT
SYSTEMCLK	8	U20	6502 System Clock
VCLK	9	U75	Vertical Clock
VIDENABLE	9	U75	Video Enable
VIDINTCLK	9	U5	Video Interrupt Clock
VIDSEL	2	U82	Video Interface Select
VSYNC	9	U2	Vertical Sync
WINDOW	6	U40	Window for Floppy Disc Precomp
WR	2	U80	Write
WSEL	2	U81	Winchester Select

5. I.C. DATA SHEETS

Included in this section are the specifications for the following I.C.'s

Z80	Z80 CPU
8251	USART
8255A	PIO
6502	Display Driver
1793	Floppy Disc Controller
8214	Interrupt Controller

6. SCHEMATICS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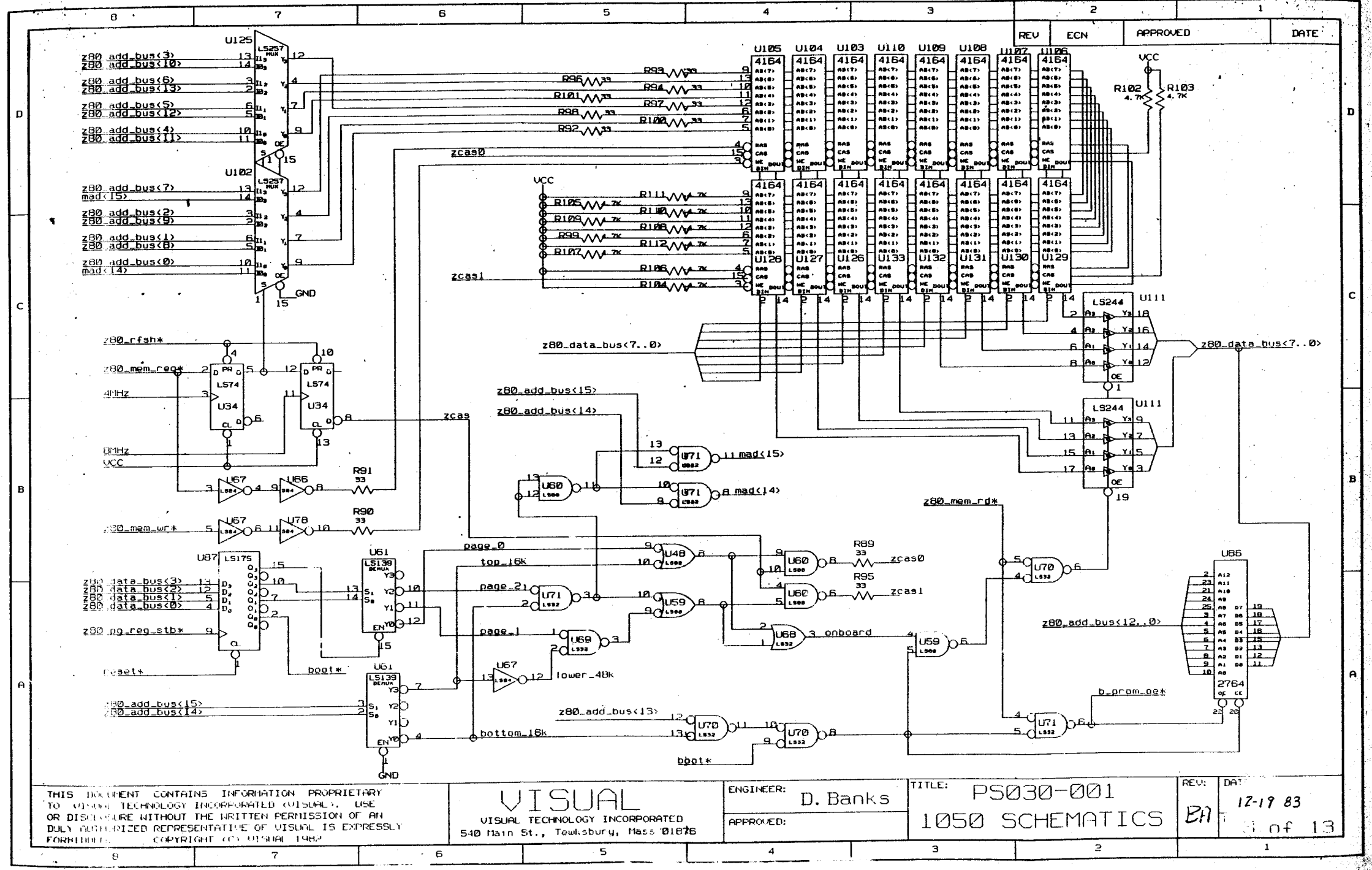
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U105
U104
U103
U110
U109
U108
U107
U106
4164
R96
R99
R94
R101
R97
R98
R100
R92
zcas0
VCC
R102
4.7K
R103
4.7K
R105
R111
R110
R109
R108
R99
R112
R107
R106
R104
U126
U127
U133
U132
U131
U130
U129
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LS244
U111
z80_rfsh*
z80_mem_req*
4MHz
8MHz
LS74
U34
zcas
R91
33
U67
U66
z80_mem_wr*
U78
R90
z80_add_bus<15>
z80_add_bus<14>
U71
mad<15>
U60
mad<14>
z80_mem_rd*
U87
LS175
z80_data_bus<3>
z80_data_bus<2>
z80_data_bus<1>
z80_data_bus<0>
z80_pg_reg_stb*
reset*
boot*
U61
LS138
page_0
top_16k
page_2
page_1
lower_48k
bottom_16k
U48
U59
U68
onboard
R89
zcas0
R95
zcas1
U70
U69
bboot*
U86
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z80_add_bus<12..0>
b_prom_oe*
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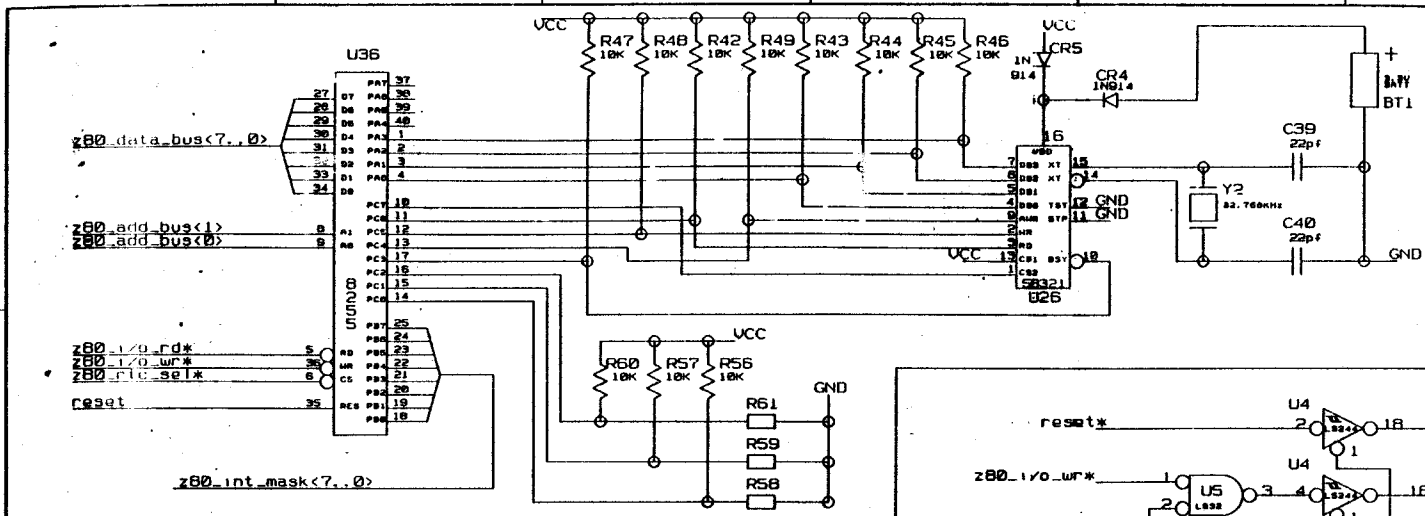
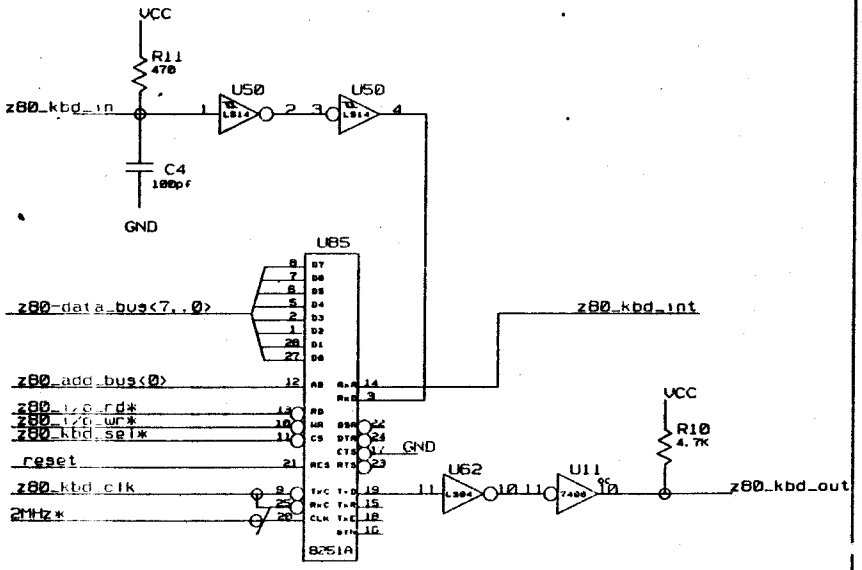


REAL TIME CLOCK & INTERRUPT MASK



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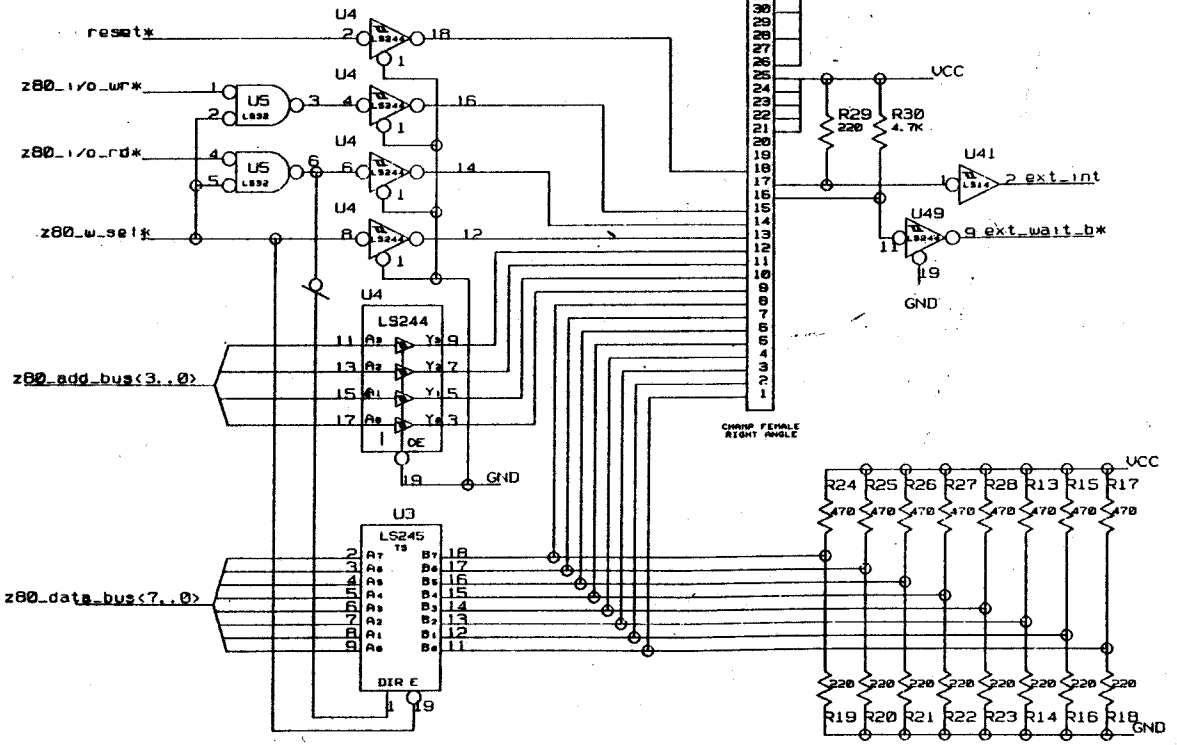

WINCHESTER INTERFACE

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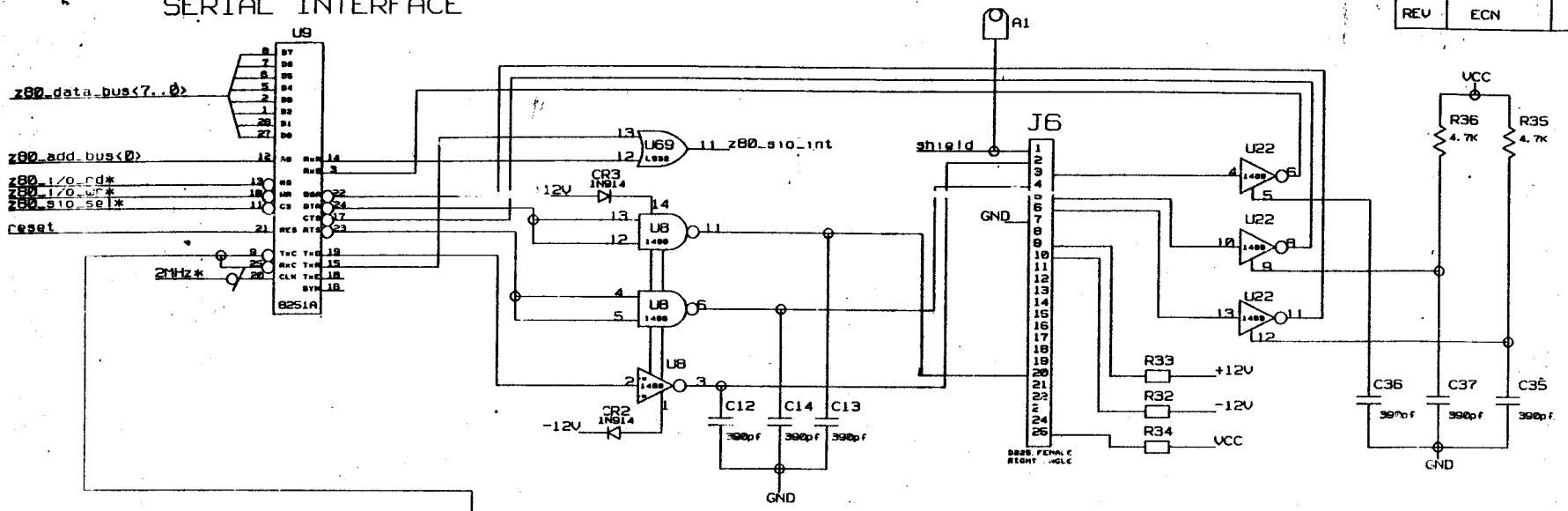

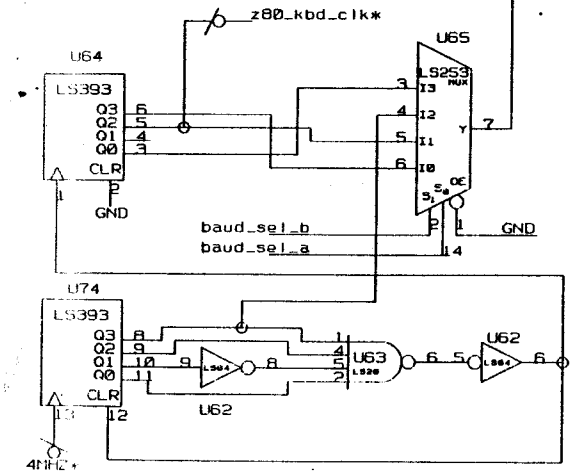

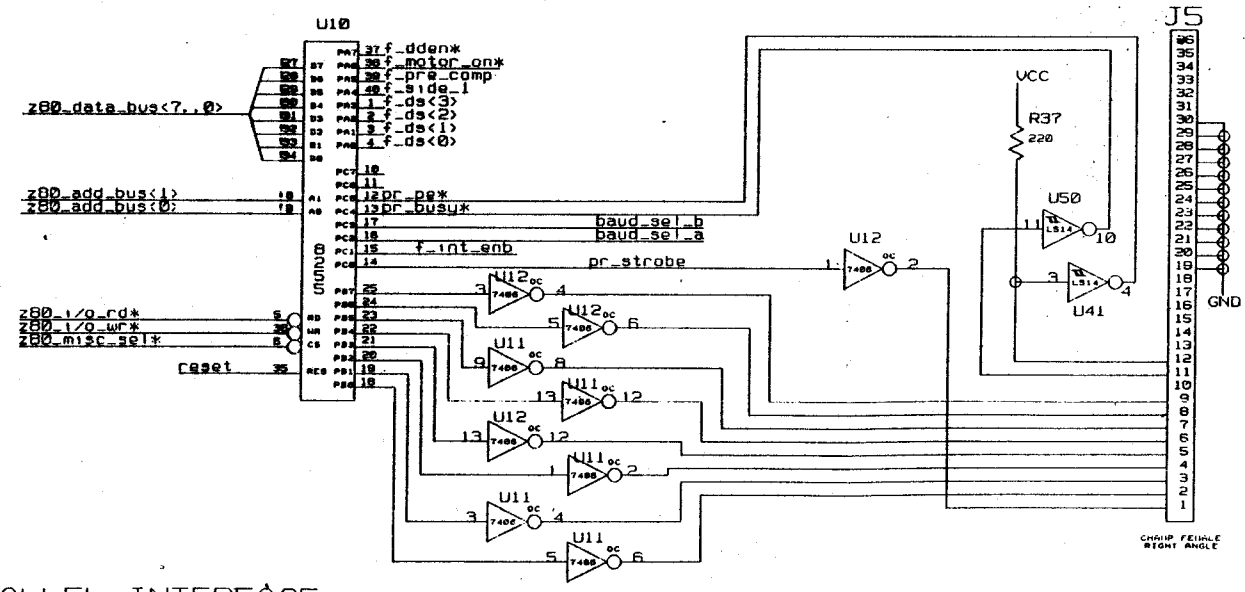

PARALLEL INTERFACE

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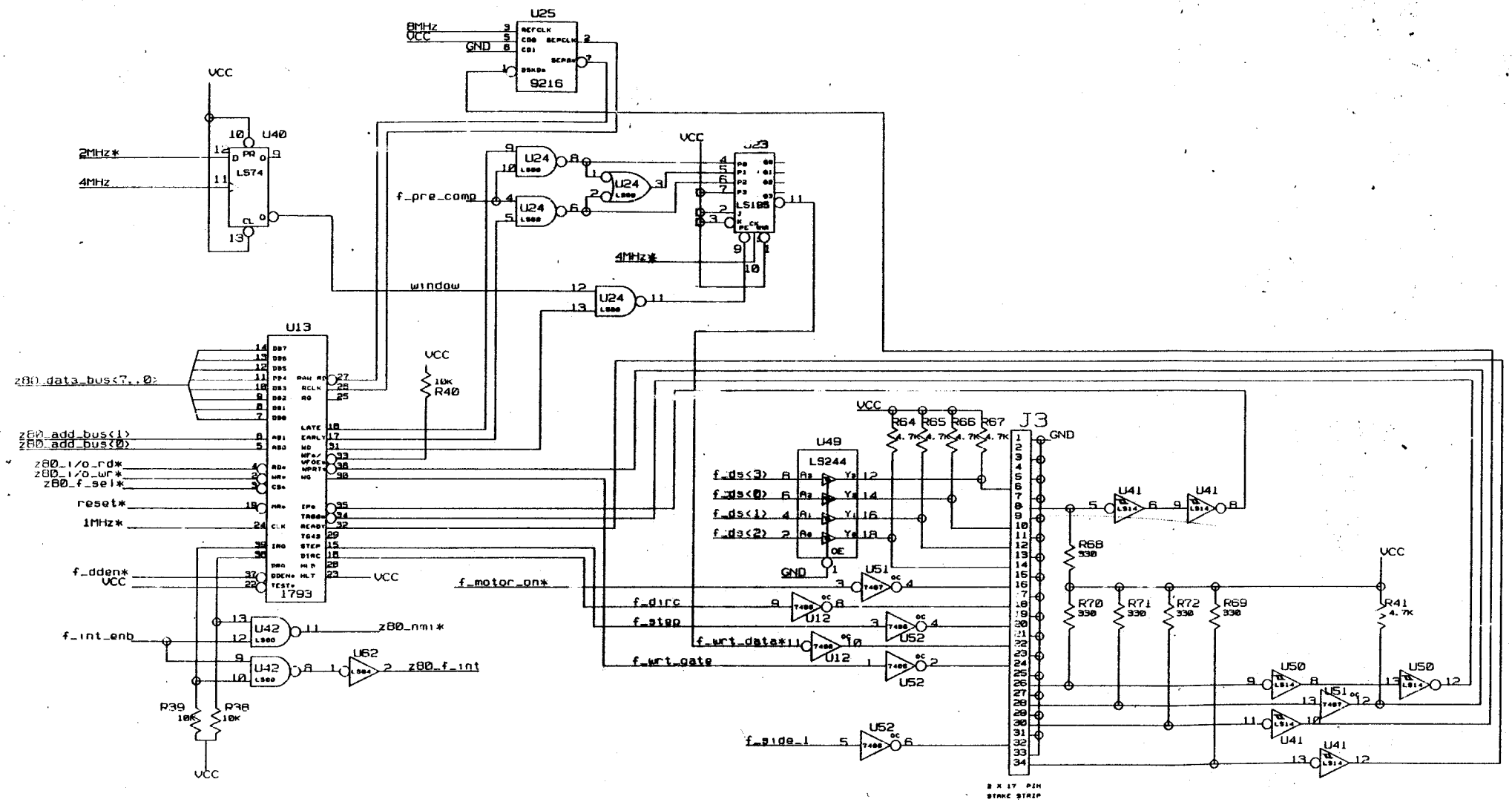

FLOPPY DISC INTERFACE

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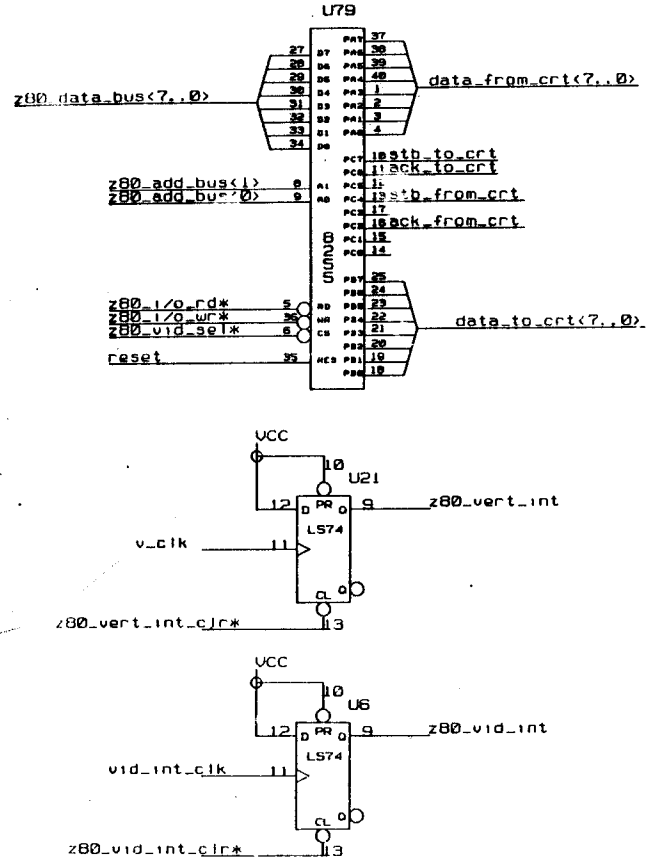
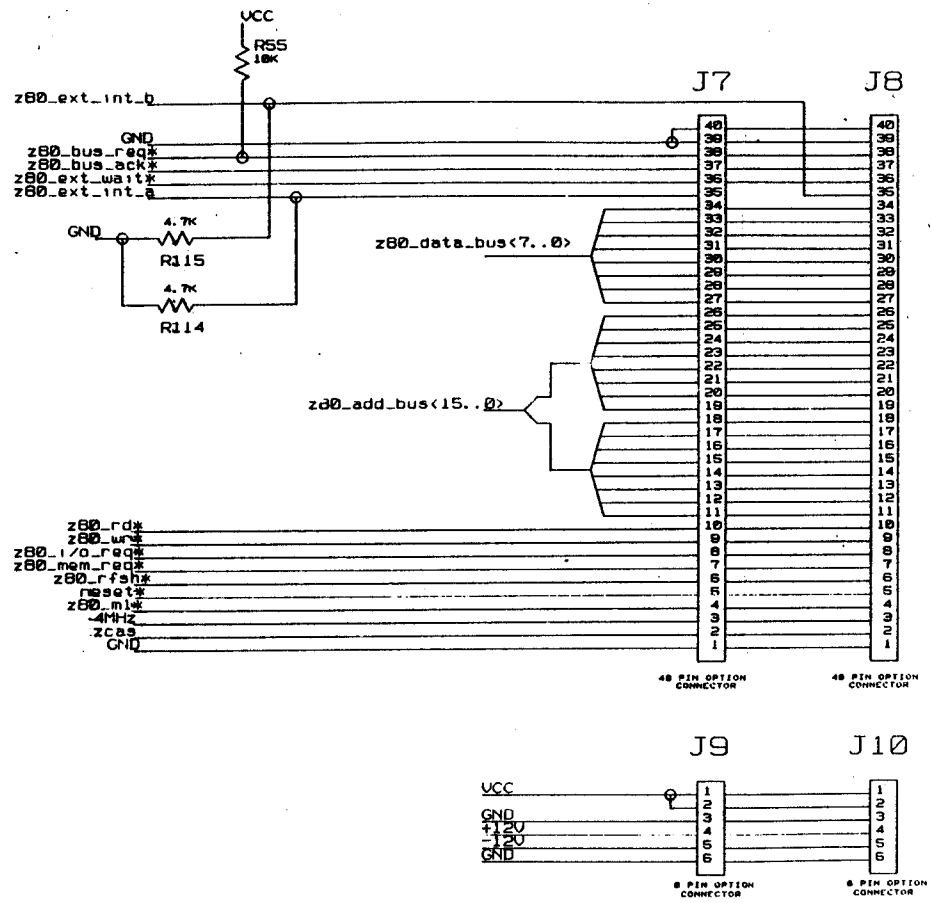


INTERFACE TO CRT



OPTION CONNECTORS

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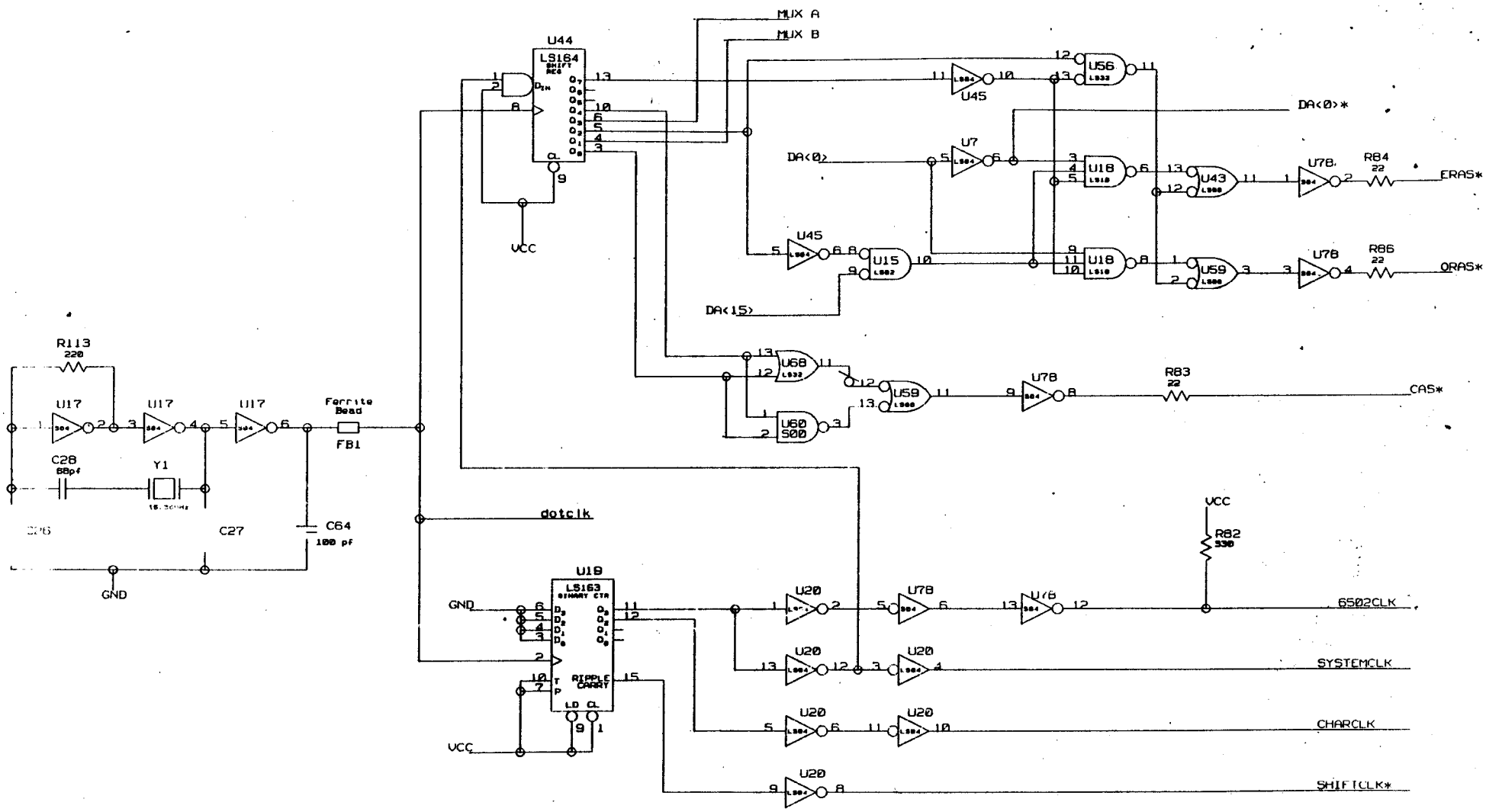

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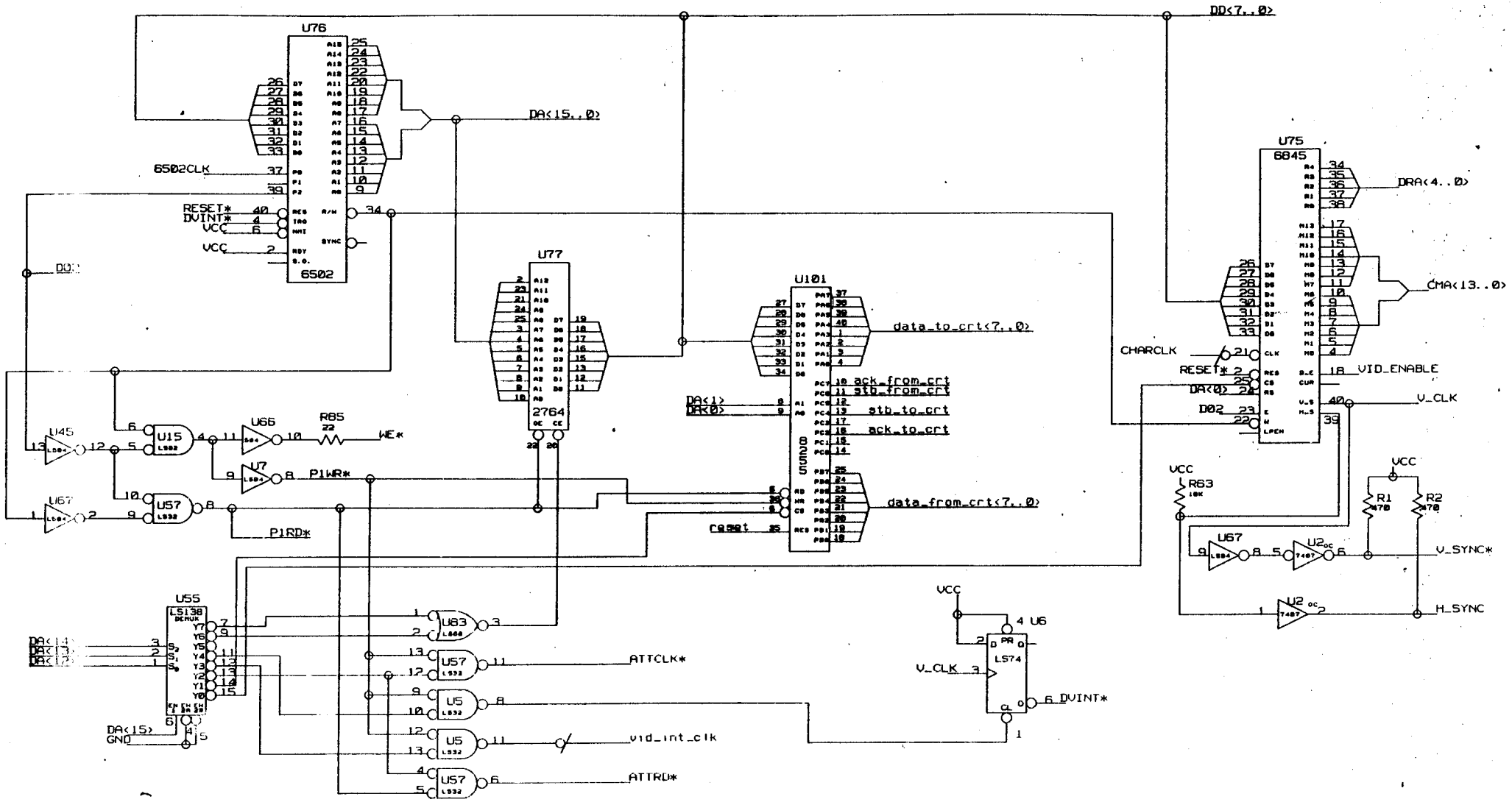

6502 AND DISPLAY CONTROLLER

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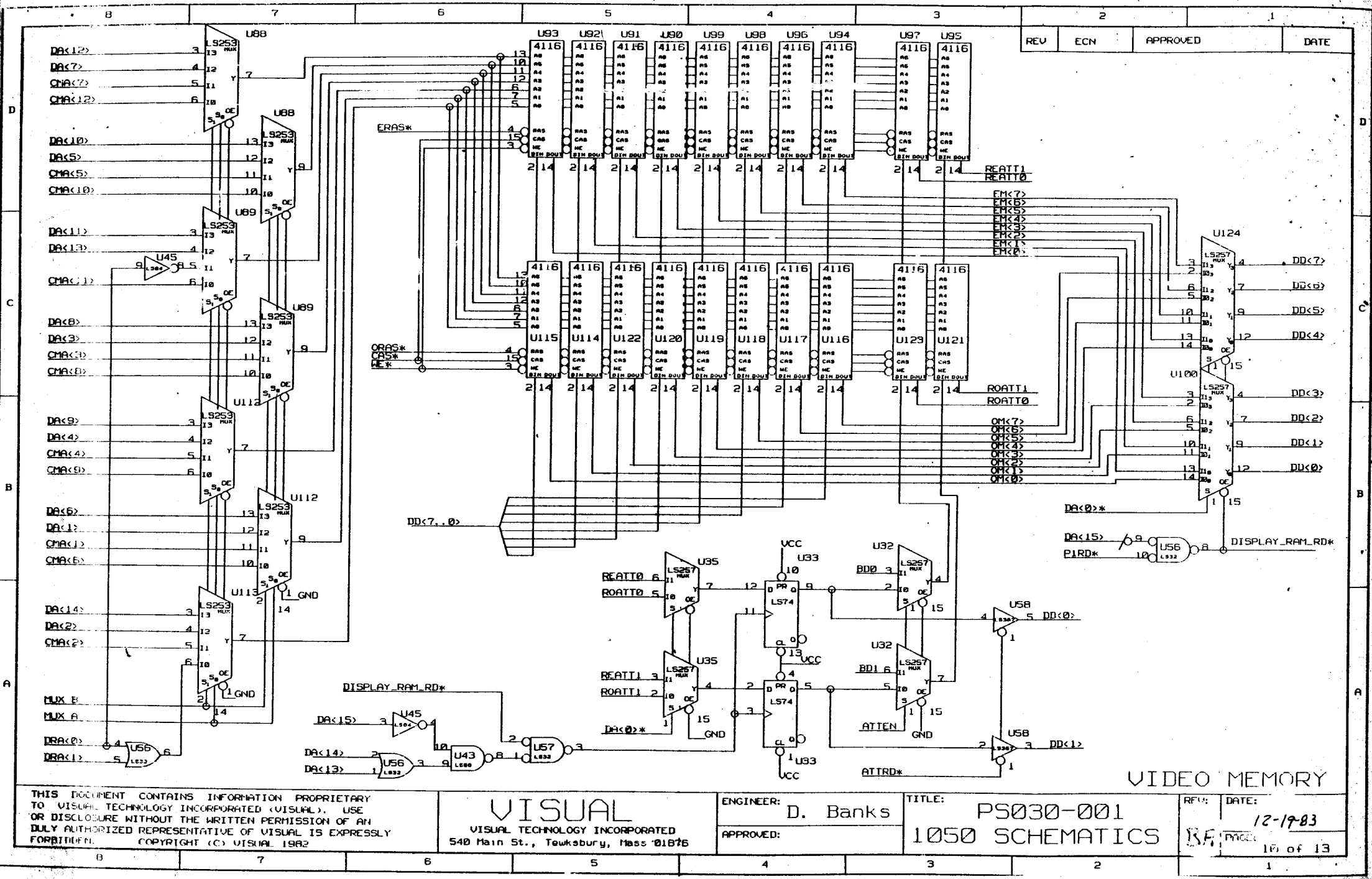
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MUX A
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GND
VIDEO MEMORY
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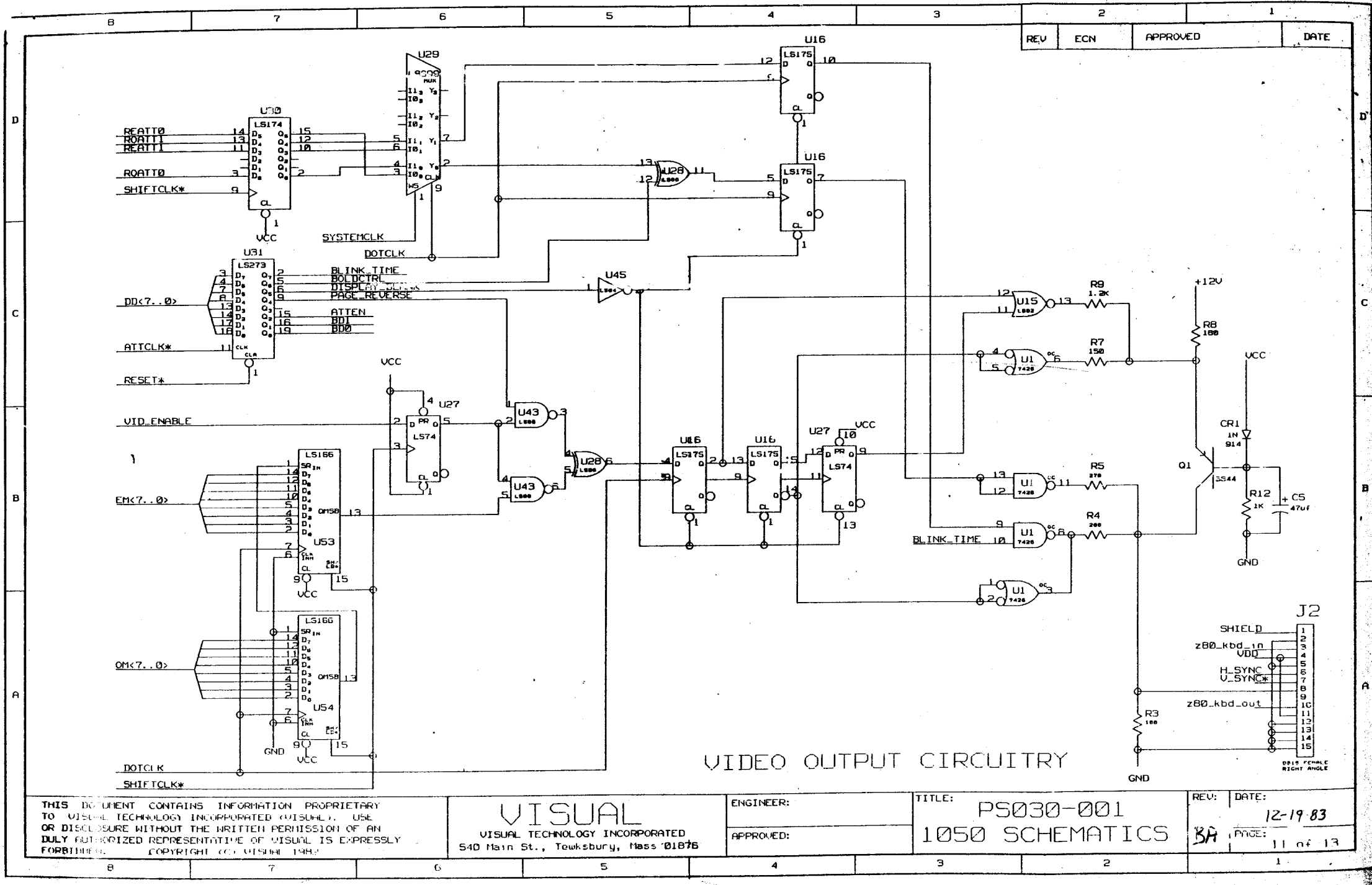
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REATT1
RQATT0
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VCC
SYSTEMCLK
DOTCLK
U31
LS273
DD<7..0>
ATTCLK*
RESET*
BLINK_TIME
BOLDCTRL
DISPCHARSET
PAGE_REVERSE
ATTEN
BD1
BD0
U16
LS175
U28
U45
U27
LS74
VID_ENABLE
U43
U53
U54
LS166
QM158
EM<7..0>
QM<7..0>
GND
U15
U1
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R9
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R8
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R7
150
R5
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R4
200
R3
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CR1
1N
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Q1
3S44
R12
1K
C5
47uf
BLINK_TIME
J2
SHIELD
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VDD
H_SYNC
V_SYNC*
z80_kbd_out
DB15 FEMALE
RIGHT ANGLE
VIDEO OUTPUT CIRCUITRY
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POWER CONNECTOR AND FILTER CAPS

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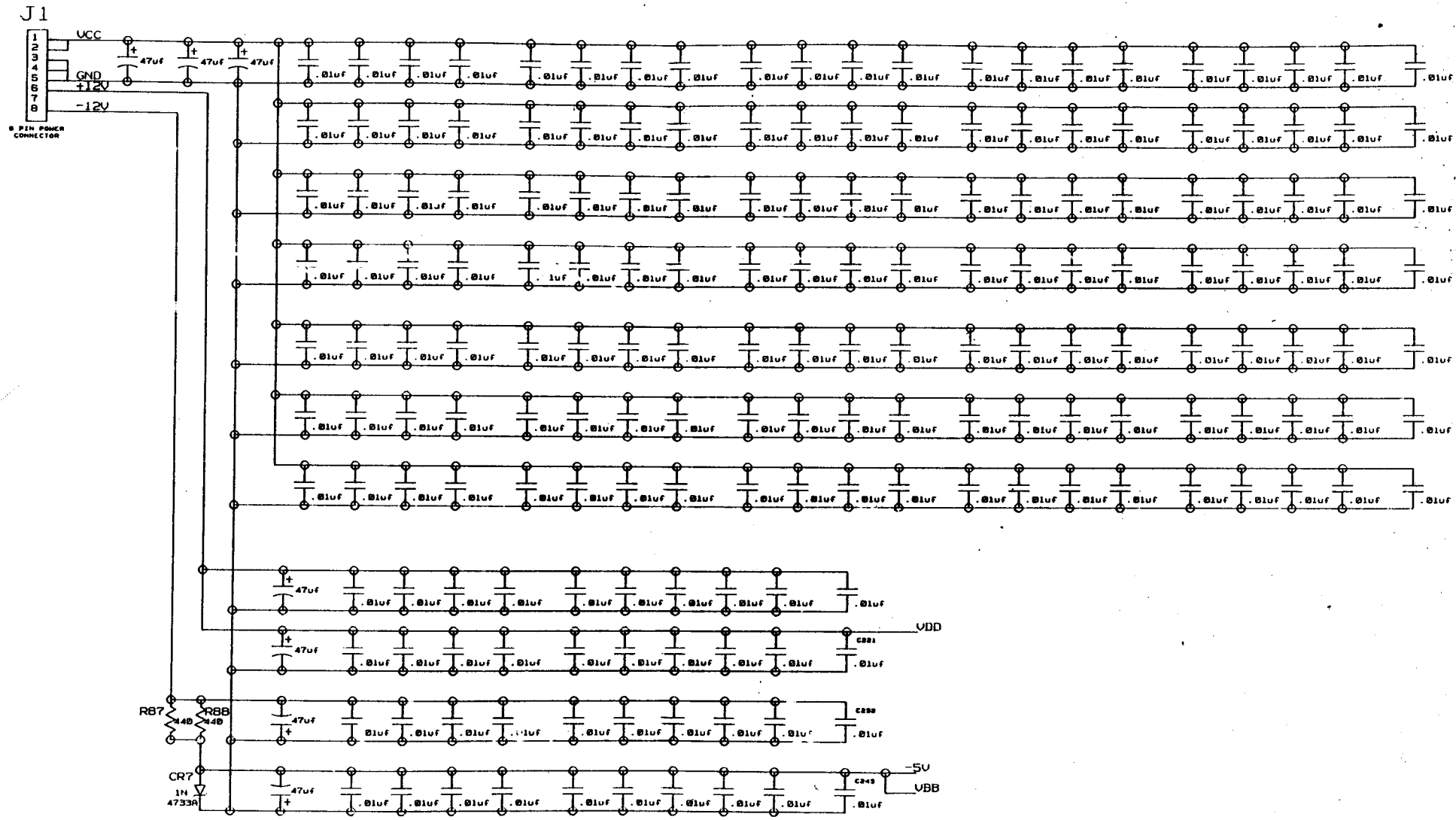

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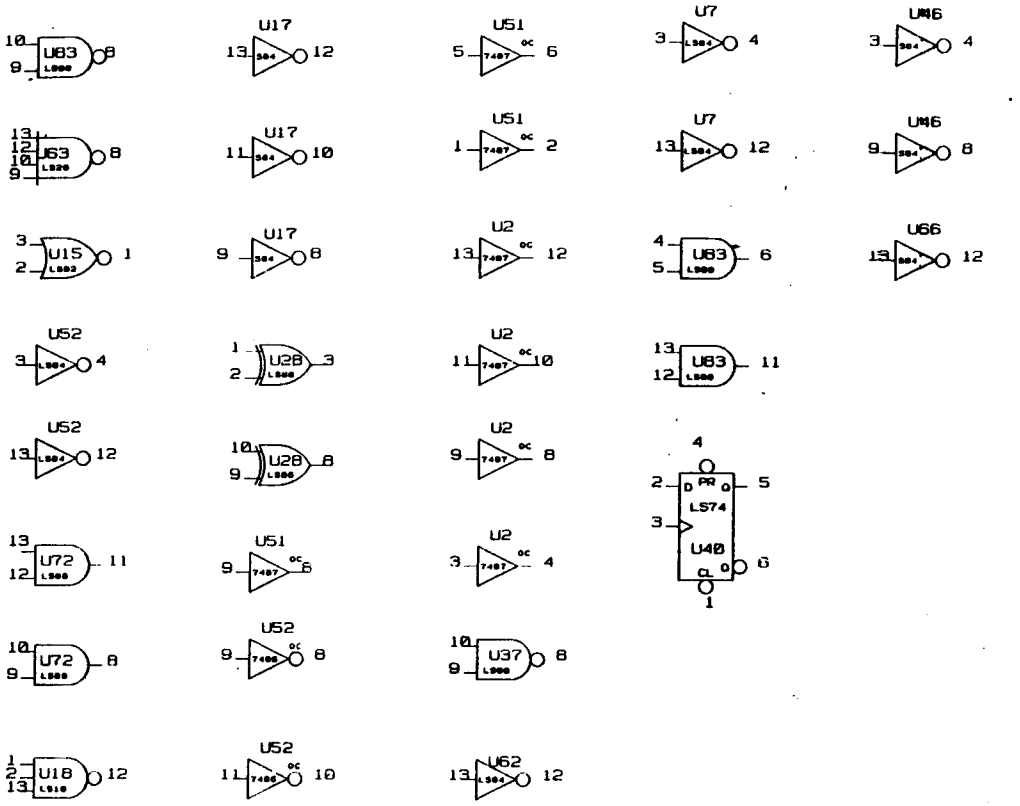

SPARE GATES

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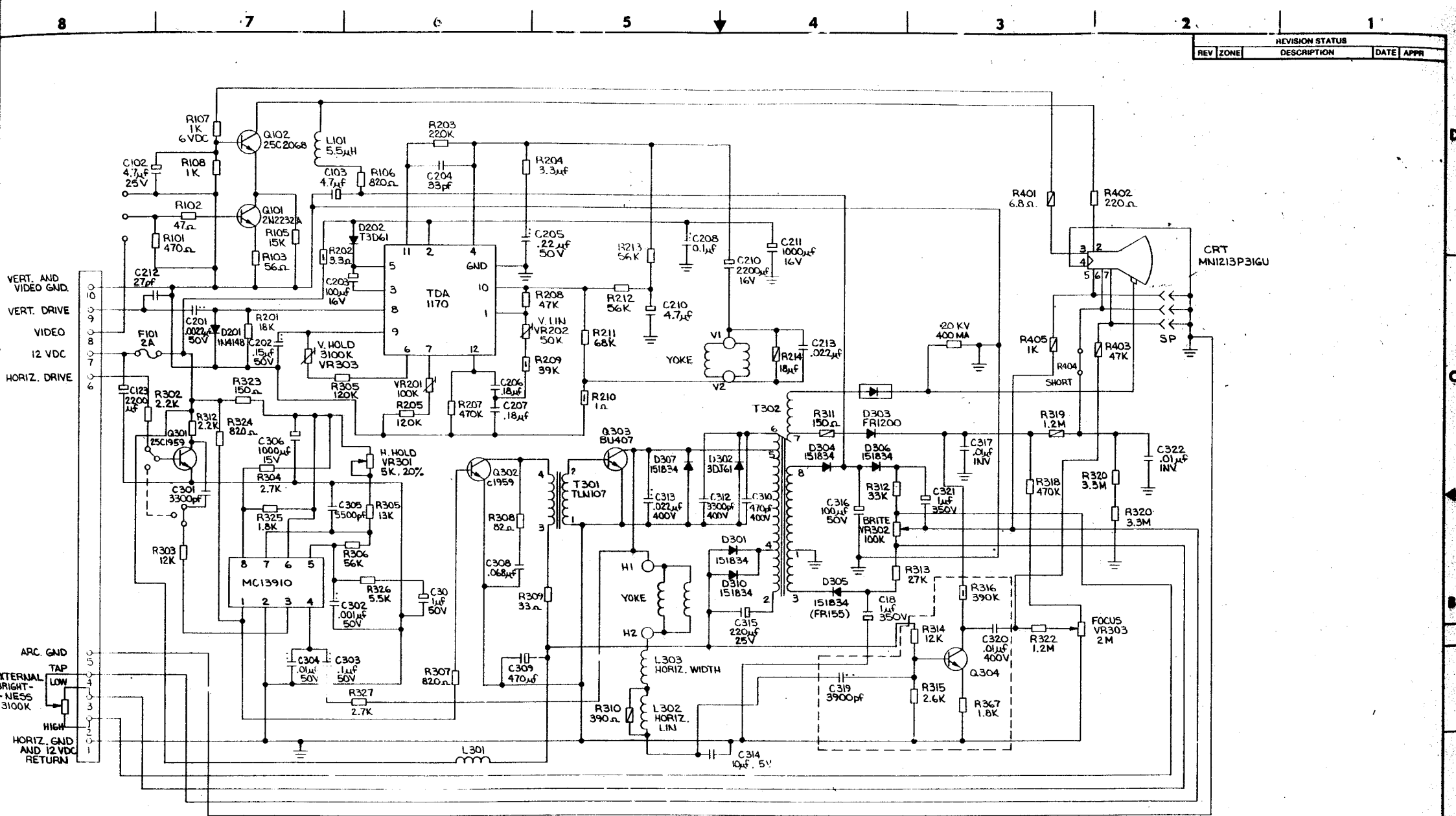
APPROVED:

TITLE: PS030-001
1050 SCHEMATICS

REV: D1
DATE: 12-19-83
PAGE: 13 of 13



SYMBOL DESCRIPTION

- 1/4 W CARBON FILM RES.
- 1/2 W CARBON FILM RES. OR CARBON COMP. RES.
- 1 W METAL FILM RES. OR CARBON FILM RES.
- 2 W METAL OXIDE FILM RES.
- 3 W METAL OXIDE FILM RES.
- CERAMIC CAP.
- POLYESTER CAP.
- ELECTROLYTIC CAP.
- SPARK GAP
- VARIABLE RES.

REVISION STATUS

REV	ZONE	DESCRIPTION	DATE	APPR

THIRD ANGLE PROJECTION
INCH
MILLIMETER

TOLERANCES: Except as noted
± INCHES/MM
.X = /
.XX = /
.XXX = /
FRACT. =
ANGLE =

DRAWN J. GLOUDEMAN 3/22/84
CHECKED
ENG
Q.A.
OPER

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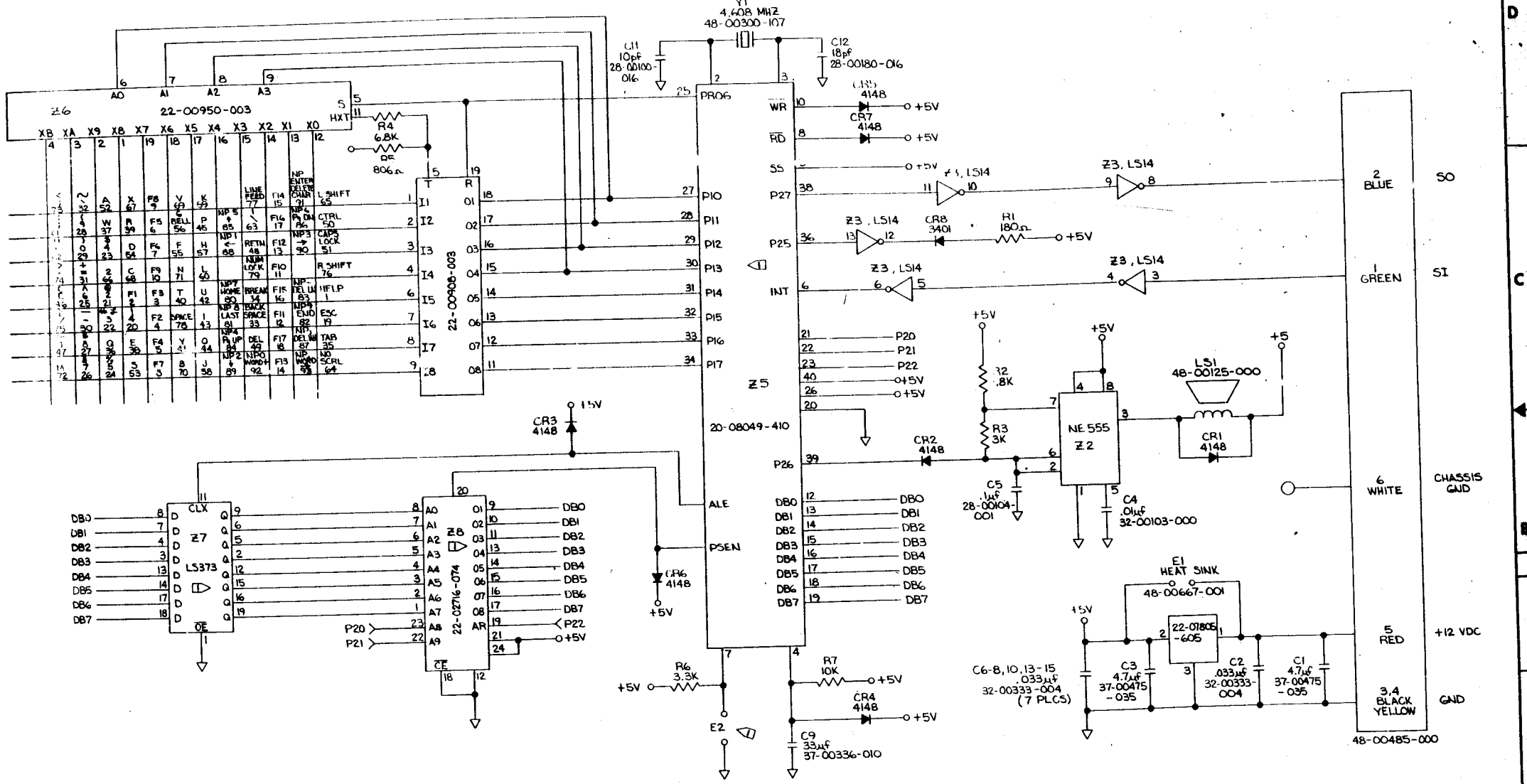
SIZE D | REV.

TITLE: TATUNG MONITOR SCHEMATIC

UNIT NO. MN103-010

Model No. | Next Assy. | SCALE | SHEET



NOTES:

1. ◁ ON PCB ASSY INSTALL 20-08039-000 AT Z5 AND INSTALL Z7 AND Z8. DELETE ETCH TIE AT E2.

REVISION STATUS

REV	ZONE	DESCRIPTION	DATE	APPR

THIRD ANGLE PROJECTION

INCH / MILLIMETER

TOLERANCES: Except as noted ± INCHES/MM .X = / .XX = / .XXX = / FRACT. = ANGLE =

DRAWN J. O'LOUGHLIN 3-23-84

CHECKED

ENG

Q.A.

OPER

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SIZE D REV.

TITLE: KEYBOARD SCHEMATIC V1050

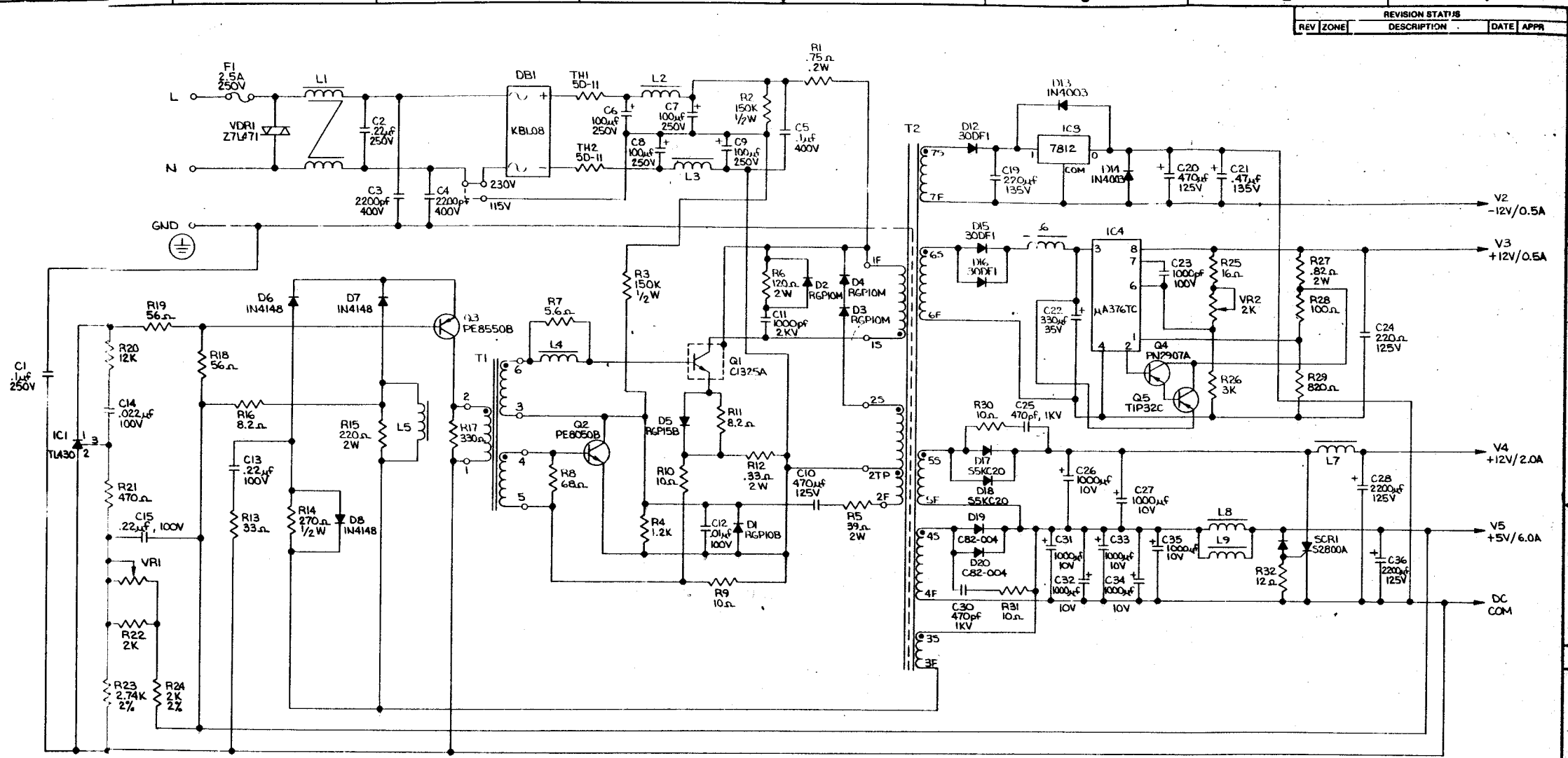
UNIT NO. KS006-001

Model No. V1050

Next Assy.

SCALE

SHEET



NOTES:

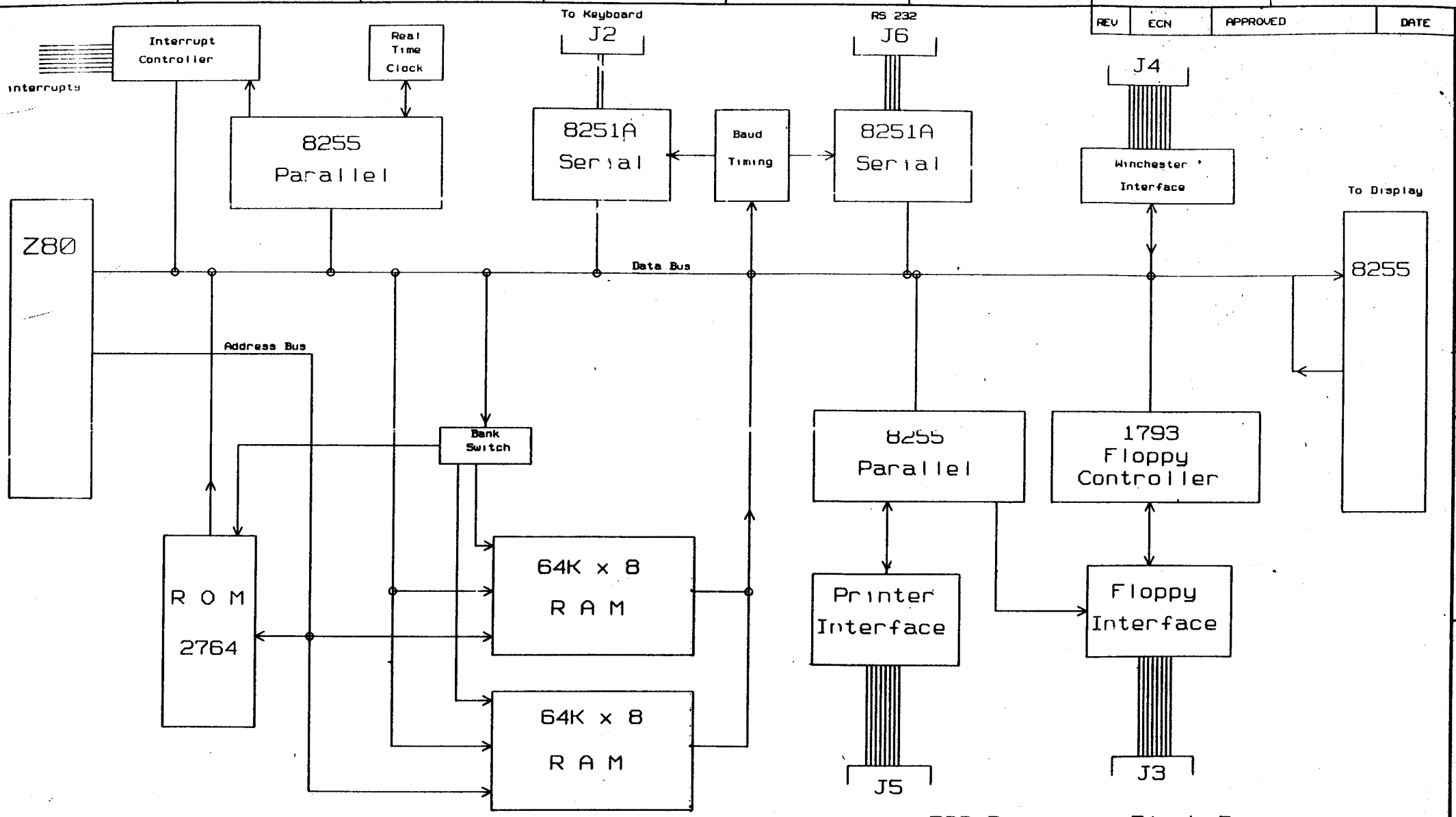
1. ALL RESISTORS 1/4W, UNLESS OTHERWISE NOTED.

REVISION STATUS

REV	ZONE	DESCRIPTION	DATE	APPR

THIRD ANGLE PROJECTION	TOLERANCES: Except as noted	DRAWN J.O'LOUGHLIN 3/22/85	VISUAL Visual Technology Incorporated 540 Main Street, Tewksbury, MA. 01876
INCH / MILLIMETER	± INCHES/MM .X = / .XX = / .XXX = / FRACT. = ANGLE =	CHECKED	SIZE D REV.
This document contains information proprietary to VISUAL and is not to be used or reproduced without express written permission of a duly authorized representative of VISUAL TECHNOLOGY INCORPORATED.		ENG	TITLE: 75W POWER SUPPLY
		Q.A.	UNIT NO. PS029-001
		OPER	Model No. Next Assy. SCALE SHEET

VISUAL FORM VF001-004



Z80 Processor Block Diagram

REV	ECN	APPROVED	DATE

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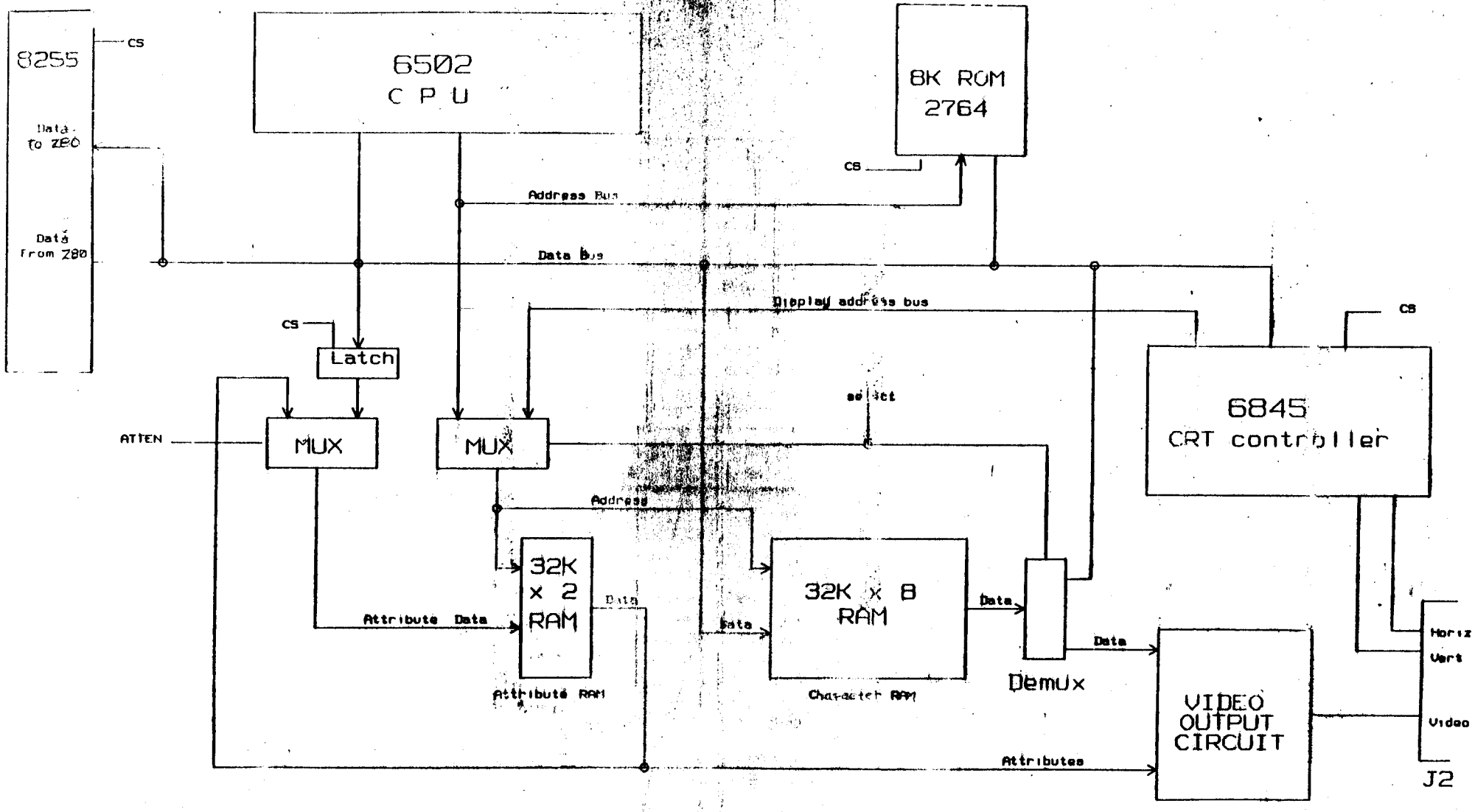
ENGINEER: D. Banks	TITLE: V1050 Block Diagram	REV: 1A	DATE: 10/8/83
APPROVED:			PAGE: 2 of

REV	ECN	APPROVED	DATE



Display Block Diagram

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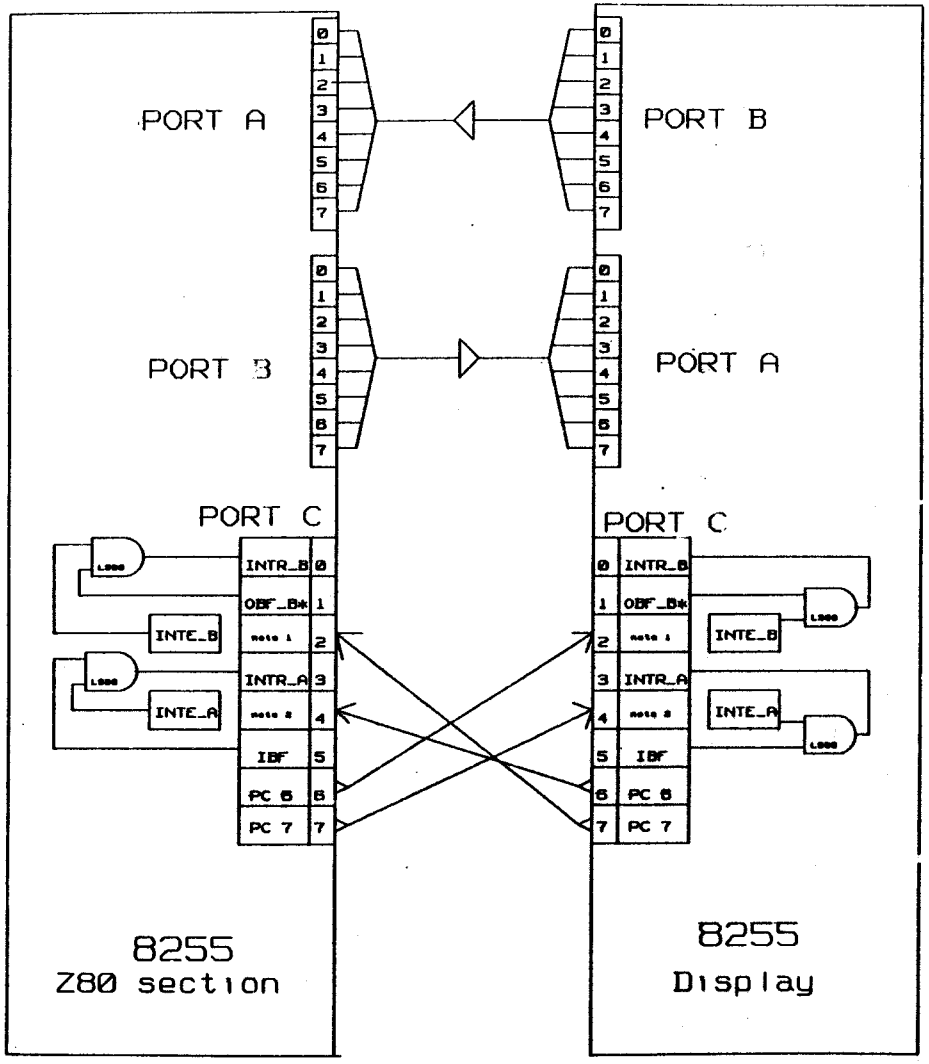
ENGINEER:	TITLE:	REV:	DATE:
D. Banks	V1050 Block Diagram	1A	10/8/83
APPROVED:			PAGE: 3 of



note 1... This pin going low causes OBF_B* to go high

note 2... This pin going low latches data into port A and sets IBF high

REV	ECN	APPROVED	DATE

6502 Initialization steps

Initialize 8255 with mode byte B4H
Set port C bit 2 high
Set port C bit 4 high
Set port C bit 6 high
Set port C bit 7 high

Z80 Initialization steps

Initialize 8255 with mode byte B4H
Set port C bit 7 high
Set port C bit 6 high
Set port C bit 4 high
Set port C bit 2 high

Send Data from Z80 section to Display section

Z80 side of transfer

1. Read port C
2. Check bit 0 (INTR_B)
3. If equal to 0 then go back to step 2, if 1 continue
   Output character data to port B which sets Z80 OBF_B* low which in turn sets Z80 INTR_B low
5. Set PC7 low which latches data into 6502 port A and sets 6502 IBF high
8. Set PC7 back to high which sets 6502 INTR-A high

6502 side of transfer

1. Read port C
2. Check bit 3 (INTR_A)
3. If equal to 0 then go back to step 2, if 1 continue
4. Read port A (the character data) which clears 6502 IBF
5. Set PC7 to a 0 which sets Z80 OBF_B* high
6. Set PC7 back to 1

Z80 Processor to Display Interface

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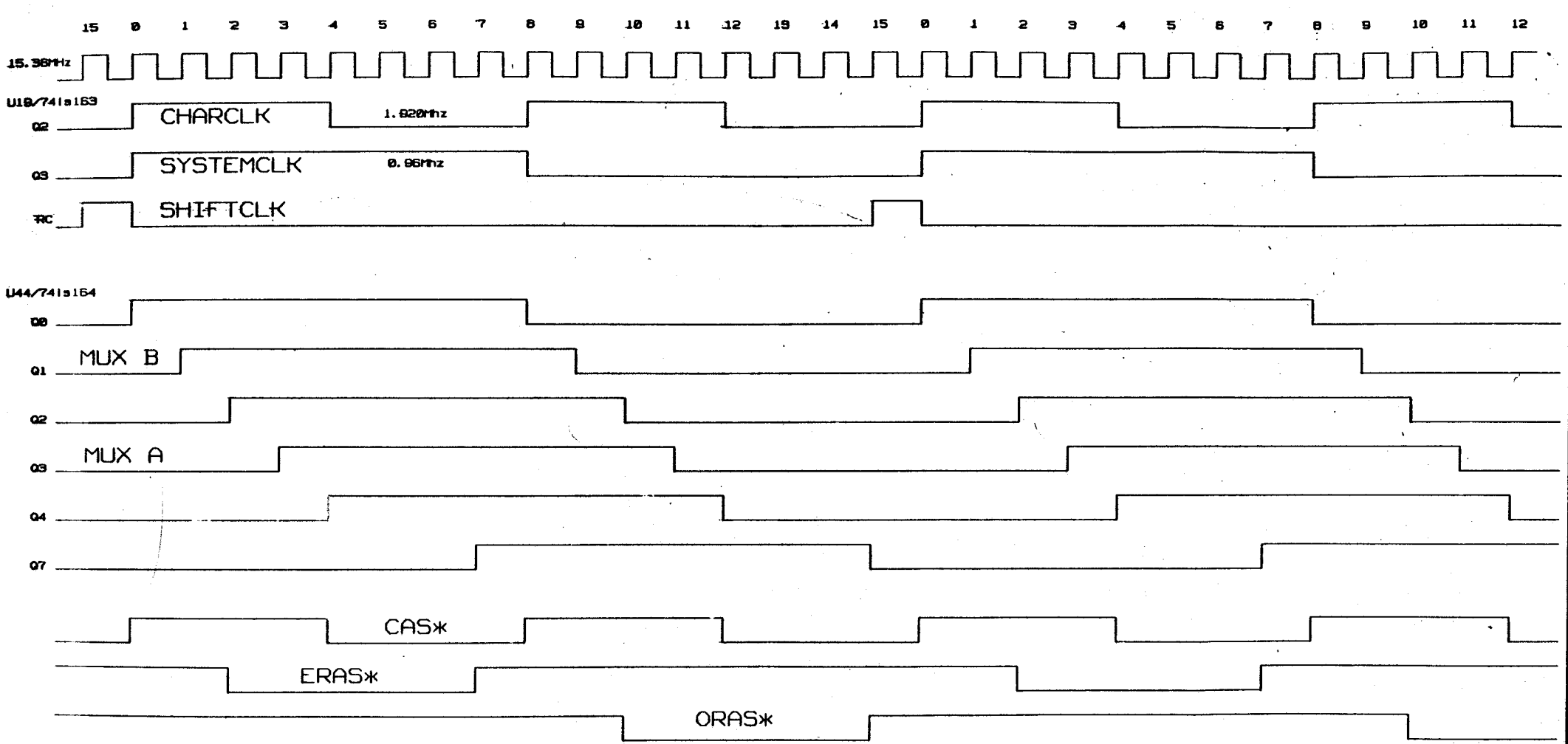
APPROVED:			PAGE: 4 of

REV	ECN	APPROVED	DATE



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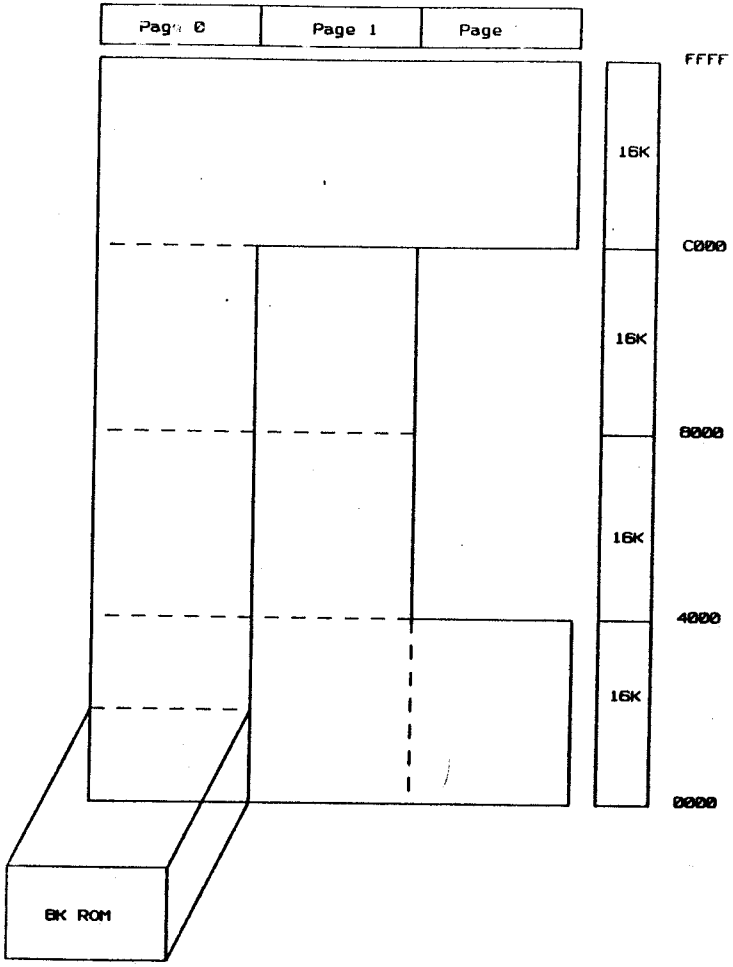
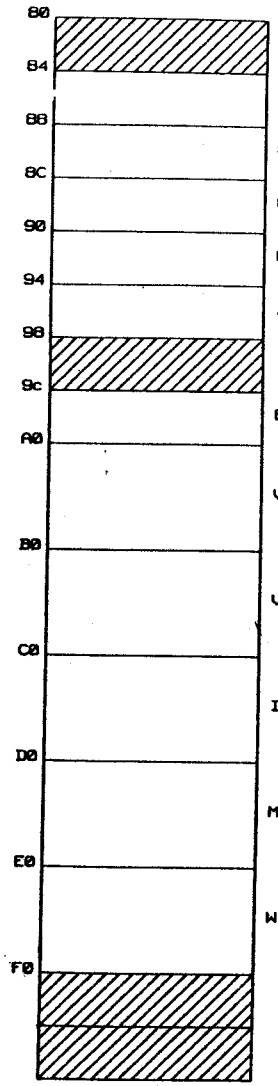
DATE:	10/8/83
PAGE:	5 of

REV	ECN	APPROVED	DATE



V1050 Memory Map



V1050 I/O Map

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ENGINEER: D. Banks
APPROVED:

TITLE: V1050 Block Diagrams

REV: 1A

DATE: 10/8/83