MOTOROLA

MC6845 (1.0 MHz) MC6845☆1 (1.0 MHz)
MC68A45 (1.5 MHz) MC68A45☆1 (1.5 MHz)
MC68B45 (2.0 MHz) MC68B45☆1 (2.0 MHz)

MOS

(N-CHANNEL, SILICON-GATE)

CRT CONTROLLER (CRTC)

CRT CONTROLLER (CRTC)

The MC6845 CRT Controller performs the interface between an MPU and a raster-scan CRT display. It is intended for use in MPU-based controllers for CRT terminals in stand-alone or cluster configurations.

The CRTC is optimized for the hardware/software balance required for maximum flexibility. All keyboard functions, reads, writes, cursor movements, and editing are under processor control. The CRTC provides video timing and refresh memory addressing.

- Useful in Monochrome or Color CRT Applications
- Applications Include "Glass-Teletype," Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays
- Alphanumeric, Semi-Graphic, and Full-Graphic Capability
- Fully Programmable Via Processor Data Bus. Timing May Be Generated for Almost Any Alphanumeric Screen Format, e.g., 80×24, 72×64, 132 ×20
- Single +5 V Supply
- M6800 Compatible Bus Interface
- TTL-Compatible Inputs and Outputs
- Start Address Register Provides Hardware Scroll (by Page, Line, or Character)
- Programmable Cursor Register Allows Control of Cursor Format and Blink Rate
- Light Pen Register
- Refresh (Screen) Memory May be Multiplexed Between the CRTC and the MPU Thus Removing the Requirements for Line Buffers or External DMA Devices
- Programmable Interlace or Non-Interlace Scan Modes
- 14-Bit Refresh Address Allows Up to 16K of Refresh Memory for Use in Character or Semi-Graphic Displays
- 5-Bit Row Address Allows Up to 32 Scan-Line Character Blocks
- By Utilizing Both the Refresh Addresses and the Row Addresses, a 512K Address Space is Available for Use in Graphics Systems
- Refresh Addresses are Provided During Retrace, Allowing the CRTC to Provide Row Addresses to Refresh Dynamic RAMs
- Programmable Skew for Cursor and Display Enable (DE)
- Pin Compatible with the MC6835

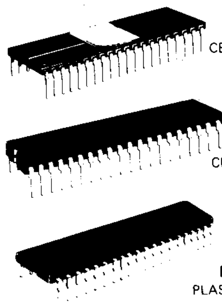
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to +7.0	V
Input Voltage	V_{in}*	−0.3 to +7.0	V
Operating Temperature Range MC6845, MC68A45, MC68B45 MC6845C, MC68A45C, MC68B45C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance Plastic Package Cerdip Package Ceramic Package	θ_{JA}	 100 60 50	°C/W

*This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.



L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734

P SUFFIX
PLASTIC PACKAGE
CASE 711

☆ = Package Suffix

FIGURE 1 — PIN ASSIGNMENTS

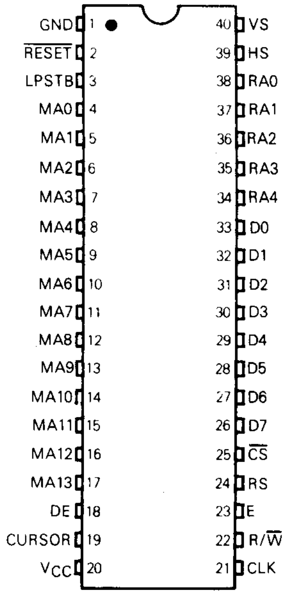


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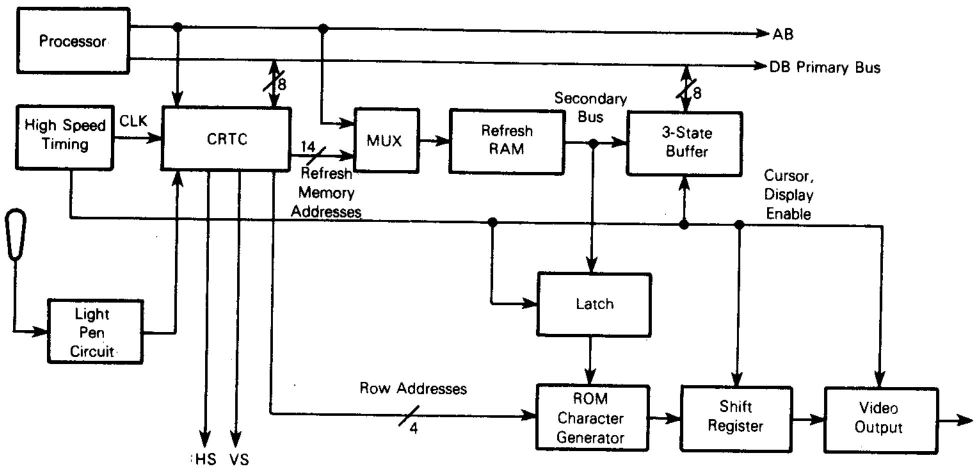
FIGURE 2 — TYPICAL CRT CONTROLLER APPLICATION



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RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D ≡ $P_{INT} + P_{PORT}$

P_{INT} ≡ $I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±10%, V_{SS} = 0, T_A = 0 to 70°C unless otheriwse noted, see Figures 3-5)

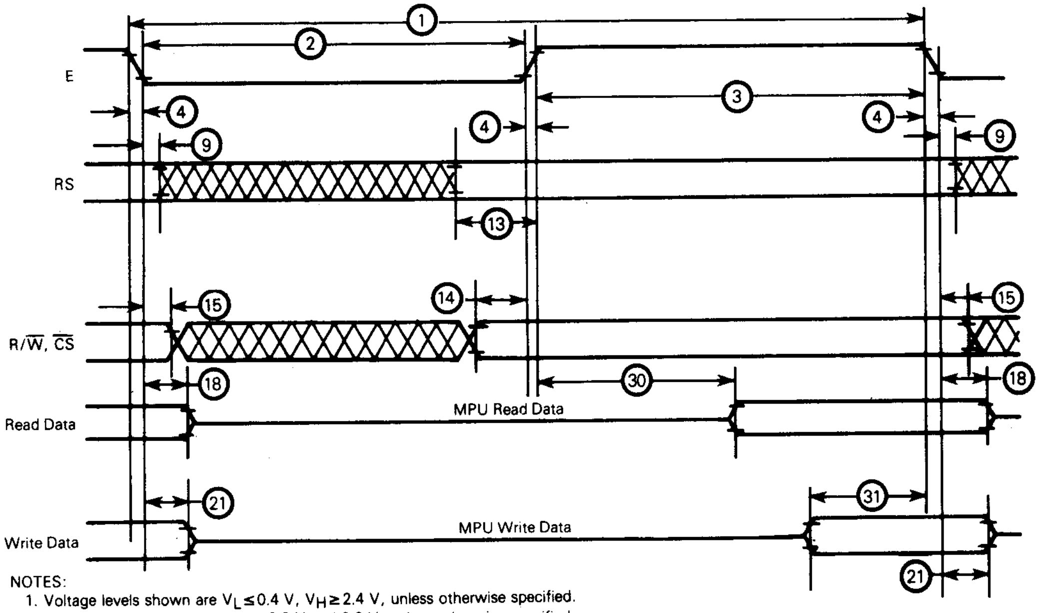
Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	−0.3	–	0.8	V
Input Leakage Current		I_{in}	–	0.1	2.5	μA
Three-State (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	−10	–	10	μA
Output High Voltage (I_{Load} = −205 μA)	D0-D7	V_{OH}	2.4	3.0	–	V
(I_{Load} = −100 μA)	Other Outputs		2.4	3.0	–	
Output Low Voltage (I_{Load} = 1.6 mA)		V_{OL}	–	0.3	0.4	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	600	750	mW
Input Capacitance	D0-D7	C_{in}	–	–	12.5	pF
	All Others		–	–	10	
Output Capacitance	All Outputs	C_{out}	–	–	10	pF

BUS TIMING CHARACTERISTICS (See Notes 1 and 2) (Reference Figures 3 and 4)

Ident. Number	Characteristic	Symbol	MC6845 MC6845☆1		MC68A45 MC68A45☆1		MC68B45 MC68B45☆1		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time (RS)	t_{AH}	10	–	10	–	10	–	ns
13	RS Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	R/$\overline{W}$ and $\overline{CS}$ Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	R/$\overline{W}$ and $\overline{CS}$ Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Peripheral Output Data Delay Time	t_{DDR}	–	290	–	180	0	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR} max (high impedance).

FIGURE 3 — MC6845 BUS TIMING



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

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FIGURE 4 — BUS TIMING TEST LOAD

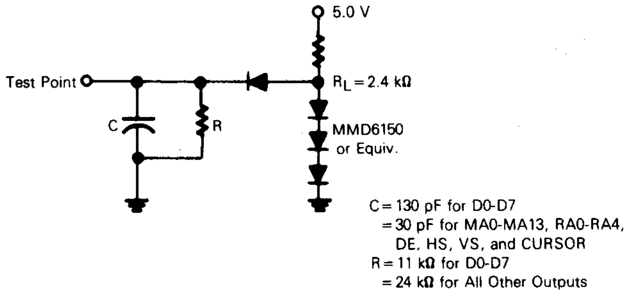
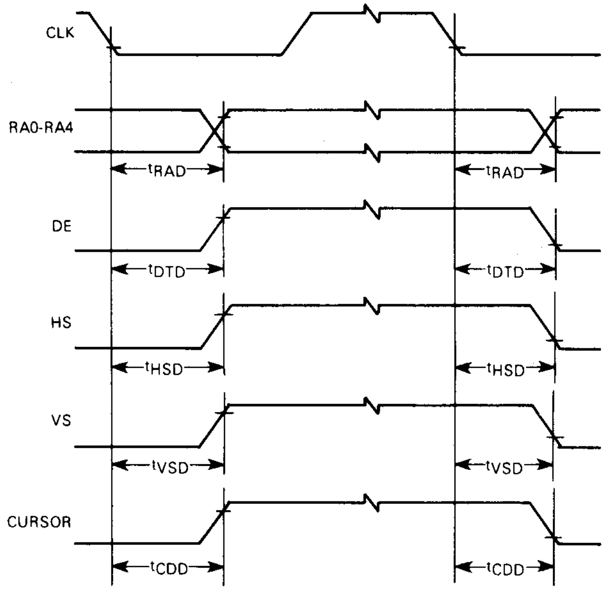
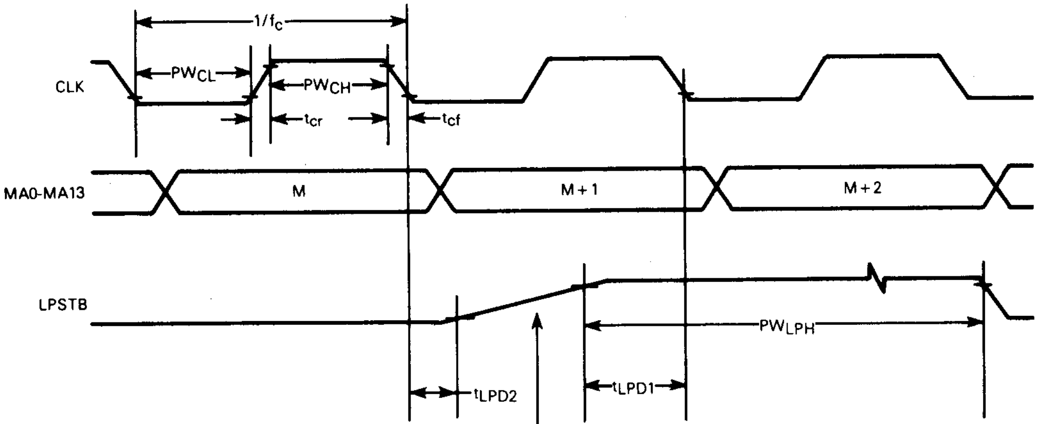


FIGURE 5 — CRTC TIMING CHART



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

FIGURE 6 — CRTC-CLK, MA0-MA13, AND LPSTB TIMING



When the CRTC detects the rising edge of LPSTB in this period, the CRTC sets the Refresh Memory Address 'M+2' into the LIGHT PEN REGISTER.

t_{LPD1}, t_{LPD2}: Period of uncertainty for the Refresh Memory Address.

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

CRTC TIMING CHARACTERISTICS (Reference Figures 5 and 6)

Characteristic	Symbol	Min	Max	Unit
Minimum Clock Pulse Width, Low	PW_{CL}	160	–	ns
Minimum Clock Pulse Width, High	PW_{CH}	200	–	ns
Clock Frequency	f_c	–	2.5	MHz
Rise and Fall Time for Clock Input	t_{cr}, t_{cf}	–	20	ns
Memory Address Delay Time	t_{MAD}	–	160	ns
Raster Address Delay Time	t_{RAD}	–	160	ns
Display Timing Delay Time	t_{DTD}	–	300	ns
Horizontal Sync Delay Time	t_{HSD}	–	300	ns
Vertical Sync Delay Time	t_{VSD}	–	300	ns
Cursor Display Timing Delay Time	t_{CDD}	–	300	ns
Light Pen Strobe Minimum Pulse Width	PW_{LPH}	100	–	ns
Light Pen Strobe Disable Time	t_{LPD1}	–	120	ns
	t_{LPD2}	–	0	ns

NOTE: The light pen strobe must fall to low level before VS pulse rises.

CRTC INTERFACE SYSTEM DESCRIPTION

The CRT controller generates the signals necessary to interface a digital system to a raster scan CRT display. In this type of display, an electron beam starts in the upper left hand corner, moves quickly across the screen and returns. This action is called a horizontal scan. After each horizontal scan the beam is incrementally moved down in the vertical direction until it has reached the bottom. At this point one frame has been displayed, as the beam has made many horizontal scans and one vertical scan.

Two types of raster scanning are used in CRTs, interlace and non-interlace, shown in Figures 7 and 8. Non-interlace scanning consists of one field per frame. The scan lines in Figure 7 are shown as solid lines and the retrace patterns are indicated by the dotted lines. Increasing the number of frames per second will decrease the flicker. Ordinarily, either a 50 or 60 frame per second refresh rate is used to minimize beating between the CRT and the power line frequency. This prevents the displayed data from weaving.

Interlace scanning is used in broadcast TV and on data monitors where high density or high resolution data must be displayed. Two fields, or vertical scans are made down the screen for each single picture or frame. The first field (even field) starts in the upper left hand corner; the second (odd field) in the upper center. Both fields overlap as shown in Figure 8, thus interlacing the two fields into a single frame.

4

In order to display the characters on the CRT screen the frames must be continually repeated. The data to be displayed is stored in the refresh (screen) memory by the MPU controlling the data processing system. The data is usually written in ASCII code, so it cannot be directly displayed as characters. A character generator ROM is typically used to convert the ASCII codes into the "dot" pattern for every character.

The most common method of generating characters is to create a matrix of dots "x" dots (columns) wide and "y" dots (rows) high. Each character is created by selectively filling in the dots. As "x" and "y" get larger a more detailed character may be created. Two common dot matrices are 5×7 and 7×9. Many variations of these standards will allow Chinese, Japanese, or Arabic letters instead of English. Since characters require some space between them, a character block larger than the character is typically used, as shown in Figure 9. The figure also shows the corresponding timing and levels for a video signal that would generate the characters.

Referring to Figure 2, the CRT controller generates the refresh addresses (MA0-MA13), row addresses (RA0-RA4), and the video timing (vertical sync — VS, horizontal sync — HS, and display enable — DE). Other functions include an internal cursor register which generates a cursor output when its contents compare to the current refresh address. A light pen strobe input signal allows capture of the refresh address in an internal light pen register.

All timing in the CRTC is derived from the CLK input. In alphanumeric terminals, this signal is the character rate. The video rate or "dot" clock is externally divided by high-speed logic (TTL) to generate the CLK input. In alphanumeric terminals, this signal is the character rate. The video rate or "dot" clock is externally divided by high-speed logic (TTL) to generate the CLK signal. The high-speed logic must also generate the timing and control signals necessary for the shift register, latch, and MUX control.

The processor communicates with the CRTC through an 8-bit data bus by reading or writing into the 19 registers.

The refresh memory address is multiplexed between the processor and the CRTC. Data appears on a secondary bus separate from the processor's bus. The secondary data bus concept in no way precludes using the refresh RAM for other purposes. It looks like any other RAM to the processor. A number of approaches are possible for solving contentions for the refresh memory:

1. Processor always gets priority. (Generally, "hash" occurs as MPU and CRTC clocks are not synchronized.)
2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.
3. Synchronize the processor with memory wait cycles (states).
4. Synchronize the processor to the character rate as shown in Figure 10. The M6800 processor family works very well in this configuration as constant cycle lengths are present. This method provides no overhead for the processor as there is never a contention for a memory access. All accesses are transparent.

The present version of the CRTC is being upgraded to improve functionality. This data sheet contains the information describing both the MC6845 (present CRTC) and the MC6845☆1 (upgraded CRTC). Complete compatibility between both versions is maintained by programming all register bits, which are undefined/unused, in the MC6845 with zero's.

FIGURE 7 — RASTER SCAN SYSTEM (NON-INTERLACE)

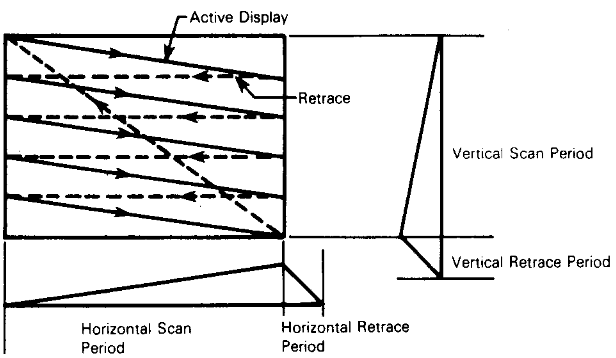


FIGURE 8 — RASTER SCAN SYSTEM (INTERLACE)

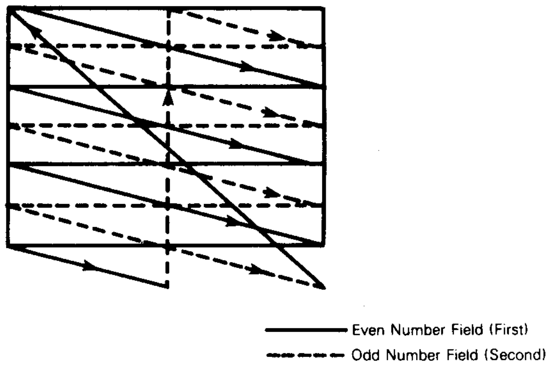


FIGURE 9 — CHARACTER DISPLAY ON THE SCREEN AND VIDEO SIGNAL

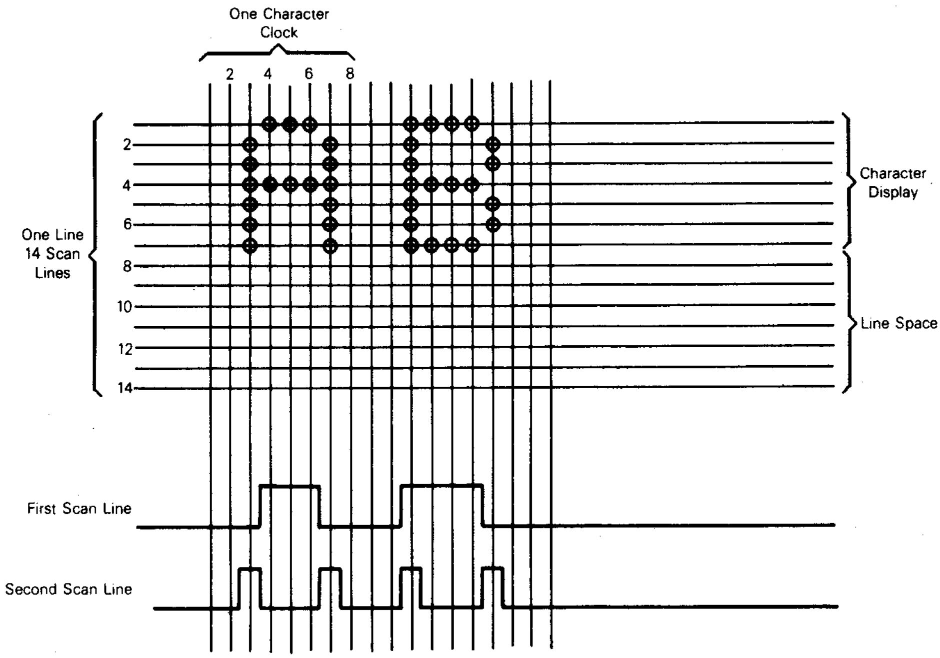
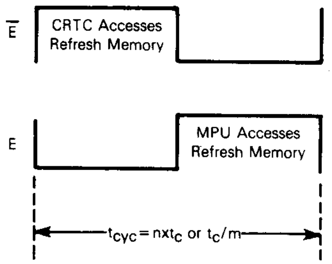


FIGURE 10 — TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING M6800 FAMILY MPU



Where: m, n are integers; t_c is character period

TABLE 1 — CRTC OPERATING MODE

$\overline{RESET}$	LPSTB	Operating Mode
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

The test mode configures the memory addresses as two independent 7-bit counters to minimize test time.

PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) — The bidirectional data lines (D0-D7) allow data transfers between the internal CRTC register file and the processor. Data bus output drivers are high-impedance state until the processor performs a CRTC read operation.

Enable (E) — The Enable signal is a high-impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock. The high-to-low transition is the active edge.

Chip Select ($\overline{CS}$) — The CS line is a high-impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write to the internal register file. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) — The RS line is a high-impedance TTL/MOS compatible input which selects either the address register (RS = "0") or one of the data register (RS = "1") or the internal register file.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ line is a high-impedance TTL/MOS compatible input which determines whether the internal register file gets written or read. A write is defined as a low level.

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and display enable (DE) signals.

NOTE

Care should be exercised when interfacing to CRT monitors, as many monitors claiming to be "TTL compatible" have transistor input circuits which require the CRTC or TTL devices buffering signals from the CRTC/video circuits to exceed the maximum-rated drive currents.

Vertical Sync (VS) and Horizontal Sync (HS) — These TTL-compatible outputs are active high signals which drive the monitor directly or are fed to the video processing circuitry to generate a composite video signal. The VS signal determines the vertical position of the displayed text while the HS signal determines the horizontal position of the displayed text.

Display Enable (DE) — This TTL-compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides memory addresses (MA0-MA13) to scan the refresh RAM. Row addresses (RA0-RA4) are also provided for use with character generator ROMs. In a graphics system, both the memory addresses and the row addresses would be used to scan the refresh RAM. Both the memory addresses and the row addresses continue to run during vertical retrace thus allowing the CRTC to provide the refresh addresses required to refresh dynamic RAMs.

Refresh Memory Addresses (MA0-MA13) — These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs are capable of driving one standard TTL load and 30 pF.

Row Addresses (RA0-RA4) — These five outputs from the internal row address counter are used to address the character generator ROM. These outputs are capable of driving one standard TTL load and 30 pF.

OTHER PINS

Cursor — This TTL-compatible output indicates a valid cursor address to external video processing logic. It is an active high signal.

Clock (CLK) — The CLK is a TTL/MOS-compatible input used to synchronize all CRT functions except for the processor interface. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high-to-low.

Light Pen Strobe (LPSTB) — A low-to-high transition on this high-impedance TTL/MOS-compatible input latches the current Refresh Address in the light pen register. The latching of the refresh address is internally synchronized to the character clock (CLK).

V_{CC}, V_{SS} — These inputs supply +5 Vdc ±5% to the CRTC.

$\overline{RESET}$ — The $\overline{RESET}$ input is used to reset the CRTC. A low level on the $\overline{RESET}$ input forces the CRTC into the following state:

(a) All counters in the CRTC are cleared and the device stops the display operation.

(b) All the outputs are driven low.

(c) The control registers of the CRTC are not affected and remain unchanged.

Functionality of $\overline{RESET}$ differs from that of other M6800 parts in the following functions:

(a) The $\overline{RESET}$ input and the LPSTB input are encoded as shown in Table 1.

(b) After $\overline{RESET}$ has gone low and (LPSTB="0"), MA0-MA13 and RA0-RA4 will be driven low on the falling edge of CLK. $\overline{RESET}$ must remain low for at least one cycle of the character clock (CLK).

(c) The CRTC resumes the display operation immediately after the release of $\overline{RESET}$. DE is not active until after the first VS pulse occurs.

CRTC DESCRIPTION
(Figure 11 CRTC Block Diagram)

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For horizontal timing generation, comparisons result in: 1) horizontal sync pulse (HS) of a frequency, position, and width determined by the registers; 2) horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock which drives the scan line counter and vertical control. The contents of the Raster Counter are continuously compared to the maximum scan line address register. A coincidence resets the raster counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in: 1) vertical sync pulse (VS) of a frequency, width and position determined by the registers; 2) vertical display of a frequency and position determined by the registers.

The vertical control logic has other functions.

1. Generate row selects, RA0-RA4, from the raster count for the corresponding interlace or non-interlace modes.
2. Extend the number of scan lines in the vertical total by the amount programmed in the vertical total adjust register.

The linear address generator is driven by CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA0-MA13, are available for addressing up to four pages of 4K characters, 8 pages of 2K characters, etc. Using the start address register, hardware scrolling through 16K characters is possible. The linear address generator repeates the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blink rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the address counter to be latched in the light pen register. The contents of the light pen register are subsequently read by the processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals — R/$\overline{W}$, $\overline{CS}$, RS, and E.

REGISTER FILE DESCRIPTIONS

The nineteen registers of the CRTC may be accessed through the data bus. Only two memory locations are required as one location is used as a pointer to address one of the remaining eighteen registers. These eighteen registers control horizontal timing, vertical timing, interlace operation, row address operation, and define the cursor, cursor address, start address, and light pen register. The register addresses and sizes are shown in Table 2.

ADDRESS REGISTER

The address register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other eighteen registers. When both RS and $\overline{CS}$ are low, the address register is selected. When $\overline{CS}$ is low and RS is high, the register pointed to by the address register is selected.

TIMING REGISTERS R0-R9

Figure 12 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in character clock time units with respect to the reference as shown in Figure 13. The point of reference for the vertical registers is the top character position displayed. Vertical registers are programmed in scan line times with respect to the reference as shown in Figure 14.

Horizontal Total Register (R0) — This 8-bit write-only register determines the horizontal sync (HS) frequency by defining the HS period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

FIGURE 11 — CRTC BLOCK DIAGRAM

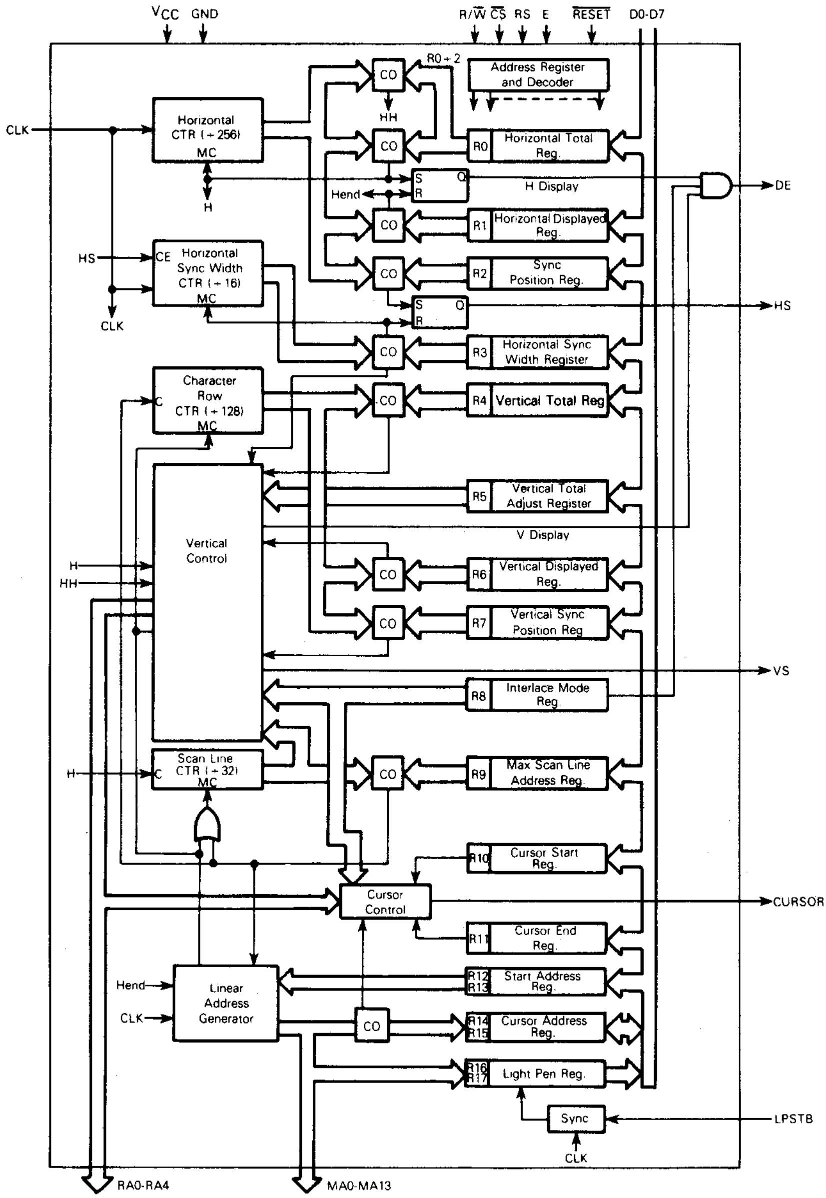


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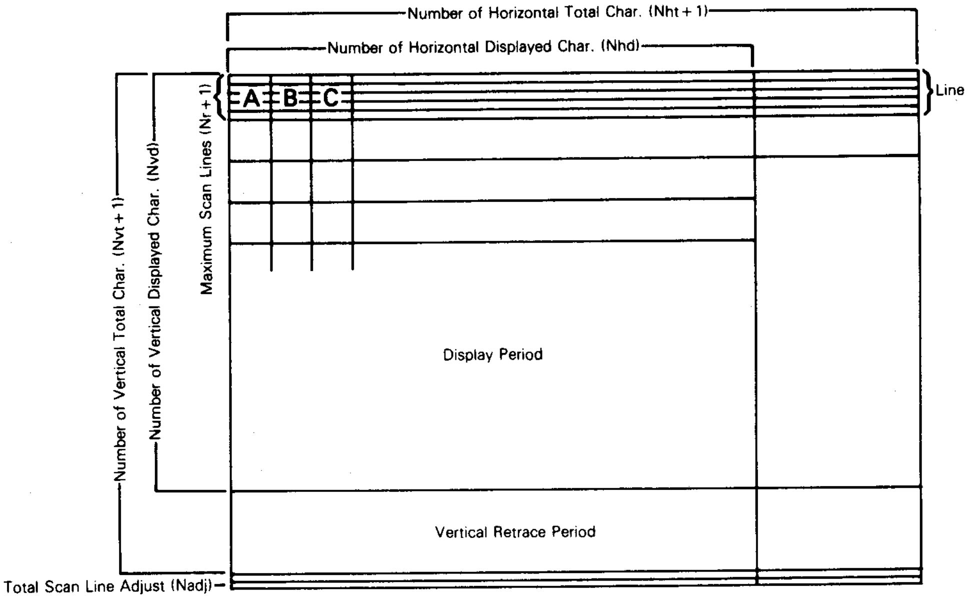
TABLE 2 — CRTC INTERNAL REGISTER ASSIGNMENT
(Features of the MC6845-1 have 1 subscript)

CS̄	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—	\	\	\	\	\	\	\	\
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes	\	\	\					
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes	V_1	V_1	V_1	V_1	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes	\							
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes	\	\	\					
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes	\							
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes	\							
0	1	0	1	0	0	0	R8	Interlace Mode and Skew	Note 1	No	Yes	C_1	C_1	D_1	D_1	\	\	I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes	\	\	\					
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes	\	B	P			(Note 2)		
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes	\	\	\					
0	1	0	1	1	0	0	R12	Start Address (H)	—	Yes	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	Yes	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

NOTES:
1. The skew control is shown in Table 3 and interlace is shown in Table 4.
2. Bit 5 of the Cursor Start Raster Register is used for blink period control, and Bit 6 is used to select blink or non-blink.

FIGURE 12 — ILLUSTRATION OF THE CRT SCREEN FORMAT



Note 1: Timing values are described in Table 8.

4

Horizontal Displayed Register (R1) – This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

Horizontal Sync Position Register (R2) – This 8-bit write-only register controls the HS position. The horizontal sync position defines the horizontal sync delay (Front Porch) and the horizontal scan delay (Back Porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased the display is shifted to the right. Any 8-bit number may be programmed as long as the sum of the contents of R1, R2, and R3 are less than the contents of R0.

Sync Width Register (R3) – This 8-bit write-only register determines the width of the vertical sync (VS) pulse and the horizontal sync (HS) pulse for the MC6845☆1 CRTC. The vertical sync pulse width is fixed at 16 scan-line times for the MC6845 and the upper four bits of this register are treated as "don't cares."

The MC6845☆1 allows control of the VS pulse width for 1-to-16 scan-line times. Programming the upper four bits for 1-to-15 will select pulse widths from 1-to-15 scan-line times. Programming the upper four bits as zeros will select a VS pulse width of 16 scan-line times, allowing compatibility with the MC6845.

For both the MC6845 and the MC6845☆1, the HS pulse width may be programmed from 1-to-15 character clock periods thus allowing compatibility with the HS pulse width specifications of many different monitors. If zero is written into this register then no HS is provided.

Horizontal Timing Summary (Figure 13) – The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor's horizontal scan components. Retrace time is less than the horizontal blanking interval. A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers, the beam overscans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about ⅓ the horizontal scanning period. The horizontal sync delay, HS pulse width, and horizontal scan delay are typically programmed with a 1:2:2 ratio.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) – The frequency of VS is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed in the 5-bit write-only vertical total adjust register (R5) as a number of scan-line times.

Vertical Displayed Register (R6) – This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7) – This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. The value programmed in the register is one less than the number of computed character-line times. When the programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased the display position is shifted down. Any number equal to or less than the vertical total (R4) may be used.

Interlace Mode and Skew Register (R8) – The MC6845 only allows control of the interlace modes as programmed by the low order two bits of this write-only register. The MC6845-1 controls the interlace modes and allows a programmable delay of zero-to-two character clock times for the DE (display enable) and cursor outputs. Table 3 describes operation of the cursor and DE skew bits. Cursor skew is controlled by bits 6 and 7 of R8 while DE skew is controlled by bits 4 and 5. Table 4 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

In the normal sync mode (non-interlace) only one field is available as shown in Figures 7 and 15a. Each scan line is refreshed at the VS frequency (e.g., 50 or 60 Hz).

Two interlace modes are available as shown in Figures 8, 15b, and 15c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VS delayed by ½ scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode the same information is painted in both fields as shown in Figure 15b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, shown in Figure 15c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given bandwidth of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design (e.g., longer persistence phosphors).

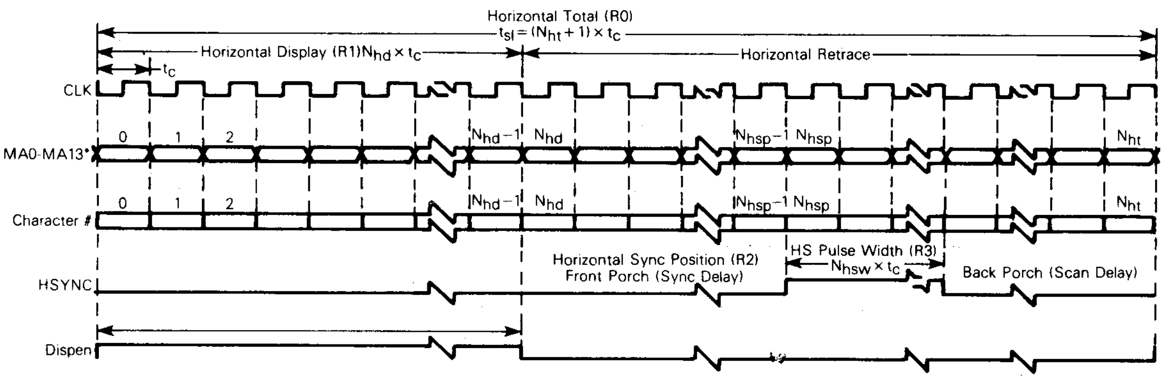
In addition, there are restrictions on the programming of the CRTC registers for interlace operation:

1. For the MC6845:
   a. The horizontal total register value, R0, must be odd (i.e., an even number of character times).
   b. For interlace sync and video mode only, the maximum scan-line address, R9, must be odd (i.e., an even number of scan lines).
   c. For interlace sync and video mode only, the vertical displayed register (R6) must be even. The programmed number Nvd, must be ½ the actual number required. The even numbered scan lines are displayed in the even field and the odd numbered scan lines are displayed in the odd field.
   d. For interlace sync and video mode only, the cursor start register (R10) and cursor end register (R11) must both be even or both odd depending on which field the cursor is to be displayed in.
2. For the MC6845☆1:
   a. The horizontal total register value, R0, must be odd (i.e., an even number of character times).
   b. For the interlace sync and video mode only, the vertical displayed register (R6) must be even. The programmed number, Nvd, must be ½ the actual number required.

TABLE 3 — CURSOR AND DE SKEW CONTROL

Value	Skew
00	No Character Skew
01	One Character Skew
10	Two Character Skew
11	Not Available

FIGURE 13 — CRTC HORIZONTAL TIMING



*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

Note 1: Timing values are described in Table 8.

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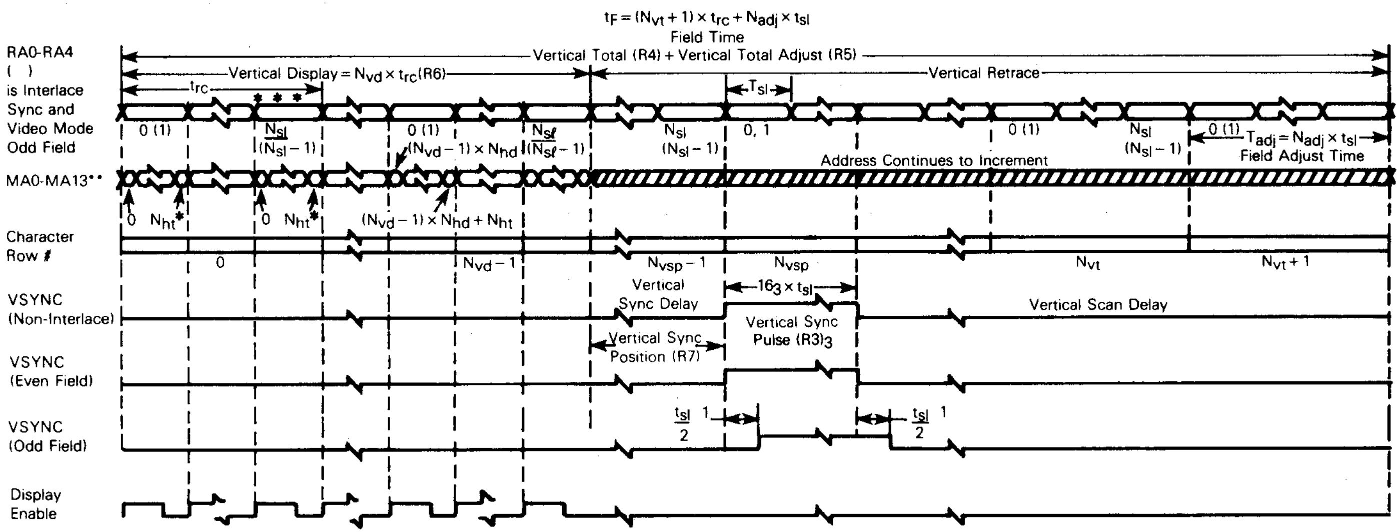
FIGURE 14 — CRTC VERTICAL TIMING



*N_{ht} must be an odd number for both interlace modes.
**Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example.
***N_{sl} must be an odd number for Interlace Sync and Video Mode.

NOTES:
1. Refer to Figure 8 — The Odd Field is offset ½ horizontal scan time.
2. Timing values are described in Table 8.
3. Vertical Sync Pulse width may be programmed from 1 to 16 scan line times for the MC6845☆1.

TABLE 4 — INTERLACE MODE REGISTER

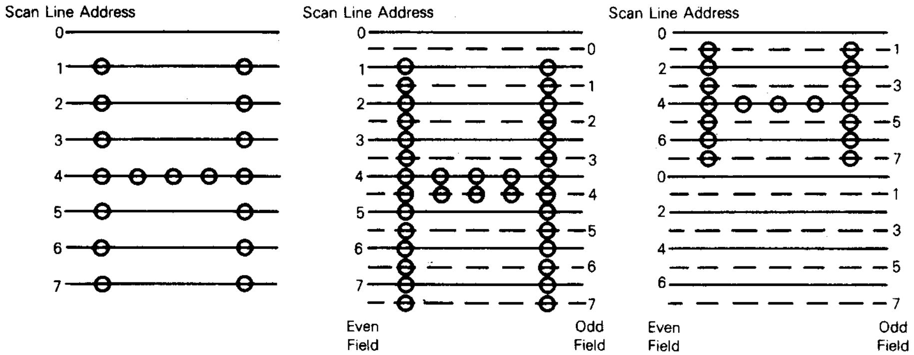
Bit 1	Bit 0	Mode
0 1	0 0	Normal Sync Mode (Non-Interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

TABLE 5 — CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Example of Cursor Display Mode

FIGURE 15 — INTERLACE CONTROL



Maximum Scan Line Address Register (R9) — This 5-bit write-only register determines the number of scan lines per character row including the spacing; thus, controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL

Cursor Start Register (R10) and Cursor End Reigster (R11) — These registers allow a cursor of up to 32 scan lines in height to be placed on any scan line of the character block as shown in Figure 16. R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the cursor start address register control the cursor operation as shown in Table 5. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. R11 is a 5-bit write-only register which defines the last scan line of the cursor.

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

Cursor Register (R14-H, R15-L) — This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area; thus, allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register.

OTHER REGISTERS

Start Address Register (R12-H, R13-L) — This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character, line, or page may be accomplished by modifying the contents of this register.

Light Pen Register (R16-H, R17-L) — This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing an internal synchronizer is designed into the CRTC. Due to delays (Figure 3) in this circuit, the value of R16 and R17 will need to be corrected in software. Figure 17 shows an interrupt driven approach although a polling routine could be used.

CRTC INITIALIZATION

Registers R0-R15 must be initialized after the system is powered up. The processor will normally load the CRTC register file from a firmware table. The worksheet of Table 6 is extremely useful in computing proper register values for the CRTC. Table 7 shows the worksheet filled out for an 80 × 24 configuration using a 7 × 9 character generator and Figure 18 shows an M6800 program which could be used to program the CRT controller. The programmed values allow use of either an MC6845 or MC6845☆1 CRTC.

The CRTC registers will have an initial value at power up. When using a direct drive monitor (sans horizontal oscillator) these initial values may result in out-of-tolerance operation. CRTC programming should be done immediately after power up especially in this type of system.

FIGURE 16 — CURSOR CONTROL

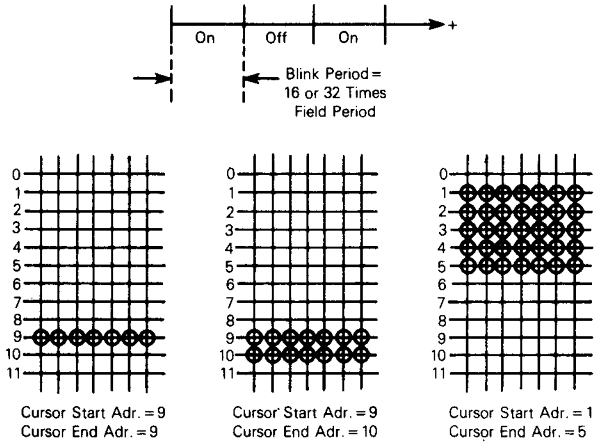


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FIGURE 17 — INTERFACING OF LIGHT PEN

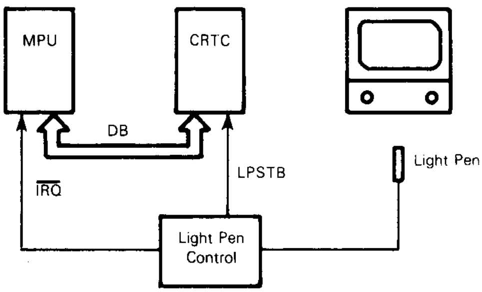


FIGURE 18 — MC6800 PROGRAM FOR CRTC INITIALIZATION

```
PAGE  001   CRTCINIT.SA:0  MC6845 / MC6845-1 CRTC initialization program

                               NAM    MC6845
                               TTL    / MC6845-1 CRTC initialization program
                               OPT    G,S,LLE=85 print FCB's, FDB's & XREF table
                          ***************************************************
                          * Assign CRTC addresses
                          *
              9000   A CRTCAD EQU    $9000    Address Register
              9001   A CRTCRG EQU    CRTCAD+1 Data Register
                          ***************************************************
                          * Initialization program
                          *
A 0000                         ORG    0        a place to start
A 0000 5F                      CLRB            clear counter
A 0001 CE 1020   A             LDX    #CRTTAB  table pointer
A 0004 F7 9000   A CRTC1       STAB   CRTCAD   load address register
A 0007 A6 00     A             LDAA   0,X      get register value from table
A 0009 B7 9001   A             STAA   CRTCRG   program register
A 000C 08                      INX             increment counters
A 000D 5C                      INCB
A 000E C1 10     A             CMPB   $10      finished?
A 0010 26 F2 0004              BNE    CRTC1    no: take branch
A 0012 3F                      SWI             yes: call monitor
                          ***************************************************
                          * CRTC register initialization table
                          *
A 1020                         ORG    $1020    start of table
A 1020      65   A CRTTAB FCB    $65,$50  R0, R1  - H total & H displayed
A 1021      50   A
A 1022      56   A             FCB    $56,$09  R2, R3  - HS pos. & HS width
A 1023      09   A
A 1024      18   A             FCB    $18,$0A  R4, R5  - V total & V total adj.
A 1025      0A   A
A 1026      18   A             FCB    $18,$18  R6, R7  - V displayed $ VS pos.
A 1027      18   A
A 1028      00   A             FCB    $00,$0B  R8, R9  - Interlace & Max scan line
A 1029      0B   A
A 102A      00   A             FCB    $00,$0B  R10,R11 - Cursor start & end
A 102B      0B   A
A 102C      0080 A             FDB    $0080    R12,R13 - Start Address
A 102E      0080 A             FDB    $0080    R14,R15 - Cursor Address
                               END
TOTAL ERRORS 00000--00000


CRTC1  0004  CRTCAD 9000  CRTCRG 9001  CRTTAB 1020
```

4

TABLE 6 — CRTC FORMAT WORKSHEET

Display Format Worksheet

1. Displayed Characters per Row		______	Char.
2. Displayed Character Rows per Screen		______	Rows
3. Character Matrix	a. Columns	______	Columns
	b. Rows	______	Rows
4. Character Block	a. Columns	______	Columns
	b. Rows	______	Rows
5. Frame Refresh Rate		______	Hz
6. Horizontal Oscillator Frequency		______	Hz
7. Active Scan Lines (Line 2 × Line 4b)		______	Lines
8. Total Scan Lines (Line 6 ÷ Line 5)		______	Lines
9. Total Rows Per Screen (Line 8 ÷ Line 4b)		______ Rows	and ______ Lines
10. Vertical Sync Delay (Char. Rows)		______	Rows
11. Vertical Sync Width (Scan Lines (16))		16	Lines
12. Horizontal Sync Delay (Character Times)		______	Char. Times
13. Horizontal Sync Width (Character Times)		______	Char. Times
14. Horizontal Scan Delay (Character Times)		______	Char. Times
15. Total Character Times (Line 1 + 12 + 13 + 14)		______	Char. Times
16. Character Rate (Line 6 × 15)		______	Hz
17. Dot Clock Rate (Line 4a × 16)		______	Hz

CRTC Registers

		Decimal	Hex
R0	Horizontal Total (Line 15 − 1)	______	______
R1	Horizontal Displayed (Line 1)	______	______
R2	Horizontal Sync Position (Line 1 + Line 12)	______	______
R3	Horizontal Sync Width (Line 13)	______	______
R4	Vertical Total (Line 9 − 1)	______	______
R5	Vertical Adjust (Line 9 Lines)	______	______
R6	Vertical Displayed (Line 2)	______	______
R7	Vertical Sync Position (Line 2 + Line 10)	______	______
R8	Interlace (00 Normal, 01 Interlace, 03 Interlace, and Video)		______
R9	Max Scan Line Add (Line 4b − 1)	______	______
R10	Cursor Start	______	______
R11	Cursor End	______	______
R12, R13	Start Address (H and L)	______	______
R14, R15	Cursor (H and L)		______

TABLE 7 — WORKSHEET FOR 80 × 24 FORMAT

Display Format Worksheet

1.	Displayed Characters per Row	80	Char.
2.	Displayed Character Rows per Screen	24	Rows
3.	Character Matrix a. Columns	7	Columns
	b. Rows	9	Rows
4.	Character Block a. Columns	9	Columns
	b. Rows	11	Rows
5.	Frame Refresh Rate	60	Hz
6.	Horizontal Oscillator Frequency	18,600	Hz
7.	Active Scan Lines (Line 2 × Line 4b)	264	Lines
8.	Total Scan Lines (Line 6 ÷ Line 5)	310	Lines
9.	Total Rows Per Screen (Line 8 ÷ Line 4b)	28 Rows and 2	Lines
10.	Vertical Sync Delay (Char Rows)		Rows
11.	Vertical Sync Width (Scan Lines (16))	16	Lines
12	Horizontal Sync Delay (Character Times)	6	Char. Times
13.	Horizontal Sync Width (Character Times)	9	Char. Times
14.	Horizontal Scan Delay (Character Times)	7	Char. Times
15.	Total Character Times (Line 1 + 12 + 13 + 14)	102	Char. Times
16.	Character Rate (Line 6 times 15)	1.8972 M	MHz
17.	Dot Clock Rate (Line 4a times 16)	17.075 M	MHz

CRTC Registers

		Decimal	Hex
R0	Horizontal Total (Line 15 minus 1)	101	65
R1	Horizontal Displayed (Line 1)	80	50
R2	Horizontal Sync Position (Line 1 + Line 12)	86	56
R3	Horizontal Sync Width (Line 13)	9	9
R4	Vertical Total (Line 9 minus 1)	24	18
R5	Vertical Adjust (Line 9 Lines)	10	0A
R6	Vertical Displayed (Line 2)	24	18
R7	Vertical Sync Position (Line 2 + Line 10)	24	18
R8	Interlace (00 Normal, 01 Interlace, 03 Interlace, and Video)		0
R9	Max Scan Line Add (Line 4b minus 1)	11	B
R10	Cursor Start	0	0
R11	Cursor End	11	B
R12, R13	Start Address (H and L)	128	00
			80
R14, R15	Cursor (H and L)	128	00
			80

OPERATION OF THE CRTC

TIMING CHART OF THE CRT INTERFACE SIGNALS

Timing charts of CRT interface signals are illustrated in this section with the aid of programmed example of the CRTC. When values listed in Table 8 are programmed into CRTC control registers, the device provides the outputs as shown in the timing diagrams (Figures 13, 14, 19, and 20). The screen format of this exmaple is shown in Figure 12 which illustrates the relation between refresh memory address (MA0-MA13), raster address (RA0-RA4), and the position on the screen. In this example, the start address is assumed to be "0".

ADDITIONAL CRTC APPLICATIONS

The foremost system function which may be performed by the CRTC controller is the refreshing of dynamic RAM. This is quite simple as the refresh addresses continually run.

Note that the LPSTB input may be used to support additional system functions other than a light pen. A digital-to-analog converter (DAC) and comparator could be configured to use the refresh addresses as a reference to a DAC composed of a resistive adder network connected to a comparator. The output of the comparator would generate the LPSTB input signifying a match between the refresh address analog level and the unknown voltage.

The light pen strobe input could also be used as a character strobe to allow the CRTC refresh addresses to decode a keyboard matrix. Debouncing would need to be done in software.

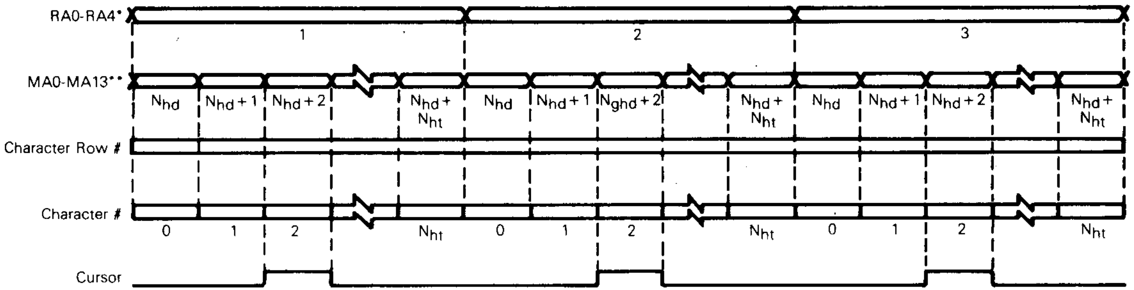
Both the VS and HS outputs may be used as a real-time clock. Once programmed, the CRTC will provide a stable reference frequency.

TABLE 8 — VALUES PROGRAMMED INTO CRTC REGISTERS

Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht}+1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt}+1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start	1	
R11	Cursor End	3	
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)	0	
R15	Cursor (L)	2	
R16	Light Pen (H)		
R17	Light Pen (L)		

4

FIGURE 19 — CURSOR TIMING



*Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:
Cursor Register = $N_{hd}+2$
Cursor Start = 1
Cursor End = 3
**The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

Note 1: Timing values are described in Table 8.

FIGURE 20 — REFRESH MEMORY ADDRESSING (MA0-MA13) STAGE CHART

Vertical region	Character Row	Scan Line	Horizontal Display: Character				Horizontal Retrace (Non-Display)		
Vertical Display	0	0	0	1	→	$N_{hd}-1$	N_{hd}	→	N_{ht}
		N_{sl}	0	1	→	$N_{hd}-1$	N_{hd}	→	N_{ht}
	1	0	N_{hd}	$N_{hd}+1$	→	$2XN_{hd}-1$	$2XN_{hd}$	→	$N_{hd}+N_{ht}$
		N_{sl}	N_{hd}	$N_{hd}+1$	→	$2XN_{hd}-1$	$2XN_{hd}$	→	$N_{hd}+N_{ht}$
	2	0	$2XN_{hd}$	$2XN_{hd}+1$	→	$3XN_{hd}-1$	$3XN_{hd}$	→	$2N_{hd}+N_{ht}$
		N_{sl}	$2XN_{hd}$	$2XN_{hd}+1$	→	$3XN_{hd}-1$	$3XN_{hd}$	→	$2N_{hd}+N_{ht}$
			↓	↓		↓	↓		↓
	$N_{vd}-1$	0	$(N_{vd}-1)\times N_{hd}$	$(N_{vd}-1)\times N_{hd}+1$	→	$N_{vd}\times N_{hd}+1$	$N_{vd}\times N_{hd}$	→	$(N_{vd}-1)\times N_{hd}+N_{ht}$
		N_{sl}	$(N_{vd}-1)\times N_{hd}$	$(N_{vd}-1)\times N_{hd}+1$	→	$N_{vd}\times N_{hd}-1$	$N_{vd}\times N_{hd}$	→	$(N_{vd}-1)\times N_{hd}+N_{ht}$
Vertical Retrace (Non-Display)	N_{vd}	0	$N_{vd}\times N_{hd}$	$N_{vd}\times N_{hd}+1$	→	$(N_{vd}+1)\times N_{hd}-1$	$(N_{vd}+1)\times N_{hd}$	→	$N_{vd}\times N_{hd}+N_{ht}$
		N_{sl}	$N_{vd}\times N_{hd}$	$N_{vd}\times N_{hd}+1$	→	$(N_{vd}+1)\times N_{hd}-1$	$(N_{vt}+1)\times N_{hd}$	→	$N_{vd}+N_{hd}+N_{ht}$
	N_{vt}	0	$N_{vt}\times N_{hd}$	$N_{vt}\times N_{hd}+1$		$(N_{vt}+1)\times N_{hd}-1$	$(N_{vt}+1)\times N_{hd}$		$N_{vt}\times N_{hd}+N_{ht}$
		N_{sl}	$N_{vt}\times N_{hd}$			$(N_{vt}+1)\times N_{hd}-1$	$(N_{vt}+1)\times N_{hd}$		$N_{vt}\times N_{hd}+N_{ht}$
	$N_{vt}+1$	0	$(N_{vt}+1)\times N_{hd}$	$(N_{vt}+1)\times N_{hd}+1$		$(N_{vt}+2)\times N_{hd}-1$	$(N_{vt}+2)\times N_{hd}$		$(N_{v}+1)N_{hd}+N_{ht}$
		$N_{adj}-1$	$(N_{vt}+1)\times N_{hd}$	$(N_{vt}+1)\times N_{d}+1$		$(N_{vt}+2)\times N_{hd}-1$	$(N_{vt}+2)\times N_{hd}$		$(N_{vt}+1)N_{hd}+N_{ht}$

NOTE 1: The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13=0. Only Non-Interlace and Interlace Sync Modes are shown.

ORDERING INFORMATION

MC68A45CP1

- MC — Motorola Integrated Circuit
- 68 — M6800 Family
- A — Blanks = 1.0 MHz; A = 1.5 MHz; B = 2.0 MHz
- 45 — Device Designation In M6800 Family
- C — Temperature Range: Blank = 0° → +70°C; C = −40° → +85°C
- P — Package: P = Plastic; S = Cerdip; L = Ceramic
- 1 — Enhanced Version of CRTC

Replaces "☆" for MC6845☆1 (Temperature Range and Package)

BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S"   Level 2 add "D"   Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles — (−25 to 150°C); Hi Temp testing at T_A max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.